Substrate Bias Enhanced Trap Effects on Time-Dependent Dielectric Breakdown of GaN MIS-HEMTs

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***Abstract*— In this work, we present the substrate bias enhanced trap effects on time-dependent dielectric breakdown (TDDB) in GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) by experiment. Under different substrate biases, the shape parameter β and scale factor η of the Weibull distribution are extracted from the experimental data. A monotonical decrease in β from intrinsic breakdown to extrinsic breakdown relating to the hole-emission from the acceptor-like buffer traps with increased negative substrate biases has been observed, while η is increased at large positive substrate biases. This unexpected increase in η suggests that the donor-like buffer traps play an important role with a longer lifetime. The trap mechanisms, relating to percolation path establishment, are analyzed based on progressive breakdown (PBD). The capacitance–voltage characteristics are measured during each stress cycle confirming the hole fluence and electron injection in the gate-stack layer with different trap distributions under various substrate biases. Finally, 2-D device simulations are carried out to probe for physical insight into the traps on TDDB failure mechanisms.**

***Index Terms*— *C–V* measurement, device simulation, GaN metal–insulator–semiconductor high electron mobility transistor (MIS-HEMT), substrate bias, time-dependent dielectric breakdown (TDDB), trap mechanism.**

I. Introduction

RECENTLY, Gallium nitride (GaN) field-effect transistors (FETs) have received great attention in power electronics applications, due to their high breakdown field, CMOS process compatibility, and the formation of 2-D electron gas (2-DEG) yielding high electron sheet density and mobility [1], [2]. The GaN metal–insulator–semiconductor high electron mobility transistor (MIS-HEMT) is developed as the predominant device structure for power switching applications as it offers lower gate leakage than its HEMT counterpart. Although GaN has excellent material properties, there are still a lot of challenges to overcome before GaN transistors are used for massive commercial deployment [3]–[5]. Particularly, the power electronics market strongly prefers transistors for low-cost, small size, low power consumption, and high reliability. The MIS structure can suppress the leakage current compared with Schottky contact GaN HEMTs and offers a lower cost than p-GaN—both things give it a promising future. However, the time-dependent dielectric breakdown (TDDB), a catastrophic condition arising after prolonged high-voltage gate stress, is a primary reliability concern.

So far, for GaN-based technologies, TDDB evaluation and model analysis have been successfully applied in several gate process technologies including Schottky gate, MIS recessed gate, and enhancement-mode p-type gate [6]–[8]. The leakage current mechanism through the Schottky/GaN junction is studied by Zhang *et al.* [9]. For positive gate voltages, Fowler–Nordheim tunneling is the dominant leakage mechanism until 150 °C, above which the current is taken over by Poole–Frenkel emission (PFE) of electrons from trap states near the metal–semiconductor interface through a continuum of states induced by conductive dislocation lines. The p-GaN gate conduction mechanism has been explored by Bae *et al.* [10], where they report the thermionic emission (TE) of holes from the Schottky contact responsible for gate conduction. The onset of thermally assisted tunneling (TAT) has been reported as field and temperature-dependent, and is why TAT is not visible for temperatures above 75 °C. Furthermore, more and more literature indicates a different physical-statistical behavior of GaN HEMTs compared with that of traditional CMOS Joint Electron Device Engineering Council (JEDEC) standard. Typically, the most conservative model (E-model) is used for extrapolation. However, Moens and Stockman [11] presented the time-to-failure data which show an exponential dependence on $1/I_G$. This suggests there are more underlying physical mechanisms that need to be clarified. Moreover, monolithic GaN chips are necessary for high-speed converters that run up to 10 MHz with reduced noise from parasitic inductances and capacitances. Under different operation conditions, the substrate bias not only affects the dynamic R_{ON} degradation by introducing distinct electron injection from substrate interacted with buffer traps, but it also induces a distinct gate current conduction mechanism relating to gate reliability issues. The physical insight into the current conduction through the material stack linked to the buffer layer should be examined for predicting the lifetime of GaN MIS-HEMTs under different substrate biases.

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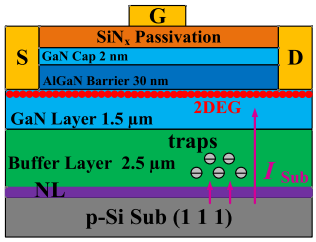

Fig. 1. Cross section of a GaN power device.

In this work, the shape parameter and scale factor in TDDB statistical distributions under different substrate biases are analyzed in order to reveal the substrate bias enhanced trapping processes in the dielectric layer and GaN buffer layer. The hole-emission from ionized acceptor-like buffer traps accelerates the percolation path establishment in the gate-stack layer from extrinsic breakdown to intrinsic breakdown subjected to negative substrate biases. The accumulated holes at the interface between the nuclear layer (NL) and p-type Si substrate help neutralize the donor-like traps, thus releasing the electron injection with increased scale parameters under positive substrate biases. By analyzing the progressive breakdown (PBD) and the *C–V* characteristics, the origin of traps, density, and energy can be obtained. Finally, numerical device simulations accounting for electron/hole distributions are carried out to probe for physical insight into the gate breakdown mechanism due to trap interactions with different substrate biases.

II. Device Description and Measurement Techniques

Devices examined in this work are normally-on (GaN)/AlGaN/GaN structures grown by metal-organic chemical vapor deposition (MOCVD) on a low-resistivity p-type silicon (111) substrate. A schematic of the fabricated device cross section is shown in Fig. 1. The epitaxial layers on top of the silicon substrate contain a layer of 2.5-μm graded AlGaN buffer with Carbon doping and a 1.5-μm-thick GaN layer followed by a 30-nm-thick $Al_{0.3}Ga_{0.7}N$ barrier layer. An extra 2-nm-thick GaN cap layer has been deposited above the barrier layer in order to increase the mobility of the 2-DEG and decrease the surface leakage current. A 140-nm-thick SiN passivation layer has been deposited by plasma enhanced chemical vapor deposition (PECVD) to suppress the current collapse. The drain and source ohmic contacts were formed using Ti/Al/Ni/Au metallization, while the gate contact uses Ni/Au. The Ti/Al/Ni/Au stack offers low contact-resistance for GaN.

The devices under test (DUT) have the gate length L_G of 2 μm, gate–source/drain spacing L_{GS} = 2 μm/ L_{GD} = 4 μm, and gate width of 100 μm. On-the-wafer characterization has been performed using a Keithley 4200 A Semiconductor Characterization System. During the stress phase, constant gate voltage V_G and substrate bias V_B are applied, while the source and drain are grounded. Under the constant voltage stress (CVS) phase, the gate leakage current was continuously monitored until it reached 1 mA, the current level chosen for the breakdown condition.

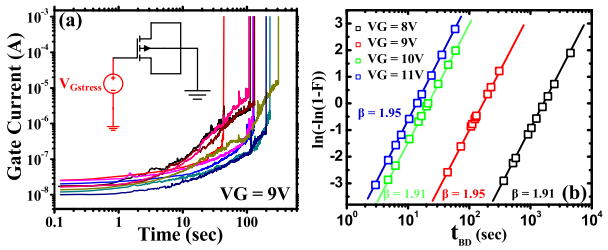

Fig. 2. (a) Gate leakage current under CVS. (b) Weibull distributions for different gate voltages.

III. Experimental Results and Discussion

The relationship between initial gate leakage current (I_G) for selected samples, monitored at the start of the stress, and breakdown time (t_{BD}) is displayed in Fig. 2. Fig. 2(a) shows that the I_G monotonically increases with stress time, which demonstrates the charge trapping process during stress. After a certain stress time, the gate leakage current becomes noisy. This is mainly attributed to the gradual formation of the percolation path. Once the full percolation path has been formed, the gate dielectric hard breakdown (HBD) occurs, which causes a sudden increase of the gate leakage current [see vertical lines in Fig. 2(a)]. Based on the theory of the percolation path formation [12], t_{BD} was extracted from the time corresponding to an increase in the leakage current to 1 mA.

t_{BD} for gate dielectric degradation, which shows a statistical distribution, follows the well-known Weibull distribution of

$$F(t) = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \tag{1}$$

where t is the time, β is the shape parameter, η is the scale factor of 63.2% value, and γ is the time delay or burn-in time. Assuming $\gamma = 0$, the Weibull failure distribution can be expressed as

$$ln[-ln(1-F(t))] = \beta ln(t) - \beta ln(\eta). \tag{2}$$

In the case of Weibull distributed data, a plot of $ln(-ln(1-F(t))$ versus $ln(t)$ yields a straight line with a slope β and intercept $ln(\eta)$.

The parameter β is strongly related to the number of defects forming the percolation path. Indeed, it has been shown in [12] that

$$\beta = mN \tag{3}$$

where m is the trap generation rate and N is the number of defects needed to form the percolation path.

In this work, the Weibull plot could be built based on the time-to-breakdown distributions for different gate voltages, as shown in Fig. 2(b). The shape parameter β is close to 1.91 under different gate stress conditions, thus indicating the same physical conduction model. According to [13], the trap-assisted Poole–Frenkel emission (PFE) through a defect band is near the valence band with a trap depth of $q\Phi_b = 0.48$ eV. Close to the metal/dielectric interface, charge states are introduced near the hole quasi-Fermi level in the forbidden zone, which act as hole traps. The electric field at the interface is

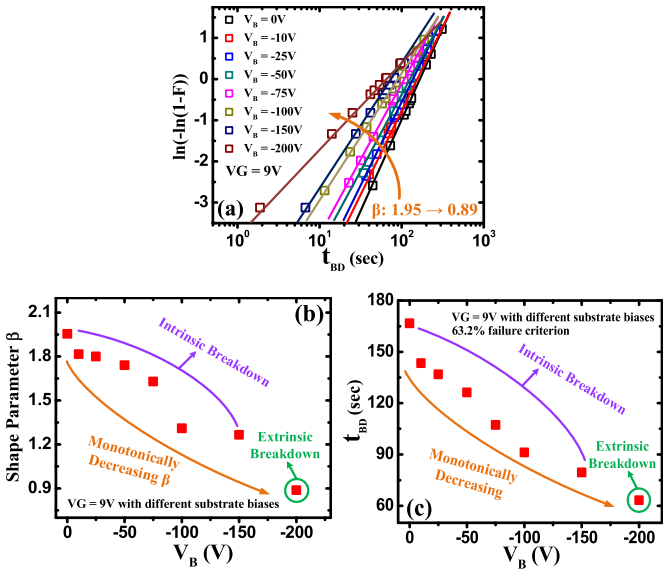

Fig. 3. (a) Weibull distributions under negative substrate biases. (b) Shape parameter versus negative substrate bias. (c) Time to 63.2% failure for different negative substrate biases.

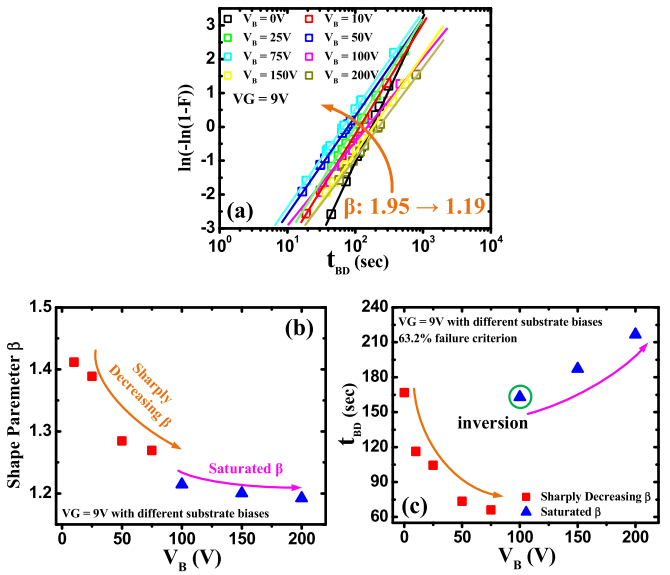

Fig. 4. (a) Weibull distributions under positive substrate biases. (b) Shape parameter versus positive substrate bias. (c) Time to 63.2% failure under positive substrate biases.

sufficiently high to initiate the PFE emission under high gate voltage, and this condition governs the conduction mechanism until HBD.

In the case of monolithic integration of GaN-based power electronics, since the conductive Si substrate is connected to both high and low side devices, the buffer traps induced from different substrate biases are expected to interact with the percolation path formation. The Weibull distribution of t_{BD} under different negative substrate biases with the same CVS is shown in Fig. 3(a). The shape parameter β monotonically decreases to less than 1 where the extrinsic breakdown occurs at $V_B = -200$ V. Fig. 3(b) shows a summary of the extrapolated shape parameters versus substrate voltage. The decreasing β with an increase in negative substrate bias indicates a spread distribution and large variability. According to (3), the decreased β implies that a smaller amount of traps form the percolation path in the device. However, the total amount of traps from PFE to establish the percolation path is constant according to the percolation model [12]. Consequently, during the TDDB experiments with increased negative substrate biases, the acceptor-like buffer traps will reduce the trap generation rate by depleting 2-DEG, resulting in smaller β [14]. It is worth noting that the type of failure has changed from intrinsic breakdown to extrinsic breakdown when the substrate bias increases to -200 V. The intrinsic breakdown is caused by electrical stress-induced defect generation, like the PFE mechanisms discussed before. The extrinsic breakdown is usually believed to be linked with process-induced imperfections such as impurities, roughness, thinning, structural weakness, and so on [15]. The depleted 2-DEG cannot provide enough electron injection into the passivation layer to establish the trap-assisted percolation path. Otherwise, the initial damage, dislocation, and roughness from the PECVD deposition of the passivation layer could be the dominant source of the percolation path. In the meantime, the scale factors which refer to 63.2% failure criterion have been extracted under different substrate biases, as shown in Fig. 3(c). Although the trap generation rate is reduced because of depleted 2-DEG density, more accelerated electrons are from the 2-DEG due to a built-in electric field from the surface to the bottom under negative substrate bias. These high-speed and energized electrons will induce more interface traps between the passivation (dielectric) layer and the semiconductor. The damaged passivation layer results in a decrease in scale factor [16], an indication of a shorter device lifetime.

The Weibull distributions of GaN MIS-HEMTs under positive substrate biases are shown in Fig. 4(a). Distinct shifts of β and η under positive substrate biases have been demonstrated in Fig. 4(b) and (c). According to our previous study [17], positive substrate biases will induce a negative band-gap bending with more electron injection from the top dielectric layer to the bottom GaN layer. The injected electrons from the dielectric layer will neutralize the ionized donor-like traps partially. Those injected electrons provide a lot of traps at the interface between the dielectric layer and GaN layer with increased trap generation rates. Although those injected electrons provide a lot of traps at the interface between the dielectric layer and semiconductor layer with increased trap generation rates, the accelerated electrons introduce a vulnerable passivation layer, which reduces the required number of defects needed to form the percolation path [12]. According to (3), a decreased β is seen in Fig. 4(b) when V_B is less than $+100$ V. On the other hand, the high trap generation rate under electron injection forms the percolation path quickly with decreased η. Nevertheless, it is interesting to note both the shape parameter and scale parameter show different performance when V_B is larger than $+100$ V. Under those very high forward substrate biases, the p-type substrate is under strong inversion which provides enormous holes through the NL and substrate junction [18]. These holes will partially neutralize the donor-like buffer traps with saturated β and increased η. As per the analysis below, the neutralized donor-like traps

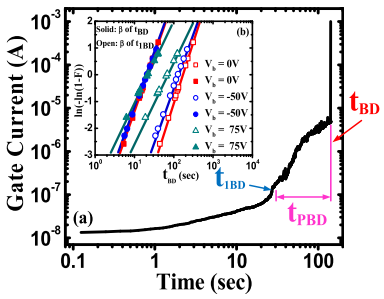

Fig. 5. PBD and Weibull distributions for the first time breakdown.

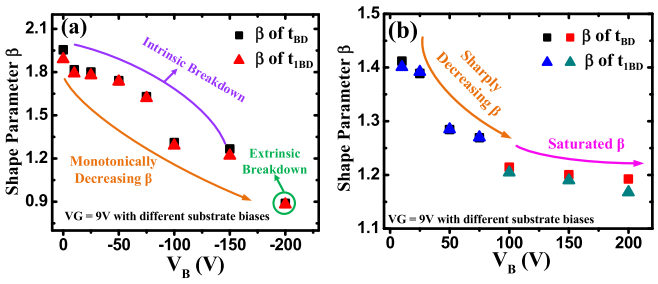

Fig. 6. Shape parameter versus (a) negative substrate bias and (b) positive substrate bias for the first time breakdown.

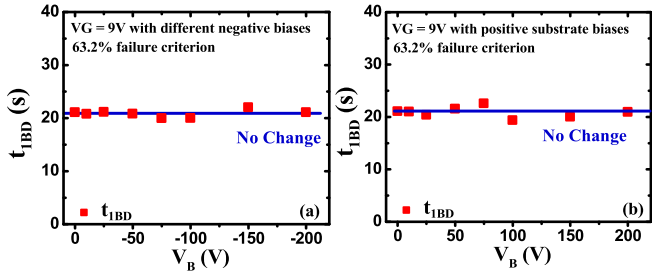

Fig. 7. First time to breakdown versus (a) negative substrate bias and (b) positive substrate bias.

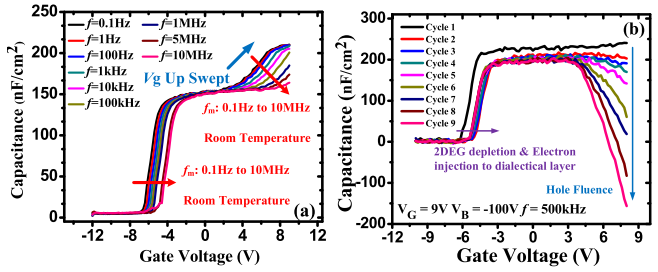

Fig. 8. *C–V* characteristics subjected to different (a) frequencies and (b) cycles.

cannot provide more electron injection to the dielectric layer with saturated trap generation. Meanwhile, less damage from electron injection in the dielectric layer mitigates the quality degradation with an increased scale factor. This result also indicates a longer lifetime of GaN MIS-HEMTs under very high positive substrate biases.

In order to further explore the failure mechanism under different substrate biases, the PBD has also been examined under different substrate biases. Fig. 5 shows the evolution of the gate current in a typical constant-voltage TDDB experiment at $V_G = 9$ V. This plot shows that the gate current is noisy before approaching HBD, a condition known as PBD [14]. PBD reflects the formation of a breakdown path created by these defects within the dielectric. After the onset of PBD, further stress increases the gate current noise between the time-to-first-breakdown, $t_{1BD,}$ and the time-lapse between t_{1BD} and t_{BD} as the length of PBD, or t_{PBD}. The inset of Fig. 5 shows the Weibull plot for t_{1BD}, and t_{BD} of several devices, stressed under selected substrate biases. The nearly parallel shift in the Weibull distributions of 1BD and HBD suggests a common origin for the two phenomena. Once the first breakdown occurs, additional gate stress continues to generate defects randomly. Eventually, HBD takes place when it becomes nearly ohmic. In addition, the shape parameter energy is delivered to the PBD breakdown path so that it is relating to the trap generation in the dielectric of t_{1BD} and t_{BD} under different substrate biases, as shown in Fig. 6. The same distribution of β under both negative and positive substrate biases verifies that the origin for $t_{1BD}$and t_{BD} follows the same trap mechanisms. Interestingly, the scale factor of t_{1BD} remains the same under different negative and positive substrate biases, as shown in Fig. 7. This indicates that the initial establishment of a percolation path is not dependent on the buffer traps induced by the substrate biases. Above all, the creation of a percolation path is strongly dependent on the dielectric material itself, while the defect accumulation process after time-to-first-breakdown is strongly related to GaN buffer traps.

Following the TDDB measurement, we extract the trap density distributions using the *C–V* characteristics during each cycle of the gate stress. The measured *C–V* curves of fresh GaN MIS-HEMTs with two sharp rising slopes are shown in Fig. 8. In this plot, the first rising slope is due to the generation of a 2-DEG and the second rising slope is caused by nonuniform interface traps [19]. An analysis of interface traps on SiN/GaN/AlGaN/GaN HEMTs has been conducted to focus on the f/T dispersion of the second slope onset in the *C–V* characteristics.

Based on the Shockley–Read–Hall (SRH) recombination theory, the following equations are used to extract the energy level and density distributions [20]:

$$\tau_T = \frac{1}{f_m} = \frac{1}{\upsilon_{th}\sigma_n N_c}\exp\left(\frac{E_C - E_T}{kT}\right) \tag{4}$$

$$\Delta V'_{2\_f1f2} = \frac{C_{br}}{C_{br} + C_{\text{Passivation}}}\Delta V_{2\_f1f2} \tag{5}$$

$$D_{it}\left(E_C - E_T = \frac{\Delta E_{T\_f1} + \Delta E_{T\_f2}}{2}\right) = \frac{C_{\text{Passivation}} \cdot \Delta V'_{2\_f1f2}}{q \cdot \left(\Delta E_{T\_f1} - \Delta E_{T\_f2}\right)} \tag{6}$$

where $C_{\text{passivation}}$ is the capacitance of the dielectric layer, C_{br} is the equivalent capacitance of the GaN/AlGaN layer, υ_{th} is the electron thermal velocity, σ_n is the electron capture cross section, and N_c is the effective density of states of GaN in the conduction band.

However, a sharp decreasing slope is seen when the *C–V* characteristics are recorded during each gate stress cycle under negative substrate bias, as shown in Fig. 8(b). The second

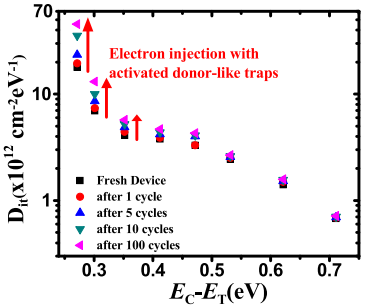

Fig. 9. Traps distribution after constant gate voltage stress cycles without a substrate bias.

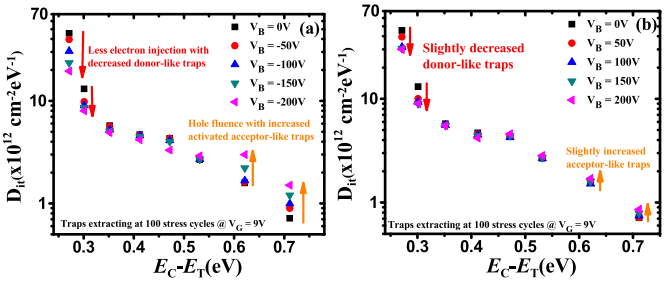

Fig. 10. Traps distribution after constant gate voltage stress cycles for (a) negative substrate biases and (b) positive substrate biases.

slope is related to the surface traps with the same polarity as the 2-DEG. The decreased slope in Fig. 8(b) indicates that holes are generated with the opposite polarity of the 2-DEG. A larger decreased capacitance at the second slope region suggests a greater hole fluence induced by the negative substrate bias. Because the f/T dispersion of the second slope onset can still be observed in Fig. 8(b), (4)–(6) can be applied to extract the distributions of the traps from $E_C - 0.71$ eV to $E_C - 0.27$ eV. The hole emission will not only deplete the 2-DEG, but also activate the deeper-level traps in the interface as well. So, the extracted traps lower than $E_C - 0.5$ eV can be regarded as in reference to the hole-emission process from buffer traps, while the extracted traps beyond $E_C - 0.5$ eV can be considered as interface donor-like traps.

The extracted trap distributions after a certain gate voltage stress cycles without a substrate bias are shown in Fig. 9. The increase in gate voltage stress time results in a significant increase in shallow-level traps (E_C-E_T $<$ 0.5 eV). Note that the variation of deeper-level traps (E_C-E_T $>$ 0.5 eV) is negligible compared with that of shallow-level traps. The experimental data here demonstrate that the released electrons from the donor-like traps are mainly responsible for the breakdown under constant gate voltage stress. However, when the trap distributions under different substrate biases are extracted, as shown in Fig. 10, two different trap mechanisms are discovered. With the increased negative substrate biases, a significant decrease in shallow-level traps and an increase in deeper-level traps are illustrated in Fig. 10(a). The hole fluence from ionized acceptor-like not only depletes the 2-DEG but plays an important role in releasing the electron injection with different gate breakdown mechanisms under negative substrate biases [12], [21]. The shape parameter β, relating to established traps in the dielectric layer, will be reduced with less electron injection from the decreased donor-like traps and depleted 2-DEG. A different trap-related breakdown behavior is analyzed with distinct trap distributions under positive substrate biases, as shown in Fig. 10(b). The electron injection from the dielectric layer neutralized the donor-like traps partially under positive substrate biases. And compared with that under negative substrate biases, the decreased shallow-level traps reach a saturated point at high positive substrate biases, which follows the saturation of β at high positive substrate biases in Fig. 4(b). The slightly increased deeper-level traps due to the accumulation of holes in the inverted p-type silicon substrate provide fewer mirror electrons to ionize the acceptor-like traps. These ionized acceptor-like traps will also release the electrons from the donor-like traps with increased η as seen in Fig. 4(c).

IV. Sentaurus Device Simulation Results

A Sentaurus 2-D simulation is used to probe for physical insight into the trap mechanism relating to the observed breakdown mechanism under constant gate voltage stress from the experiment. The AlGaN/GaN device structure shown in Fig. 1 is examined in simulation. The source and drain contacts are implemented using heavily doped GaN to form ohmic contacts. The high-field mobility saturation model and inverse piezoelectric effect are adjusted to improve the simulation accuracy and consistency with the device situation. The polarization scale parameter with 0.29 has been implemented to be consistent with the measured experimental data [22]. SRH and Dynamic Nonlocal Path Trap-assisted Tunneling Model are enabled to simulate the trapping and detrapping mechanisms under different gate voltage stresses. The self-heating effect including the lattice temperature model and electron/hole thermal model is enabled to monitor possible hole/electron emission processes. The buffer layer is set as a low mole-fraction AlGaN to mimic graded buffer layers in fabrication. In the device simulation, a Gaussian distribution with a peak density of 10^{19} cm^{-3} shallow compensating donors in the Carbon-doping buffer layer is implemented. As shown in [23], trapping phenomena in the Carbon-doped buffer layer can be reproduced by adopting deep-level acceptor-like traps with a concentration almost two orders of magnitude lower than that at the nominal Carbon doping level. Therefore, low-density deep-level ($E_V + 0.9$ eV) acceptor-like traps (10^{15} cm^{-3}) with deeper-level capture cross section area of 10^{-15} cm^2 are used in the buffer layer. In order to verify the trap effect on the gate breakdown mechanism, an evaluation of the parameters under time-transient voltage stresses is simulated. The key parameters used in the 2-D simulation are listed in Table I.

Using the abovementioned physical models in the device simulation, the simulated electron density distribution before the gate breakdown at different gate voltages is shown in Fig. 11. Since the trap emission model [24] may not be accurate enough, we add measured interface trap distributions at the GaN cap/Nitride interface, extracted from reference [4], to mimic the electron injection to the gate subjected to different gate voltages. The electron density as a function of gate voltage stress successfully reflects the trap effect observed

TABLE I
KEY PARAMETERS USED IN SIMULATION

Parameter	Value
Gate-source spacing	2 μm
Gate-drain space	4 μm
Gate length	2 μm
Gate width	100 μm
Al mole fraction of barrier layer	0.23
Al mole fraction of buffer layer	0.01
Gate metal work-function	4.25 V
Polarization scale parameter	0.29
Shallow compensating donors in the GaN buffer	1×10^{19} cm^{-3}
Acceptor-like traps doping concentration	1×10^{17} cm^{-3}

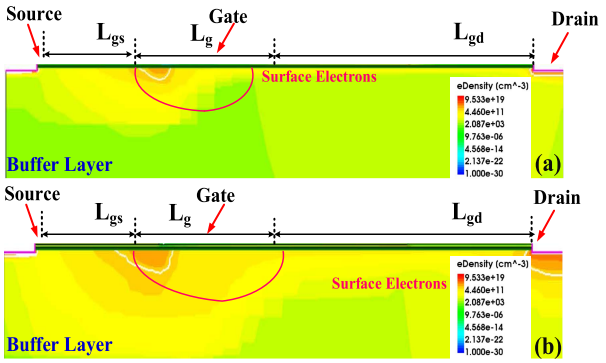

Fig. 11. Electron distribution under the gate voltage stress of (a) $V_G = 4$ V and (b) $V_G = 9$ V.

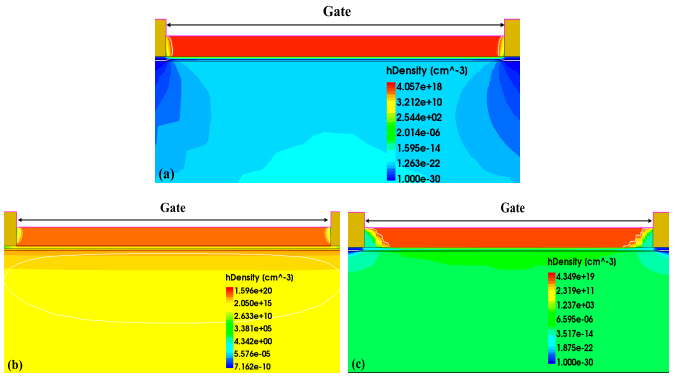

Fig. 12. Hole distribution after a constant gate voltage stress under (a) no-substrate bias, (b) negative substrate bias, and (c) positive substrate bias.

by the experiment. A larger high electron density area is shown under the gate region which acts as the source of electron injection to the gate with the increased gate voltage. This confirms that the released electrons from the donor-like traps are responsible for the gate breakdown in the absence of a substrate bias.

To examine the simulation results further, the hole density of the dielectric layer under different substrate biases is depicted in Fig. 12. Compared with the peak hole density in the gate region at $V_B = 0$ V, higher hole density is observed under both positive and negative substrate biases. The simulation results imply that the hole fluence from the ionized acceptor-like traps will modulate the electron injection process with different gate breakdown mechanisms. And compared with the hole density under a positive substrate bias, higher hole density is shown under a negative substrate bias which demonstrates that more acceptor-like traps are ionized.

V. CONCLUSION

The correlation between substrate bias-enhanced traps and TDDB in the GaN MIS-HEMT is studied by experiment. The hole fluence from ionized acceptor-like traps releasing the electron injection from 2-DEG results in a monotonic decrease in shape parameter β from intrinsic breakdown to extrinsic breakdown. Two different trap mechanisms, with decreased β and increased scale parameter η, have been observed under positive substrate biases. The statistical parameters of PBD have been examined. The percolation path in the GaN MIS-HEMT is strongly dependent on the dielectric material itself, while the trap generation process is heavily related to the GaN buffer traps induced from deep-level traps. The traps at different energy levels are extracted from the C–V characteristics, which successfully reveal the electron/hole emission processes from the traps. Finally, the electron/hole distributions relating to different gate voltages and substrate biases have been verified via the physical insight of device simulation results.

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