Fixtures Design Considerations for Impedance Measurement

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***Abstract*— The parasitic impedance in a current commutation loop (CCL) is a major factor for the switching performance of power electronics especially the wide bandgap (WBG) devices, which usually generate high di/dt. The terminals of components in a CCL may not always be standard. The fixture adapter with clip lead may not be accurate enough for WBG application, while the commercial high bandwidth fixture adapters are not always available. Therefore, it is critical to design fixture adapter boards to make a better interface and mitigate measurement errors. In this work, detailed fixture design procedures are presented. These design methods were validated by comparing with the commercial fixture adapters. In addition, various considerations to further improve the measurement accuracy are discussed, summarized, and evaluated through tests. The dc-link capacitors and the busbar for a half-bridge module are regarded as the device under test, whose impedance is extracted using the proposed fixture design. Finally, the experimental results from the double pulse test verified the accuracy of the proposed fixture design, with an error of less than 1%.**

Keywords—fixture adaptor; impedance analyzer; impedance measurement; parasitic inductance.

I. INTRODUCTION

The large stray inductance over a current commutation loop (CCL) may lead to switching oscillations, voltage overshoot, and additional power losses [1], [2], especially when using silicon carbide (SiC) devices. The stray inductances in a high-power CCL may come from 1) dc-link capacitors, 2) the power modules [3], [4], and 3) busbars connecting capacitors to power modules [4]-[7]. For dc-link capacitors, their stray inductance information provided by the manufactures is usually the reference value instead of the actual value, and it is difficult to obtain through the simulation. As a result, it is recommended to measure and compare the stray inductance by using an impedance analyzer during the capacitor selection process. In addition, when a busbar is built, it is necessary to measure the parasitic inductance before its application to ensure its performance can match the finite element analysis (FEA) simulation result [8]-[10] in the early stage. The problem is that the most accurate off-the-shelf adapter fixture with high-bandwidth, e.g., greater than 10MHz, is designed for

(a)

(b)

(c)

Fig. 1. Commercial fixture adapter of impedance analyzer (a) for SMD (b) for leaded passive device (c) with clip lead.

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surface mount device (SMD) or leaded passive device, as shown in Fig. 1(a) and (b). When it comes to larger components like dc-link capacitor and custom busbars with screw terminals, the only choice for adapter fixture is clip lead, as shown in Fig. 1(c), most of which designed with low-bandwidth accuracy, e.g., less than 100kHz. Meanwhile, the connection between clip leads and device under test (DUT) is not stable, and the measurement result will change when the position of clip leads slightly moves. To solve this problem and make better interface between the impedance analyzer and DUT with different kinds of terminals, it is better to build customized adapter fixtures.

References [11] and [12] claimed that an impedance analyzer with a custom fixture board was used to measure the busbar impedance. However, no details on the fixture board design have been presented. In [13], custom fixture boards were designed for impedance measurement of power modules, and the results obtained using commercial and custom fixtures were compared with each other. However, there are no fixture board design considerations and guidance presented in this literature. In this work, a detailed design procedure on the fixture adapters is presented, which has not been discussed in the existing literature. In addition, various fixture designs are compared to conclude design guidance. Furthermore, the proposed design approach has been validated by experimental studies.

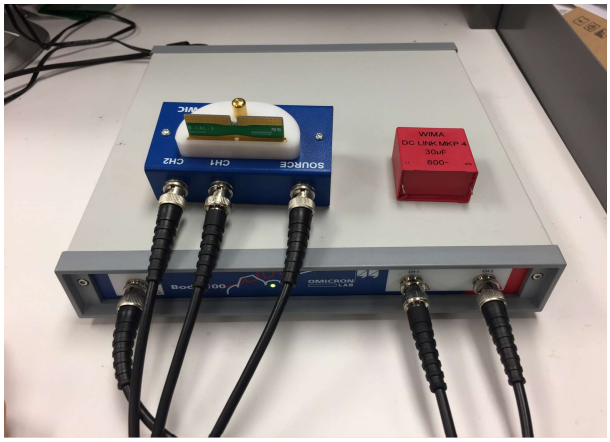
II. Measurement by Using the Commercial Fixture Adapter

To validate the accuracy of custom fixture designs, a leaded 800V 30 µF capacitor DCP4L053007HD4KSSD from WIMA is selected as a DUT, whose parasitic inductance was measured by using commercial adapters and custom fixture adapters. Two off-the-shelf fixtures were used, i.e., a B-WIC (1 Hz - 50 MHz) with Bode 100 (1 Hz - 40 MHz), as shown in Fig. 2(a) and a 16047E (up to 120 MHz) with impedance analyzer E4990A (20 Hz - 30 MHz), as shown in Fig. 2(b).

The measured DUT parasitic inductance, Ls, at 10MHz, using different methods are summarized in Table I. It should be noted that before the measurement, standard open/short/load and open/short calibrations [8] have been completed for B-WIC and 16047E, respectively.

Table I. Measurement Results by Different Methods

Fixture adapter	Ls (nH) @ 10MHz
B-WIC (commercial)	27.006
16047E(commercial)	28.027
Method 1 (customized)	29.242
Method 2 (customized)	25.183
Method 3 (customized)	28.257



(a)

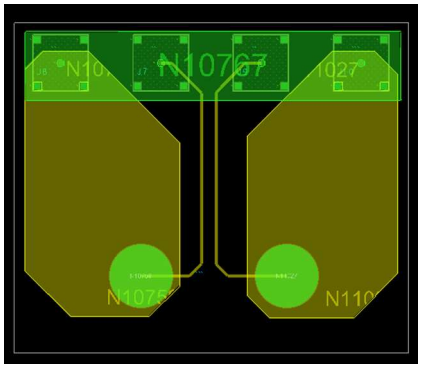
(b)

Fig. 2. Setup for commercial fixture adapters with impedance analyzers (a) B-WIC with Bode 100 (b) 16047E with E4990A.

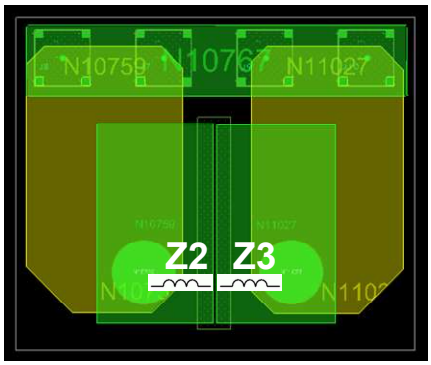
III. Design Approach for the Custom Fixture Adapter Boards

In this section, three fixture design methods are presented for four-terminal (4T) sensing impedance analyzer E4990A. The 4T sensing approach, known as Kelvin sensing [8], uses separate pairs of the current-carrying and the voltage-sensing electrodes to enhance the accuracy compared to the two-terminal (2T) sensing methods. Therefore, the customized fixtures all have four BNC connecters to interface with E4990A, while the inner two ports are for voltage measuring named sense, the outer two ports are for current measuring named force. A pair of sense traces are independent with force traces, such that they do not induce the voltage drop across the force leads or contacts. Since almost no current flows to the measuring instrument, the voltage drop in the sense leads is negligible.

The PCB layouts of three fixture adapters are shown in Fig. 3. Since the impedance of DUT is very small, the current will be large; all force traces use a large gauge to avoid overheating. The traces for the force and sense in Method 2 are the same, while force and sense traces are separated from each other in Methods 1 and 3. In Method 3, the copper layer and solder mask layer are placed on top, which can help the short/load calibration, while in Method 1, the short calibration can be accomplished by using a copper bar, and it is hard to provide load calibration.



(a)



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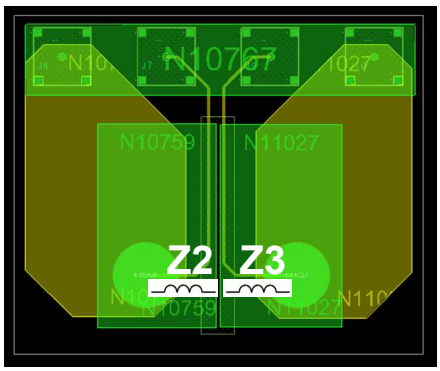


(c)

Fig. 3. PCB layout for three customized fixture designs (a) Method 1 (b) Method 2 (c) Method 3.

Instead of using the BNC cables to connect the fixture board to the impedance analyzer, four L-shape BNC plugs are utilized to mitigate their impact to the measurement. The test setup is shown in Fig. 4, and the measurement results are summarized as part of the Table I. As shown in Fig. 4(a), a copper bar is used in Method 1 for the short calibration. It should be noted the impedance of the copper bar itself, Z1, should be considered and compensated. For Methods 2 and 3, 0 Ω and 100 Ω SMD resistors are soldered for short/load calibration, respectively. It should be noted that the impedance of the green top traces Z2 and Z3 in these two methods should be considered and compensated.

(a)

(b)

(c)

Fig. 4. Test setups for (a) Method 1with an external copper bar connected for the short calibration, (b) Method 2 or 3 and (c) zoomed-in view for Method 3.

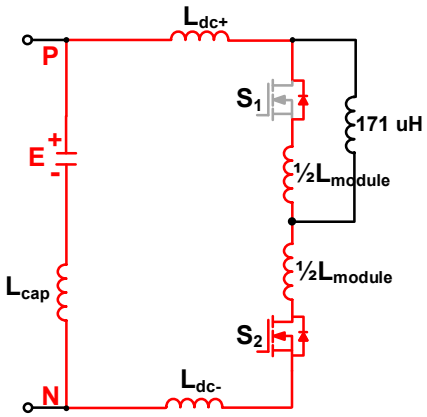
As can be seen from Table I, the Ls measured using Method 2 is much lower than others, due to the force and sense sharing the same traces, which violates the rules for Kelvin sensing. At the same time, due to the lack of load calibration, the error of Method 1 is greater than method 3. From the comparisons among these three custom fixture designs, several

considerations for the fixture adapter design are summarized as follows.

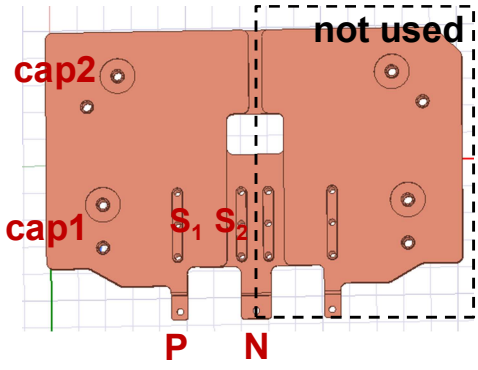
1) The force and sense traces should be separated, otherwise, its performance would be similar to the 2T sensing.
2) Recommend to use a large gauge for force trace and small gauge for sense trace.
3) Method 1 and Method 3 has higher accuracy with an error less than 5% compared to the commercial fixtures.
4) It is preferred to use Method 3 since it performs all the open/short/load calibrations.

IV. Experimental Validations

A single-phase HB inverter is used to verify the accuracy of proposed fixture design Method 3, which consists of two 1500V 195 µF WIMA dc-link capacitors DCP6S06195E000 in parallel, a laminated copper busbar and a 1.2 kV SiC HB power module CAS325M12HM2 from Wolfspeed. The schematic of the DPT is shown in Fig. 5(a), where the CCL inductance includes the stray inductances of dc-link capacitors, HB module, and busbar. The layout of the busbar was originally designed to connect two HB modules in series, as shown in Fig. 5(b). In the DPT test, only one HB is connected to the busbar. The setup for impedance measurement is shown in Fig. 5(c), where the capacitors and busbar are connected together as the DUT. The fixture adapter was designed based on Method 3. All open/short/load calibrations were completed before measurement. The result indicates that the summation of



(a)



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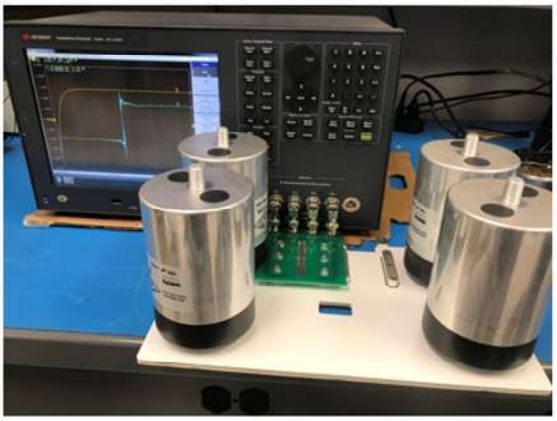


(c)

Fig. 5. HB inverter (a) schematic of its DPT (b) its bus bar layout (c) setup for its impedance measurement (bus bar + dc-link capacitors).

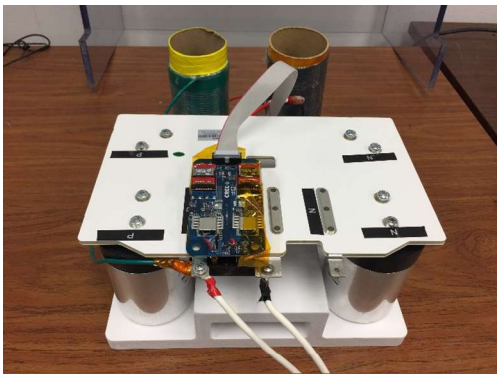
Lcap, Ldc+ and Ldc- equal 18.81 nH at 20MHz, where Lcap is the parasitic inductance in dc-link capacitors, and Ldc+, Ldc- represent the parasitic inductance in dc+ and dc- layers of the bus bar, respectively, as shown in Fig. 5(a).

DPT is widely used to evaluate the performance of the power device, and the CCL inductance can be calculated by the resonant frequency from equation (1).

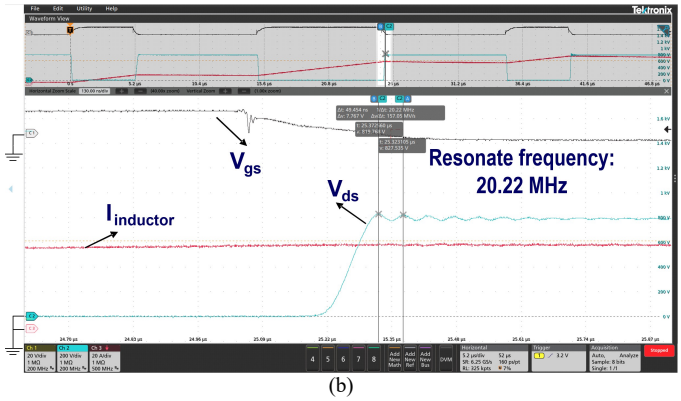
$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

where L is the CCL inductance, as the summation of Lcap, Ldc+, Ldc- and Lmodule; Lmodule is the internal parasitic inductance of the HB module. C is the Coss of the switching device and equals 2.578 nF within the module used in this work.

The DPT setup is shown in Fig. 6(a). The load used for DPT is two series-connected air-core inductors with a total inductance of 171 µH. To drive the module, a dual-channel differential isolated gate diver from Wolfspeed is used. DC bus is 800 V. Gate pulses are applied to S_2, and the anti-parallel diode of S_1 is the freewheeling diode. Drain-source and gate-source voltage are measured by differential probes THDP0200. Inductor current is measured by PEM 30 MHz Rogowski coil.



(a)



(b)

Fig. 6. Half-bridge inverter DPT (a) setup (b) turn-off waveforms.

From the V_{ds} waveform during the turn-off shown in Fig. 6(b), it can be seen that the resonant frequency is 20.22 MHz. Then it can be calculated using equation (1) and C value from module's datasheet, L equals 24 nH according to the DPT result. Lmodule can be obtained from module's datasheet, which is 5 nH. Then from impedance measurement result, L = 18.81 + 5 = 23.81 nH, with only 0.79% difference comparing from the DPT result. Therefore, the accuracy of fixture design Method 3 can be verified.

V. CONCLUSION

This paper presents the three different fixture adapter design methods for 4T impedance analyzers. The measurement results are also compared with the commercial ones. Based on their parasitic inductance measurement results, the design considerations and guidance are summarized. Finally, the DPT experimental results have verified that the proposed fixture board design Method 3 is accurate enough.

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