Parasitic Inductances Extraction for SiC Power Modules Using An Enhanced Two-Port S-Parameter Approach

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***Abstract*—Parasitic inductance of power modules is one nonnegligible part of inductance on converters' current commutation loop (CCL). Larger CCL inductance leads to higher switching oscillation, voltage overshoot, electromagnetic interference (EMI), and larger power losses. This paper uses two-port scattering (S) parameter measurement to extract the parasitic inductance of the power module. The innovation of this paper is that it considered the impact of mutual inductance and fixture printed circuit board (PCB) when using S-parameter approach. Accurate internal parasitic inductance values can be obtained by logic analysis, no matter used in a traditional two-level (2-L) inverter or three-level (3-L) T-type inverter. And it provides the guidance to build the fixture PCB board to connecting vector network analyzer (VNA) and the module, which has not been discussed in the existing literature. The approach is experimentally validated by a commercial 1200V SiC half-bridge power module.**

Keywords—parasitic inductance; scattering parameter, SiC MOSFET; two-port network.

I. INTRODUCTION

To increase the efficiency of power electronics converters and improve the system power density, increasing the switching frequency is the trend nowadays. Wide band gap (WBG) devices such as SiC and GaN devices are a good solution to replace the traditional silicon (Si) IGBT due to the high temperature, high voltage operation possibility, and especially the high switching frequency characteristic [1]-[4]. At the same time, high *di/dt* and *dv/dt* bring negative effects due to the existence of parasitic inductance. Larger CCL inductance leads to higher switching oscillation, voltage overshoot, EMI, and larger power losses. [5]-[7] For instance, drain-to-source overshoot of switching position $V_{ds}=L\cdot di/dt$, where L is the CCL inductance. High overshoot will avoid the switching frequency increases to the target. In order to model and reduce the negative effect at the early design stage, the parasitic inductance of CCL must be accurately characterized. The parasitic inductance in a CCL may come from 1) the parasitic inductance of the DC link capacitors; 2) the stray inductance of the semiconductor discrete devices or power modules; 3) the stray inductance on the bus bars connecting the capacitors and the power devices. The parasitic inductance from the discrete semiconductor devices or power modules is nonnegligible, especially when the topology is complicated and includes many power devices. In addition, when a new kind of power device packaging is built, it is necessary to measure the internal parasitic inductance before its delivery and application. Therefore, it is critical to apply a suitable method to obtain the parasitic inductance from the semiconductor discrete devices and power modules. Discrete devices and power modules can both be regarded as a two-port network. The difference is that for discrete devices, the three terminals are drain, source, and gate pins. In contrast, for Half-bridge (HB) power modules, the parasitic inductance on the pin connections of bus positive, negative, and output are our focus, which will be discussed in Section II. HB power module is the device under test (DUT) in this work, and it is simplified to a three-terminal equivalent circuit model.

There are several ways to obtain the parasitic inductance of the power module, which can be classified into two groups. One is the simulation method, such as the finite element analysis (FEA) or partial element equivalent circuit (PEEC) using numerical software simulation tools. [12]-[14] The other one is the measurement-based method, such as directly measured by time domain reflectometry (TDR) and impedance measurement in the frequency domain. The simulation methods calculate inductance and capacitance based on the objects' geometry and material information by solving Maxwell's equation. However, the two simulation methods usually take a long time due to the complex internal structure of power modules and may suffer from the poor convergence problem. More importantly, it is not easy to obtain the detailed internal design file of power module from the manufactures. The principle of TDR method is transmission line theory, and the parasitic inductance is extracted from the reflected signal with respect to delay time [15], [16]. TDR is relatively complicated and needs the modeling of differential interconnects. Comparatively speaking, the impedance measurement in the frequency domain is more accurate and applicable by using an impedance analyzer or a vector network analyzer (VNA).

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Impedance analyzer approach is commonly used in one-port structure components' measurement [17]-[19]. But when it comes to HB power module with a two-port network, the result will couple with errors from the other floating terminal. [20] S-parameter measurement using VNA is mainly used in microwave and radio frequency (RF) applications [21], [22]. It can extract the small-signal equivalent circuit and intrinsic elements of microwave field effect transistors. The impedance between the tested ports can be calculated by transferring S-parameter to Z-parameter through a two-port network analysis. After analyzing of Z-parameter network, accurate values of the internal parasitic inductance can be obtained. The S-parameter measurement approach was tried on Si power metal-oxide semiconductor field-effect transistor (MOSFET) in [23], but the iterative process made it complex and lost accuracy. In [24], a simple indirect two-port network measurement method and computation are used to the characterization of discrete power MOSFET. Later, the authors extended it into the measurement of SiC MOSFET power modules [25]-[27]. [28], [29] used a similar but direct method to extract the parasitic inductance of HB module, avoiding the error from indirect computation, at the same time the inductance from AC output power terminal was also measured. However, the previous researches all ignore the existence of mutual inductance. Nevertheless, the mutual inductance generated during the measurement procedure has never been discussed. Besides the discussion of mutual inductance, this paper also provides detailed fixture board design guidance, which has never been mentioned before. Additionally, this paper clarifies the parasitic inductance measurement procedure for HB power module using in both 2-L and 3-L T-type inverter.

The two-port S-parameter measurement approach is accurate and feasible to extract parasitic inductance of semiconductors. The equivalent circuit simplification of HB power module is presented in Section II. The principle of S-parameter based measurement is described in Section III, which including both self-inductance and mutual-inductance. In Section IV, the theoretical analysis is evaluated by a Wolfspeed HB SiC MOSFET power module using VNA. Because the inductance being measured is so small, at the nH level, it is critical to make a fixture board that does not introduce errors. Two design methods are compared in this Section, and the design guidance can be summarized from it.

II. Equivalent Circuit of a HB Power Module

As shown in Fig.1 (a), there are seven terminals in a typical half-bridge power module, that is drain of up switch position (V+), source of up switch position/drain of down switch position (Mid), source of down switch position (V–), gate of up switch position (G_H), Kelvin source of up switch position (S_H), gate of down switch position (G_L), and Kelvin source of down switch position (S_L). C_{gd}, C_{gs}, C_{ds} are three critical parasitic capacitances between gate-drain, gate-source, and drain-source. L_{ss} is the common source inductance, which is very small with Kelvin source structure. L_{g_in}, L_{s_in}, and R_{g_in} are internal parasitic inductance and resistance in gate loop. Since the voltage overshoot and switching oscillation on Vds are caused by output capacitance C_{oss} (C_{oss} = C_{gd}+C_{ds}) and power loop inductance [9], [10], parasitic components in gate loop is not the focus of this paper. Hence, the gate loop parasitic components are not indicated in the simplified model. Fig. 1(b) shows the simplified three-terminal equivalent circuit model of a typical HB power module with gate state OFF. L_H and L_L represent the lumped parasitic inductance in high and low internal path. Similarly, the simplified three-terminal equivalent circuit model with ON state is shown in Fig. 1(c). C_{oss} is bypassed, and R_{on}, the on-resistance is included in this model at this time. The S-parameter measurement can be conducted under both ON and OFF state, and the final inductance results are almost the same. Under OFF state, the Z-parameter network will display a typical RLC resonant circuit. The target parasitic inductance can be obtained by reading the slope of high-frequency range impedance. Under ON state, the Z-parameter network will display a typical RL circuit. The parasitic inductance can be obtained by reading the impedance at the target frequency. The analysis and tests in this paper are all under OFF state.

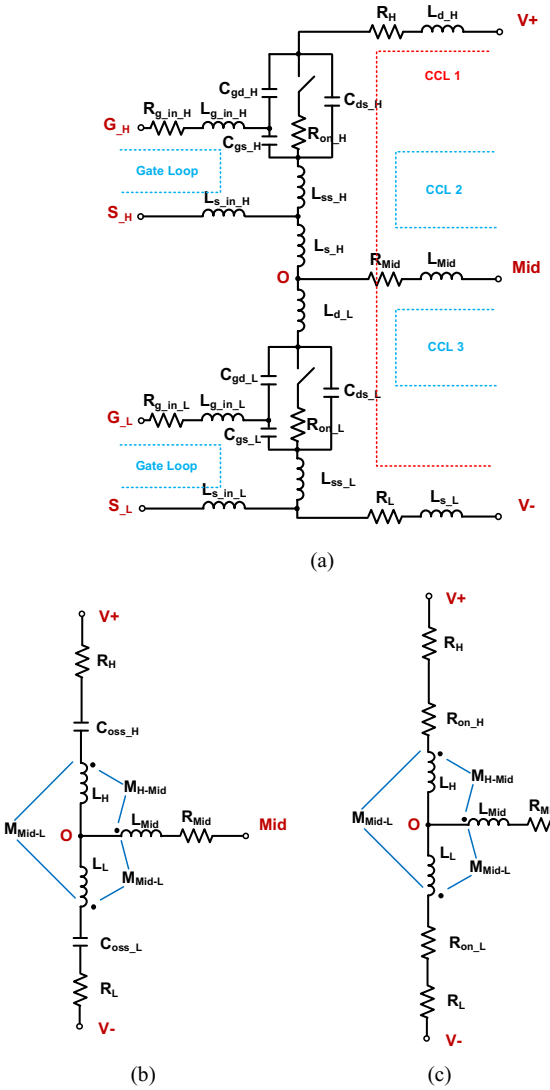


Fig. 1. The equivalent circuit models of a typical HB module: (a) the detailed model without considering the mutual inductance; (b) in the OFF state considering mutual inductance and (c) in the ON state considering mutual inductance.

When HB power module is applied in traditional 2-L inverters, the current commutation power loop is shown in red dash line in Fig. 1(a), named power loop1. At this time, only L_H and L_L participate in the loop inductance. Because current flows through up and down path at the same time, the mutual inductance will exist. The homonymous terminals of an inductor depend on specific internal power module structures. Here, the homonymous terminals of L_H, L_L, and L_{Mid} are assumed, as shown in Fig. 1(b) and (c). $M_{H\text{-}L}$ represents the mutual inductance between L_H and L_L. Because there is not high-frequency current flowing through Mid terminal, Mid terminal will not generate mutual inductance on high and low path.

When HB power module is applied in 3-L T-type inverters, there are two separate current commutation power loops, shown in blue dash line in Fig. 1(a), named power loop2 and power loop3 [11], [12]. Because of the operation principle of the T-type inverter, high and low switch position cannot participate in the power loop at the same time. So only L_H and L_{Mid}, or L_L and L_{Mid} consist the loop inductance. $M_{H\text{-}Mid}$ represents the mutual inductance between L_H and L_{Mid}, and $M_{Mid\text{-}L}$ represents the mutual inductance between L_{Mid} and L_L.

In summary, the internal parasitic inductance of HB power module applied in 2-L inverter is:

$$L_{module\_CCL1} = L_H + L_L - 2 \cdot M_{H-L} \tag{1}$$

The internal parasitic inductance of Hb power module applied in 3-L T-type inverter is:

$$L_{module\_CCL2} = L_H + L_{Mid} + 2 \cdot M_{H-Mid} \tag{2}$$

$$L_{module\_CCL3} = L_L + L_{Mid} + 2 \cdot M_{Mid-L} \tag{3}$$

III. Practical Issues of Module Inductance

Fig. 2 shows the two-port S-parameter measurement setup used in this work, where the device under test (DUT) is a SiC power module. The VNA measures S-parameters of the DUT, i.e., S11, S21, S12, and S22. According to [31], the Z-parameters can be calculated by these measured S-parameters as

$$Z_{11} = Z_0 \left[\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \right]$$

$$Z_{21} = Z_0 \left[\frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \right]$$

$$Z_{12} = Z_0 \left[\frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \right]$$

$$Z_{22} = Z_0 \left[\frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \right]$$

where the characteristic impedance $Z_0 = 50\ \Omega$.

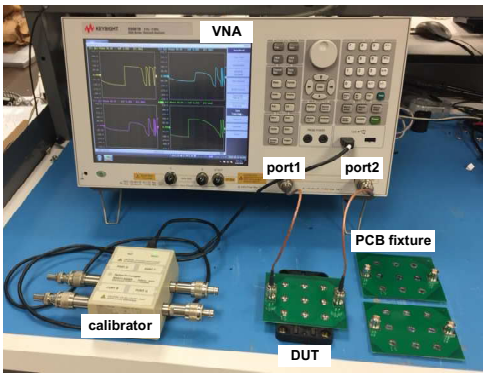


Fig. 2. The setup for 2-port S-parameter measurement.

The Z-parameter network is a typical RLC circuit, and parasitic inductances can be extracted by measuring the impedance in the high-frequency range.

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = R_H + R_{Mid} + j\omega \cdot (L_H + L_{Mid}) + \frac{1}{j\omega \cdot C_{oss\_H}} + Z_{T1} + Z_{T4} \tag{4}$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = R_{Mid} + j\omega \cdot L_{Mid} \tag{5}$$

$$Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = R_L + R_{Mid} + j\omega \cdot (L_L + L_{Mid}) + \frac{1}{j\omega \cdot C_{oss\_L}} + Z_{T2} + Z_{T5} \tag{6}$$

$$Z_{12} = Z_{21} = R_{Mid} + j\omega \cdot (L_{Mid} + M_{H-L} + M_{Mid-L} + M_{H-Mid}) \tag{7}$$

$$Z_{12} = Z_{21} = R_H + j\omega \cdot (L_H + M_{H-Mid} - M_{Mid-L} - M_{H-L}) + (j\omega \cdot C_{oss\_H})^{-1} \tag{8}$$

$$Z_{12} = Z_{21} = R_L + j\omega \cdot (L_L + M_{Mid-L} - M_{H-Mid} - M_{H-L}) + (j\omega \cdot C_{oss\_L})^{-1} \tag{9}$$

A. *Impact of the Fixture Board*

As shown in Fig. 2, the VNA has two BNC ports, which are connected with the two BNC ports on the fixture board. The traces T1 and T2 connecting module terminals V+ and V- to the positive terminals of BNC1 and BNC2, respectively. Through traces T3, T4, and T5, the terminal Mid of the module shares the ground with the ground terminals of BNC1 and BNC2.

When mutual inductance is not considered, the Z-parameters model can be described as follows [31], and there are two methods that can be applied. Method I: 1. Simulate the trace impedances, i.e., Z_{T1} to Z_{T5} using FEA software; 2. Measure the impedance of DUT using setup-1, as shown in Fig. 3(a); 3. Calculate L_{Mid} using Z_{21} or Z_{12}; 4. Calculate L_H and L_L using equations (4), (6), and the simulated Z_{T1} to Z_{T5}. Method II: 1. Use a fixture board connecting terminal Mid to ground, i.e., setup-1 shown in Fig. 3(a); perform the S-parameter measurement for DUT; calculate L_{Mid} using Z_{21} or Z_{12}. 2. Build a fixture board connecting terminal V+ to GND, shown as setup-2 in Fig 3(b); measure the DUT by VNA; Calculate L_H through Z_{21} or Z_{12}. 3. Build a fixture board

connecting terminal V- to GND, shown as setup-3 in Fig 3(c); measure the DUT by VNA; Calculate L_L through Z_{21} or Z_{12}.

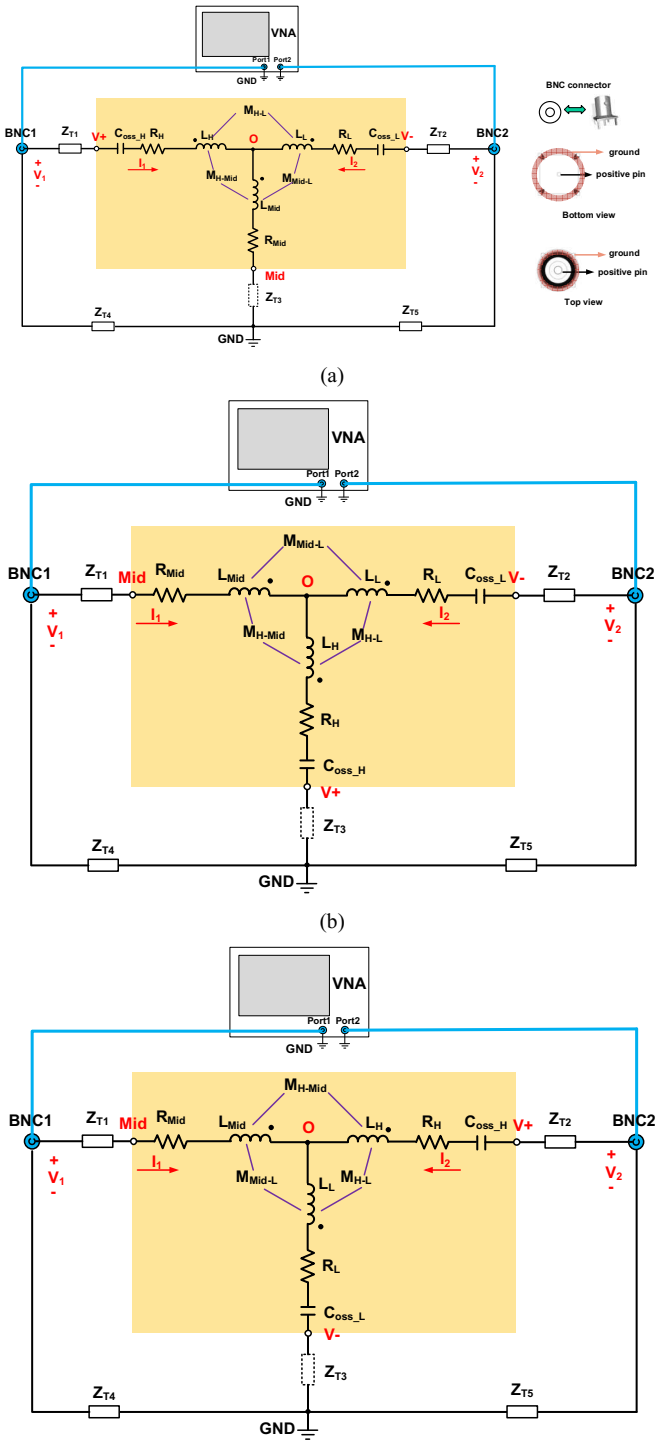


Fig. 3. The 2-port S-parameter measurement equivalent circuits: (a) setup1 (terminal Mid connecting to GND), (b) setup2 (terminal V+ connecting to GND) and (c) setup3 (terminal V- connecting to GND).

The major difference is that the Method I is a hybrid approach, which requires only one fixture board but needs additional simulations, while Method II requires three fixture boards with 3 separate measurements but doesn't require additional simulations. Two of the inductances extracted by Method I are indirect; thus, the accuracy can be significantly affected by the quality of FEA simulation and fixture design. Method II solely relies on the measurements, eliminating errors due to simulations. This work uses Method II, and considers all the ground loop impedances ZT3, ZT4, and ZT5 and also the mutual inductances.

B. *Impact of the Mutual Inductance*

As shown in Fig. 3, when considering the mutual inductances, Z_{12} or Z_{21} can be rewritten for all three cases, shown as (7)-(9), which are the expressions for setup-1 to 3, respectively. By calculating the reactance of the Z_{12} or Z_{21} in the high-frequency range, the extracted parasitic inductances, denoted as L^*, including both self-inductance and mutual inductances, are shown in (10)-(12).

$$L^*_{Mid} = L_{Mid} + M_{H-L} + M_{Mid-L} + M_{H-Mid} \quad (10)$$

$$L^*_{H} = L_{H} + M_{H-Mid} - M_{Mid-L} - M_{H-L} \quad (11)$$

$$L^*_{L} = L_{L} + M_{Mid-L} - M_{H-Mid} - M_{H-L} \quad (12)$$

According to (10)-(12), the CCL inductances described by equations (1)-(3) can be obtained as (13)-(15).

$$L_{module\_CCL1} = L^*_H + L^*_L \quad (13)$$

$$L_{module\_CCL2} = L^*_H + L^*_{Mid} \quad (14)$$

$$L_{module\_CCL3} = L^*_L + L^*_{Mid} \quad (15)$$

IV. Experimental Validations And Fixture Design Considerations

The two-port S-parameter measurement setup used for the experimental validation has been shown in Fig. 2, where VNA is the Keysight E5061B. The electronic calibration module N4431-60004 is used to compensate for the errors brought by the two BNC cables. The DUT is a 1.2 kV SiC HB module CAS325M12HM2 [32] from Wolfspeed, shown in Fig. 4(a).

Although the measurement Method II focuses on Z_{12} and Z_{21} to avoid the error brought by Z_{T1}, Z_{T2}, Z_{T4}, and Z_{T5}, it is still easily impacted by the existence of Z_{T3}. Z_{T3} is the impedance to the common part of BNC1 and BNC2 grounding path. Z_{T3} will be part of the Z_{12} and Z_{21}. To obtain the inductance value in the internal module, One method is to extract the inductance from Z_{T3} by FEA simulation and subtracted from the Z_{12} or Z_{21} inductance. However, it is preferred to eliminate Z_{T3} in the fixture design process.

Here, two sets of fixture designs are presented. The Design I is shown in Fig. 4(b), (c), and (d), where the terminal Mid, V+, V- grounded, respectively. The fixture design principle is quite straightforward: locate the BNC connectors close to the ungrounded branches to minimize the Z_{T1} and Z_{T2}. The yellow shaded part is grounding polygon; the purple arrow is the common current grounding path related to Z_{T3}, blue and red arrow is grounding path related to Z_{T4} and Z_{T5}, L_{T1} and L_{T2} are the trace inductance connected BNC positive pin and DUT

ungrounded branches. As it can be seen from the layout, L_{T3} inevitably exists.

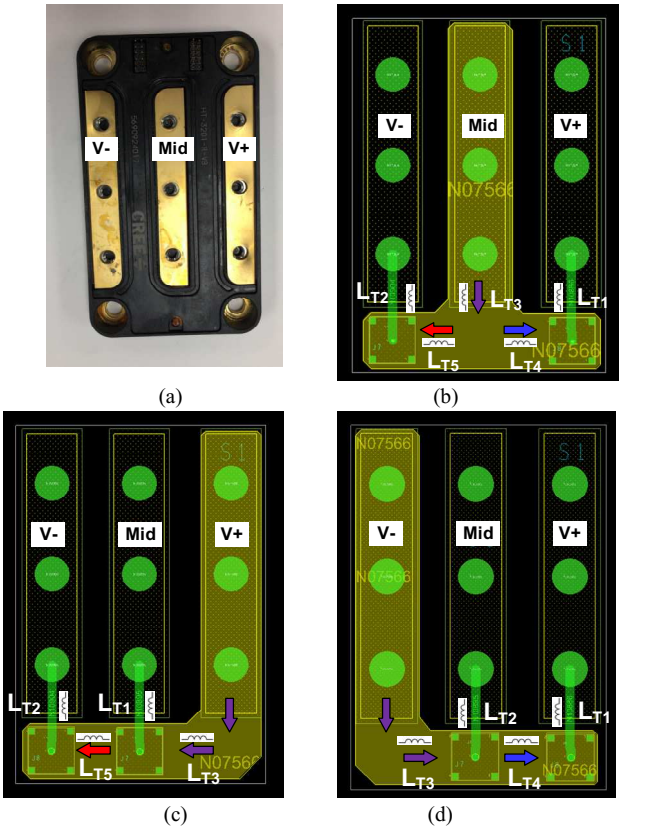
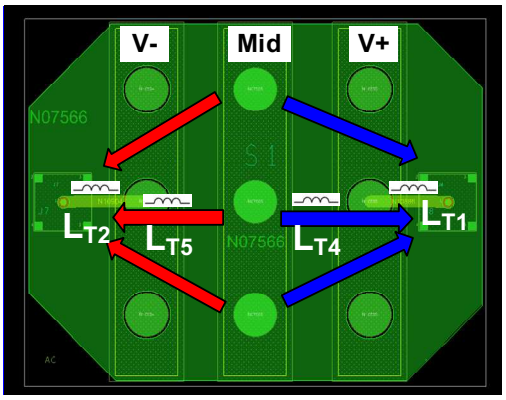


Fig. 4. (a) Half-bridge power module from Wolfspeed (b) Design I PCB layout with Mid grounded (c) Design I PCB layout with V+ grounded (d) Design I PCB layout with V- grounded.

The layouts of Design II are shown in Fig. 5(a), (b), and (c) with Mid, V+, and V- grounded, respectively. To eliminate Z_{T3}, BNC1 and BNC2 were placed symmetrically to the Mid terminal of the power module. As shown in Fig. 5, the BNC1 and BNC2 are placed on the left and right ends of the fixture boards, such that the red and blue arrows, i.e., grounding polygon T4 and T5, are always separated away from each other to eliminate the common path T3. Although the Z_{T1} and Z_{T2} may be increased significantly due to the prolonged traces, it does not affect the measurement results, since only the measured Z_{21} or Z_{12} is used in each step.



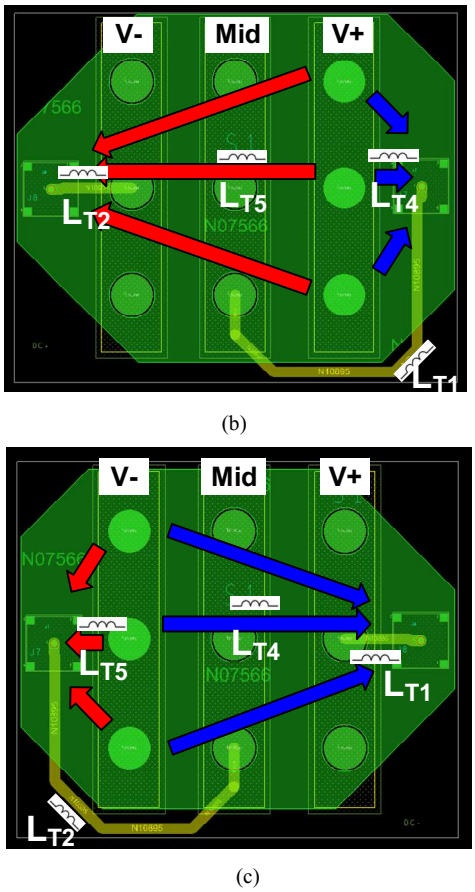
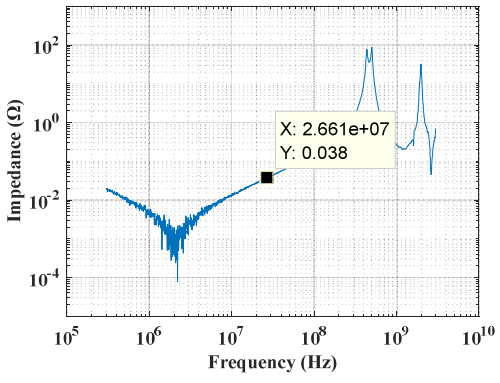
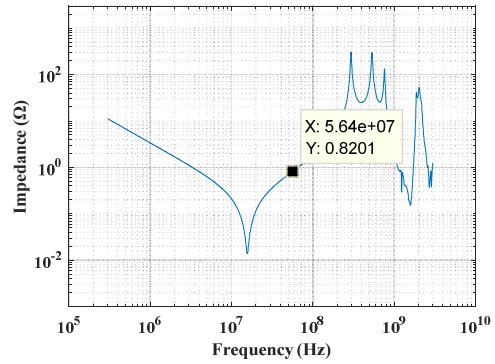


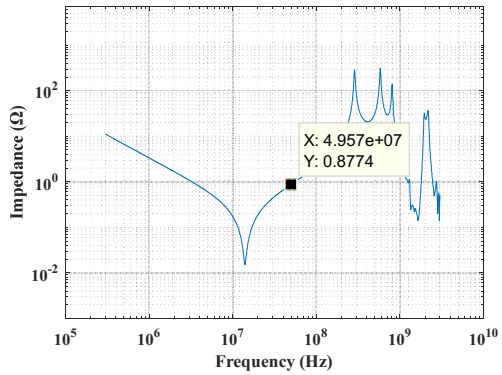
Fig. 5. Design II PCB layout (a) with Mid grounded (b) with V+ grounded (c) with V- grounded

The Design II measured impedance Z_{12} or Z_{21} versus frequency plots are shown in Fig. 6. The power module internal parasitic inductance L^*_{Mid}, L^*_H, L^*_L can be calculated and summarized in Table I. According to (13), when used in a 2-L inverter, the internal parasitic inductance of the module that contributes to the total CCL stray inductance can be determined as $L_{module\_CCL1} = L^*_H + L^*_L = 5.13$ nH. As a comparison, the inductance value of Lmodule_CCL1 provided in the datasheet [32] is 5 nH. For 3-L applications, according to (14) and (15), L_{module_CCL2} and L_{module_CCL3} are 2.54 nH and 3.05 nH, respectively.





(b)



(c)

Fig. 6. Result of impedance versus frequency with fixture Design II (a) Mid grounded (b) V+ grounded (c) V-grounded

TABLE I
INDUCTANCE MEASUREMENT RESULTS

	L^*_{Mid}	L^*_H	L^*_L
Value	0.23 nH	2.31 nH	2.82 nH

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