A Hybrid Multivector Model Predictive Control for an Inner-Interleaved Hybrid Multilevel Converter

Yufei Li, *Member*, *IEEE*, Fei Diao, *Student Member*, *IEEE*, Yue Zhao, Senior *Member, IEEE*

***Abstract*—A hybrid multivector model predictive control strategy for an inner-interleaved hybrid multilevel converter is brought forward in this work, which can enable the separation of the low- and high-frequency stages. It initiates with the use of sign patterns of the reference vector in the stationary reference frame to determine switching states of the low-frequency stage. Then, the reference vector is converted to the inner virtual space vector diagram, which is further transformed into a 120° oblique coordinate system, where the adjacent vectors are selected. Further, the current tracking is realized through the duty cycle optimization of the chosen vectors. Finally, a symmetric switching sequence, which serves as the best one for dc capacitors voltages balancing and circulating current suppression, is selected among all the switching sequences that belong to the three chosen vectors with optimal duty cycles. The proposed method reduces both current ripples and computational burden while achieving a constant equivalent switching frequency. Comprehensive experimental results performed on an all silicon-carbide prototype verify the effectiveness of the proposed control.**

***Index Terms*—Hybrid multilevel converter (HMC), model predictive control (MPC), optimal duty cycle.**

NOMENCLATURE

j	Three phases, $j \in \{a, b, c\}$.
x	Power switch index, $x \in \{1, 2, \ldots, 10\}$.
R, L	Load resistance and inductance.
U_{dc}	External dc-source voltage.
u_{dc_1}, u_{dc_2}	DC-link capacitor voltages and deviation.
Δu_{dc}	Deviation of dc-link capacitor voltages.
L_0, L_{eq}	Interleaved and equivalent inductance.
$\boldsymbol{v}$, $\boldsymbol{i}$	Converter voltage and current vectors.
C, C_1	DC-link and flying capacitance.
u_{dc_j1}, i_{fj}	Flying capacitors voltages and currents.
i_{dc_1}, i_{dc_2}	Currents of the dc-link capacitors.
i_{oj}, i_o	Three-phase and total neutral point currents.
i_j, i_{cj}	Converter phase and circulating currents.
i_{j1}, i_{j2}	Currents of the interleaved legs.
u_{jo1}, u_{jo2}	Interleaved legs voltages in each phase.
v_j	Equivalent three-phase output voltages.
M_{jx}	Power switches in each phase.
S_j, S_{jx}	Switching states of phase j and power switches.
d_{jx}	Duty cycles of the power switches.
$y(k)$, $y(k+1)$	Variable y at k, $k+1$ time instant.
$\boldsymbol{v}^*$, $\boldsymbol{v}_{abc}{}^*$	Reference vectors in $\alpha\beta$- and abc-coordinate.
$\boldsymbol{v}_v{}^*$	Reference in the virtual space vector diagram.
$\boldsymbol{V}_n$, $\boldsymbol{S}_n$	Shift vector and state, $n \in \{1, 2, \ldots, 6\}$.
$\boldsymbol{v}_{v1}{}^*$, θ_{v1}	Virtual reference vector and its angle in Sector 1 of the virtual space vector diagram.
$\boldsymbol{V}_k$, $\boldsymbol{S}_k$	Adjacent vectors and their slops, $k \in \{1, 2, 3\}$.
t_k,	Dwell time of the three chosen vectors.
d_k	Optimal duty cycles of the three chose vectors.
T_s	Control or sampling period
$[V_{vg1}\ V_{vh1}]^{\mathrm{T}}$	Virtual reference vector in the 120° gh-frame.
J_{dc}, J_{cir}	DC voltages and circulating currents cost function.
J, J_{min}	Total cost function and minimum cost function.
λ_1, λ_2	Weighting factors.
S_{jx_i}	The ith switching state of M_{jx}, $i \in \{1, 2, 3, 4\}$.

This work was supported in part by the U.S. National Science Foundation (NSF) under CAREER Award ECCS-1751506. *(Corresponding author: Yufei Li.)*

Yufei Li is with the Department of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment, Princeton University, Princeton, NJ 08544 USA (e-mail: yl5385@princeton.edu).

Fei Diao and Yue Zhao are with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA (feidiao@uark.edu; yuezhao@uark.edu).

I. INTRODUCTION

HYBRID multilevel converters (HMCs) [1] have been ever-increasingly injecting vitality to the multilevel converter family [2] over the past few decades, which are adopted in a wide range of applications [3]-[5]. Compared with multilevel converters constructed with a single type of power electronic building block (PEBB) [6], the HMC has multiple advantages due to the integration of multiple PEBBs into the topology [7]. In particular, the inner-interleaved HMCs (IHMCs), which contains inner-interleaved structures, feature additional benefits such as increased output voltage levels, reduced device current stress, enhanced modularity [8], etc. In spite of inarguable advantages, the combination of various types of PEBBs complicates the control of HMCs, especially the IHMCs, which therefore, requires enhanced control strategies to deal with multiple control objectives, e.g., capacitor voltages balancing, current quality improvement, and circulating current mitigation, etc.

Heretofore, the vast majority of research effort on the control of the HMCs concentrates upon the phase-disposition (PD) pulse width modulation (PWM) [9], the phase-shifted (PS) PWM [2], [10], and the space vector modulation (SVM) [3], [11], which, although mature, suffer from inherent weaknesses, to name a few: the difficulty to balance dc capacitor voltages and to tune controller parameters, and the cross-coupling among co-existing multiple control loops [12]. In addition, due to the increased complexity of the IHMC in both circuit-level and control-level, achieving capacitor voltage balancing and other control objectives may become even harder. In particular, an SVM for a five-level diode-clamped-converter is proposed in [13], which innovatively

uses the minimum energy concept, searching for the lowest derivative of the energy coefficient, effectively achieves the current tracking and dc voltage balancing at the same time. However, this SVM method is specifically designed for this five-level diode-clamped-converter, where the minimization of the dc capacitor energy is very similar to the cost function minimization process of the model predictive control (MPC) [14], which on the other hand, is born for dealing with multi-objective controls [15], [16], and therefore, perfectly fits the needs of HMCs. Nevertheless, it faces two major challenges when applied to HMCs. On one hand, assessing the massive switching states brought by the multilevel topology significantly burdens the state-of-the-art digital processors [17]. On the other hand, applying only one switching state over each control period results in relatively large output current ripples and a variable equivalent switching frequency, which further complicates the filter design [18].

Meanwhile, a broad range of research has been conducted in an effort to cope with these issues. For instance, the dc capacitors voltages sorting method is adopted to mitigate the calculation burden in modular multilevel converters [19] and cascaded H-bridge converters [20]. In [21], the proposed indirect MPC for the MMC uses the field programmable gate array (FPGA) to conduct the sorting algorithm, while the switching control actions are further simplified through consideration of only neighboring index values with respect to their previously applied values, which significantly reduces he computational burden. In [18], a simplified MPC scheme is proposed to theoretically increase the sampling rate up to 60 kHz, which can fully exploit the benefits of the wide-bandgap (WBG) power devices. In addition, there are also extensive literatures focusing on the steady-state performance improvement for the MPC. A long-horizon MPC is introduced in [22], which however, faces tremendous calculation burden when increasing the prediction horizon. The authors hence bring forward a modified sphere decoding algorithm to dramatically reduce the calculation burden. Whereas, the long-horizon MPC still remains a mathematically complicated approach [15]. In [23], the sampling cycle is divided into N parts, enabling insertion of N voltage vectors within each control period, such that the current tracking can be improved. However, the performance of this method depends largely on the circuit parameters. A novel MPC method that combines the reference trajectory tracking and its derivative trajectory tracking together is presented in [24] to reduce the voltage total harmonic distortion (THD). In addition, the virtual vectors-based MPC method has also been widely studied to improve the steady-state performance [7], [25]-[27], but is associated with several drawbacks. First, when dividing the control cycle, the pulse pattern is presumably asymmetric [26], which results in unnecessary switching actions. Second, the design of the virtual vectors group seems to vary greatly on a case-by-case basis [27]. Third, synthesis of the virtual vectors can result in higher switching frequency, and thus, higher power losses, unless the WBG devices are used [7].

In addition, there is also research attempting to design MPC with a constant equivalent switching frequency. In [28], the harmonics of the output current are shaped into concentrated groups by a notch filter, and in [29], the harmonics are re-shaped by a period management method. Nonetheless, these re-shaped harmonics are limited to the frequency barrier set by the sampling frequency, that is, half of the sampling frequency. In other words, the modification of the harmonics can only be conducted with the half sampling frequency range. When it comes to HMCs, the sampling frequency is very hard to be too high to provide enough bandwidth for the regulations of current harmonics. Moreover, the output current may have obvious oscillations at the regulated frequency when applying these methods [28]. Besides, the concept of duty cycle optimization is proposed in [30], then the three-vector-based MPC [31] for motor drives is brought forward recently, which also works well in achieving both satisfactory current tracking and the constant switching frequency. However, the abovementioned approaches cannot be directly employed to HMCs because of the enormous number of voltage vectors to be evaluated and the difficulty in shaping symmetric switching patterns. As such, there is a research gap.

This article proposes a hybrid multivector MPC (HMV-MPC) for a nine-level IHMC, which overcomes inherent obstacles of the conventional MPC (C-MPC). The proposed method can enable the separation of the low-frequency stage (LFS) and high-frequency stage (HFS) in the IHMC and reduce both the output current THD and computational burden while achieving a constant equivalent switching frequency. The remainder of this article is organized as follows. Section II analyzes the IHMC from the topological point of view. Section III elaborates the proposed HMV-MPC from LFS to HFS control. Section IV validates the proposed method by experimental results on an all silicon-carbide (SiC) prototype. Finally, Section VI draws the conclusion of this article.

II. Circuit Description

Fig. 1 illustrates the configuration of the nine-level IHMC, where $u_{dc\_1} = u_{dc\_2} = U_{dc}/2$ and $u_{dc\_j1} = U_{dc}/4$. Table I lists all the switching states, where it can be seen that M_{j1}-M_{j4} can work at fundamental switching frequency. The IHMC is thereby split into an LFS and HFS, respectively, as highlighted in Fig.1.

A. Comparison and Discussion

To better understand the advantages of the nine-level IHMC, comparisons between other nine-level multilevel topologies and the nine-level IHMC are hereby conducted. Fig. 2 demonstrates a wide range of nine-level multilevel topologies, covering the flying capacitor converter (FCC) [32], the hybrid MMC (HMMC) [1], the nine-level ANPC (ANPC-9L) [33], the five-level ANPC cascaded with H-bridge (ANPC-5L-H) [34], the stacked T-type converter [35], the T-type ANPC converter (T-ANPC) [9], the flying capacitor (FC) internal parallel converter (IPC) (FC-IPC) [8], and the nine-level

IHMC in this work. Table II compares the above nine-level topologies in terms of LFS, HFS, and FCs count. As shown, the nine-level IHMC in this work has the lowest device count and lowest capacitor energy storage at the same time. Specifically, it is noteworthy that compared with the FC-IPC in [8], the nine-level IHMC in this work has two fewer power devices when generating a nine-level voltage. Therefore, voltage stresses across power devices of the HFS and the current stresses of M_{j7}-M_{j9} are reduced, these facts can enable the choice of using lower-cost devices with lower-voltage or -current ratings.

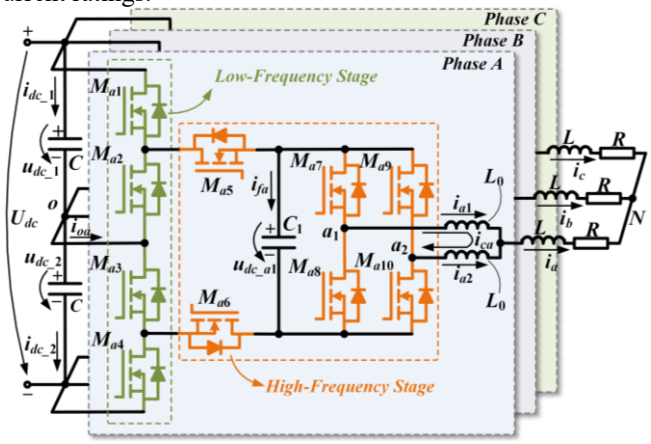

Fig. 1. The nine-level IHMC topology.

TABLE I
SWITCHING STATES OF THE NINE-LEVEL IHMC

Switching States S_j	LFS S_{j1} ($\overline{S}_{j2}$)	LFS S_{j3} ($\overline{S}_{j4}$)	HFS S_{j5} ($\overline{S}_{j6}$)	HFS S_{j7} ($\overline{S}_{j8}$)	HFS S_{j9} ($\overline{S}_{j10}$)	u_{jo1}	u_{jo2}	i_{oj}	i_{fj}
8 (U_{dc}/2)	1	1	1	1	1	U_{dc}/2	U_{dc}/2	0	0
7 (3U_{dc}/8)	1	1	1	1	0	U_{dc}/2	U_{dc}/4	0	i_{j2}
	1	1	1	0	1	U_{dc}/4	U_{dc}/2	0	i_{j1}
6 (U_{dc}/4)	1	1	1	0	0	U_{dc}/4	U_{dc}/4	0	i_j
	1	1	0	1	1	U_{dc}/4	U_{dc}/4	i_j	$-i_j$
5 (U_{dc}/8)	1	1	0	1	0	U_{dc}/4	0	i_j	$-i_{j1}$
	1	1	0	0	1	0	U_{dc}/4	i_j	$-i_{j2}$
4 (0)	1	1	0	0	0	0	0	i_j	0
	0	0	1	1	1	0	0	i_j	0
3 ($-U_{dc}$/8)	0	0	1	1	0	0	$-U_{dc}$/4	i_j	i_{j2}
	0	0	1	0	1	$-U_{dc}$/4	0	i_j	i_{j1}
2 ($-U_{dc}$/4)	0	0	1	0	0	$-U_{dc}$/4	$-U_{dc}$/4	i_j	i_j
	0	0	0	1	1	$-U_{dc}$/4	$-U_{dc}$/4	0	$-i_j$
1 ($-3U_{dc}$/8)	0	0	0	1	0	$-U_{dc}$/4	$-U_{dc}$/2	0	$-i_{j1}$
	0	0	0	0	1	$-U_{dc}$/2	$-U_{dc}$/4	0	$-i_{j2}$
0 ($-U_{dc}$/2)	0	0	0	0	0	$-U_{dc}$/2	$-U_{dc}$/2	0	0

B. Modeling and Analysis

1) System Model: The current model can be given by

$$\boldsymbol{v} = L_{eq}\frac{d\boldsymbol{i}}{dt} + \boldsymbol{i}R \tag{1}$$

where $\boldsymbol{v} = [v_\alpha\ v_\beta]^{\mathrm{T}}$, $\boldsymbol{i} = [i_\alpha\ i_\beta]^{\mathrm{T}}$, and $L_{eq} = L_0/2+L$. Also, the equivalent output voltage $v_j = (u_{jo1}+u_{jo2})/2$ [36].

2) Capacitor Model: The models of the dc capacitors are

$$i_o = C\frac{d\Delta u_{dc}}{dt} \tag{2}$$

$$i_{fj} = C_1\frac{du_{dc\_j1}}{dt} \tag{3}$$

where

$$i_o = \sum_{j=a,b,c} i_{oj} = \sum_{j=a,b,c}\left(S_{j1}+S_{j5}-2S_{j1}S_{j5}\right)i_j \tag{4}$$

$$i_{fj} = S_{j5}i_j - S_{j7}i_{j1} - S_{j9}i_{j2}. \tag{5}$$

3) Inner Circulating Current Model: The models of the inner circulating currents can be given by

$$u_{jo1} - u_{jo2} = 2L_0\frac{di_{cj}}{dt} \tag{6}$$

where

$$\begin{cases} u_{jo1} = U_{dc}\left(S_{j1}/2 + S_{j5}/4 + S_{j7}/4 - 1/2\right) \\ u_{jo2} = U_{dc}\left(S_{j1}/2 + S_{j5}/4 + S_{j9}/4 - 1/2\right) \end{cases} \tag{7}$$

$$i_{cj} = \left(i_{j1} - i_{j2}\right)/2. \tag{8}$$

TABLE II
COMPARISON OF VARIOUS NINE-LEVEL MULTILEVEL CONVERTERS

Topology	Device Count			Energy Storage
	LFS Switch	HFS Switch	FC	
FCC	0	16	7	$\varepsilon = \frac{43}{32}CU_{dc}^2$
HMMC	4	8	4	$\varepsilon = \frac{3}{8}CU_{dc}^2$
ANPC-9L	4	8	3	$\varepsilon = \frac{23}{64}CU_{dc}^2$
ANPC-5L-H	4	8	2	$\varepsilon = \frac{37}{128}CU_{dc}^2$
S-T	0	16	6	$\varepsilon = \frac{15}{32}CU_{dc}^2$
T-ANPC	4	10	4	$\varepsilon = \frac{21}{64}CU_{dc}^2$
FC-IPC	4	8	2	$\varepsilon = \frac{5}{16}CU_{dc}^2$
Nine-Level IHMC	4	6	1	$\varepsilon = \frac{9}{32}CU_{dc}^2$

4) Discrete-Time Model: The discrete-time models can be obtained by applying the Euler Forward Approximation as

$$\boldsymbol{i}(k+1) = T_s\boldsymbol{v}(k)/L_{eq} + \left(1 - RT_s/L_{eq}\right)\boldsymbol{i}(k) \tag{9}$$

$$\Delta u_{dc}(k+1) = T_s i_o(k)/C + \Delta u_{dc}(k) \tag{10}$$

$$u_{dc\_j1}(k+1) = T_s i_{fj}(k)/C_1 + u_{dc\_j1}(k) \tag{11}$$

$$i_{cj}(k+1) = T_s\left[u_{jo1}(k) - u_{jo2}(k)\right]/(2L_0) + i_{cj}(k). \tag{12}$$

When applying multiple vectors, the current variables at time instant k can be given by

$$\begin{cases} i_{cj}(k) = \left[i_{j1}(k) - i_{j2}(k)\right]/2 \\ i_{fj}(k) = d_{j5}i_j(k) - d_{j7}i_{j1}(k) - d_{j9}i_{j2}(k) \\ i_o(k) = \sum_{j=a,b,c}\left(d_{j1} + d_{j5} - 2d_{j1}d_{j5}\right)i_j(k) \end{cases}. \tag{13}$$

The voltage variables at time instant k can be given in the duty cycle manner by:

$$\begin{cases} u_{jo1}(k) = U_{dc}\left(d_{j1}/2 + d_{j5}/4 + d_{j7}/4 - 1/2\right) \\ u_{jo2}(k) = U_{dc}\left(d_{j1}/2 + d_{j5}/4 + d_{j9}/4 - 1/2\right) \end{cases} \tag{14}$$

where d_{jx} can be simply derived through switching states of the employed vectors and their corresponding dwell time.

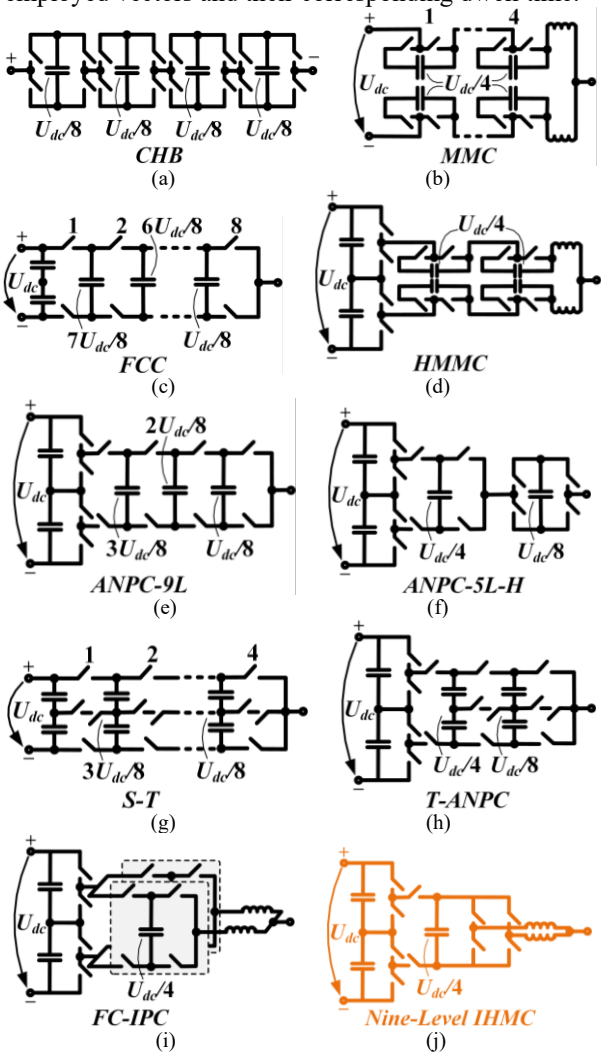

Fig. 2. Various nine-level multilevel topologies. (a) CHB, (b) MMC, (c) FCC, (d) HMMC, (e) ANPC-9L, (f) ANPC-5L-H, (g) S-T, (h) T-ANPC, (i) FC-IPC, and (j) Nine-level IHMC.

III. Hybrid Multivector Model Predictive Control

A. LFS Control

The control framework of the proposed HMV-MPC is given in Fig. 3. Since S_{j1}/S_{j3} works at fundamental switching frequency, it can be directly determined by the sign pattern of the references. The reference vector, through the use of the system model (1), can be given by:

$$\boldsymbol{v}^*(k)=\frac{L_{eq}}{T_s}\boldsymbol{i}^*(k+1)+\left(R-\frac{L_{eq}}{T_s}\right)\boldsymbol{i}(k). \tag{15}$$

Then the reference vector in the *abc*-frame can be derived by the inverse Clarke Transformation [37] as $\boldsymbol{v_{abc}}^* = [v_a^*\ v_b^*\ v_c^*]^{\mathrm{T}}$.

As such, the original space vector diagram (SVD) of the IHMC can be categorized into six types of internal hexagons (Fig. 4), i.e., the virtual SVDs, which respectively, refer to the six sign patterns described in Table III. It is noteworthy that although the reference vector may lie in the overlapped area of two adjacent internal hexagons, there are redundant switching states for each voltage vector in the space vector diagram, which are affiliated to adjacent hexagons separately. In other words, the voltage vectors in the overlapped areas have redundant switching states that can be subject to two different adjacent hexagons, which can be used individually to obtain optimal control performance.

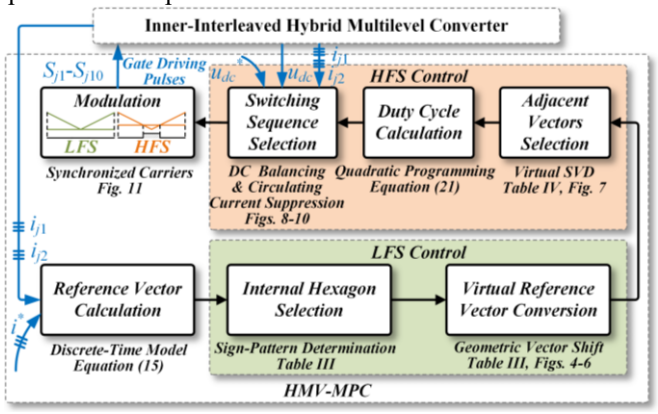

Fig. 3. The control framework of the proposed HMV-MPC.

As depicted in Fig. 5, the reference vector can be converted from the original SVD to the virtual SVD as

$$\boldsymbol{v}_v^* = \boldsymbol{v}^* - \boldsymbol{V}_n. \tag{16}$$

Proceeding to Fig. 6, the switching states of the original SVD and the virtual switching states of the virtual SVD are highlighted with yellow and grey background, respectively. Through adding the "Shift State" in Table III to the virtual switching states, the original switching states can be obtained.

TABLE III
Switching States of the Internal Hexagon

Sign Pattern v_a^*	v_b^*	v_c^*	$S_{a1}S_{b1}S_{c1}$ ($S_{a3}S_{b3}S_{c3}$)	Internal Hexagon (H_n)	Shift Vector ($\boldsymbol{V_n}$)	Shift State ($\boldsymbol{S_n}$)
≥0	≤0	≤0	100	H_1	$\boldsymbol{V_1}$ = [4 0]	$\boldsymbol{S_1}$ = [4 0 0]
≥0	≥0	≤0	110	H_2	$\boldsymbol{V_2}$ = [2 2√3]	$\boldsymbol{S_2}$ = [4 4 0]
≤0	≥0	≤0	010	H_3	$\boldsymbol{V_3}$ = [−2 2√3]	$\boldsymbol{S_3}$ = [0 4 0]
≤0	≥0	≥0	011	H_4	$\boldsymbol{V_4}$ = [−4 0]	$\boldsymbol{S_4}$ = [0 4 4]
≤0	≤0	≥0	001	H_5	$\boldsymbol{V_5}$ = [−2 −2√3]	$\boldsymbol{S_5}$ = [0 0 4]
≥0	≤0	≥0	101	H_6	$\boldsymbol{V_6}$ = [2 −2√3]	$\boldsymbol{S_6}$ = [4 0 4]

B. HFS Control

1) Multivector Selection:

There are two effective ways to facilitate the selection process: 1) through leveraging the symmetry of the virtual SVD [18], the selection process can be performed in Sector 1 of the virtual SVD, and 2) via converting the $\alpha\beta$-frame to the 120° *gh*-frame [18], a complete integer coordinate system is established, which leads to the integer arithmetic when seeking multiple vectors, which further, translates into a much simpler calculation process than the trigonometric calculation or the lookup-table approach [31].

Fig. 7 depicts the virtual reference vector and its adjacent vectors in Sector 1 of the virtual SVD, where the minimum-value switching states are defined as the fundamental switching states (FSSs). The conversion table of the FSSs is

exhibited in Table IV, where $[S_{va1}\ S_{vb1}\ S_{vc1}]$ is the FSS in Sector 1. The vector $\boldsymbol{V_1}$ in the 120° gh-frame can be given by

$$[g_{v0}\quad h_{v0}]^{\mathrm{T}}=\left[\lfloor V_{vg1}\rfloor\quad \lfloor V_{vh1}\rfloor\right]^{\mathrm{T}}. \tag{17}$$

The following criterion can be applied to further define the switching triangle type where the reference vector locates in:

$$\boldsymbol{v_{v1}}^{*}\in\begin{cases}\mathrm{I},\ V_{vg1}-V_{vh1}\le g_{v0}-h_{v0}\\ \mathrm{II},\ V_{vg1}-V_{vh1}>g_{v0}-h_{v0}\end{cases}. \tag{18}$$

Recapping Fig. 7, the vectors $\boldsymbol{V_k}$ are the chosen adjacent vectors, the FSSs of which can be deduced from the vector coordinates, as per the characteristic of the 120° coordinate system [18].

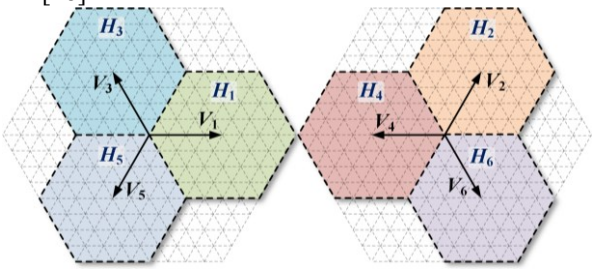

Fig. 4. Six virtual SVDs in the original SVD.

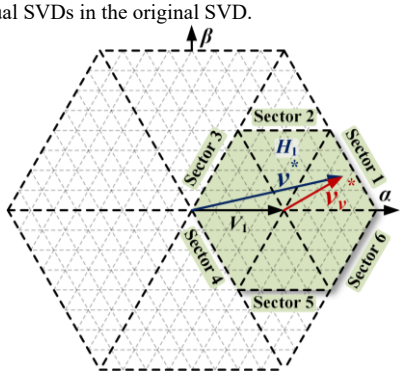

Fig. 5. Vector shifting process (to Hexagon H1).

2) Duty Cycle Optimization:

TABLE IV
FSS CONVERSION TABLE

Sector	Phase A	Phase B	Phase C
1	S_{va1}	S_{vb1}	S_{vc1}
2	S_{va1}−S_{vb1}	S_{va1}	0
3	0	S_{va1}	S_{vb1}
4	0	S_{va1}−S_{vb1}	S_{va1}
5	S_{vb1}	0	S_{va1}
6	S_{va1}	0	S_{va1}−S_{vb1}

The duty cycle optimization is enabled by the current tracking error minimization. The current slopes are given by

$$\boldsymbol{s_k}=\left(\boldsymbol{V_k}-\boldsymbol{i}R\right)/L \tag{19}$$

where $\boldsymbol{s_k}=[s_{\alpha k}\ s_{\beta k}]^{\mathrm{T}}$. Then, the current error can be given by

$$\begin{cases}\Delta I_\alpha=I_\alpha-s_{\alpha1}t_1-s_{\alpha2}t_2-s_{\alpha3}\left(T_s-t_1-t_2\right)\\ \Delta I_\beta=I_\beta-s_{\beta1}t_1-s_{\beta2}t_2-s_{\beta3}\left(T_s-t_1-t_2\right)\end{cases} \tag{20}$$

where $I_\alpha=i_\alpha^*(k{+}1){-}i_\alpha(k)$, $I_\beta=i_\beta^*(k{+}1){-}i_\beta(k)$. Subsequently, the cost function is given by $J=\Delta I_\alpha^2{+}\Delta I_\beta^2$. To solve the quadratic programming problem, the optimal condition can be obtained through the gradient method [38]:

$$\partial J/\partial t_1=0\,;\,\partial J/\partial t_2=0\,. \tag{21}$$

Solving (21) yields the optimal duty cycles:

$$\begin{cases}d_1=\dfrac{I_\alpha\left(s_{\beta3}-s_{\beta2}\right)+I_\beta\left(s_{\alpha2}-s_{\alpha3}\right)+T_s\left(s_{\alpha3}s_{\beta2}-s_{\alpha2}s_{\beta3}\right)}{T_s s_{\beta1}\left(s_{\alpha2}-s_{\alpha3}\right)+T_s s_{\beta2}\left(s_{\alpha3}-s_{\alpha1}\right)+T_s s_{\beta3}\left(s_{\alpha1}-s_{\alpha2}\right)}\\ d_2=\dfrac{I_\alpha\left(s_{\beta1}-s_{\beta3}\right)+I_\beta\left(s_{\alpha3}-s_{\alpha1}\right)+T_s\left(s_{\alpha1}s_{\beta3}-s_{\alpha3}s_{\beta1}\right)}{T_s s_{\beta1}\left(s_{\alpha2}-s_{\alpha3}\right)+T_s s_{\beta2}\left(s_{\alpha3}-s_{\alpha1}\right)+T_s s_{\beta3}\left(s_{\alpha1}-s_{\alpha2}\right)}\\ d_3=1-d_1-d_2\end{cases} \tag{22}$$

where $d_k=t_k/T_s$.

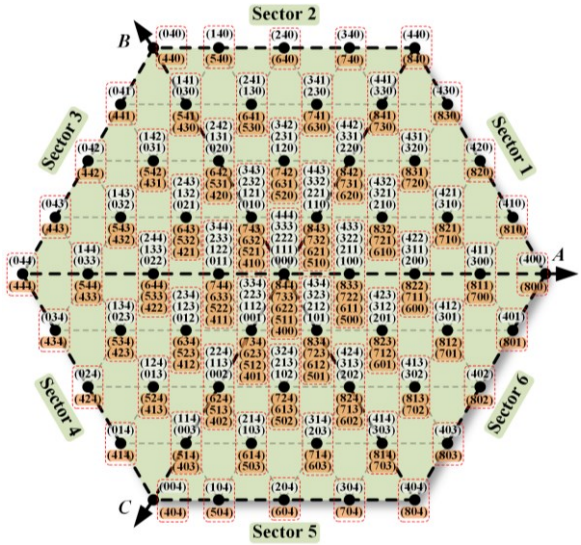

Fig. 6. Original and virtual SSs in the virtual SVD (Hexagon H1).

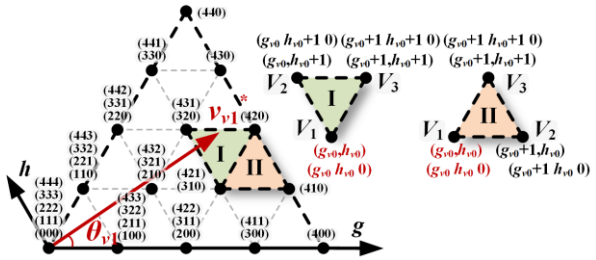

Fig. 7. The multiple adjacent vectors in Sector 1 of the virtual SVD.

3) Switching Sequence Selection and Modulation:

The symmetric switching sequences (SSs), the ones have fixed equivalent switching frequency, can be achieved through: 1) shifting only one voltage level over each switching cycle and 2) resuming the voltage level when each switching cycle ends to lower switching actions. Fig. 8 shows the switching states of the chosen vectors distributed to six sectors, and Fig. 9 enumerates all the symmetric SSs that are subject to the chosen vectors, where the vectors of each sector are marked with various background color. Notably, four switching states are employed in total over each control cycle. As it can be seen, the initial direction of the vector rotation in Sectors 1, 3, and 5 is inverse to that in Sectors 2, 4, and 6, i.e., in a clockwise and counter-clockwise manner, respectively. As such, all the symmetric SSs can be found in an effort to leverage the symmetry of the virtual SVD, which further leads to the abandonment of the inefficient lookup-table [31].

Further, selecting the symmetric SS can be transformed into an optimization problem whose constraint conditions are the regulation of dc capacitor voltages and suppression of inner circulating currents. Thus, the cost functions can be given by

$$\begin{cases} J_{dc} = \sum_{j=a,b,c} \left\| u_{dc\_j1}(k+1) - U_{dc}/4 \right\|_2^2 + \left\| \Delta u_{dc}(k+1) \right\|_2^2 \\ J_{cir} = \sum_{j=a,b,c} \left\| i_{cj}(k+1) \right\|_2^2 \\ J = \lambda_1 J_{dc} + \lambda_2 J_{cir} \end{cases} . \quad (23)$$

In addition, the duty cycles of each switch can be derived by

$$d_{jx} = D_1 \left(S_{jx\_1} + S_{jx\_4} \right) / 2 + D_2 S_{jx\_2} + D_3 S_{jx\_3} \quad (24)$$

where $D_k \in \{d_1, d_2, d_3\}$, which is defined as the duty cycles of the vectors in the candidate SS, with the initial vector being either $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, or $\boldsymbol{V}_3$, and S_{jx_i} can be inferred from the ith switching state in the SS to be evaluated. Subsequently, the variables at time instant k+1 can be attained by substituting (24) into (10)-(14). As a result, the description of the constrained optimization problem for seeking the optimal symmetric SS can be given by

$$\begin{cases} \min\limits_{S_{jx\_i}} J \\ s.t. \quad \text{equations (10)-(14), (22), and (24)} \\ \quad S_{jx\_i} \in \{0,\ 1\} \\ \quad \sum_{i=1}^{3} D_i = 1 \end{cases} . \quad (25)$$

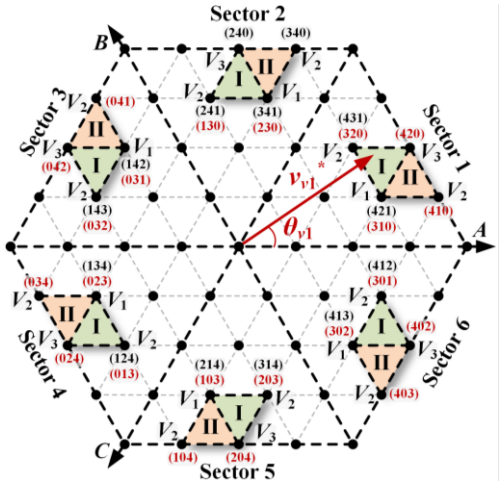

Fig. 8. The virtual SVD and switching states distributed to its six sectors.

Fig. 10 illustrates a flowchart, which, together with the control diagram in Fig. 3, gives an overview of the proposed HMV-MPC strategy. On top of that, the modulation for each switch can be conducted individually [7] through comparing the duty cycles derived from (24) with a group of synchronized triangle carriers. Fig. 11 exemplifies the modulation of one particular case in Figs. 8 and 9, where the selected SS in the virtual SVD is: (310), (320), (420), (421), (420), (320), and (310), which is equivalent to the SS in the original SVD: (531), (541), (641), (642), (641), (541), and (531), is selected (D_1 = 1/2, D_2 = 1/4, D_3 = 1/4). As it can be seen, whenever the switching states unfolds the state shift of 1-to-0, it needs to adjust its derived duty cycle from (24), e.g., the S_{b9} is modulated by an inverse triangle carrier in Fig. 11.

In addition, due to the adoption of multiple vectors over each switching period, the delay effect caused by digital implementation is even severer [14], which significantly exacerbates the dc capacitor voltage balancing in particular. It is therefore of great significance to eradicate the adverse effect of the delay through two-step prediction of not only the current but also the dc voltages and circulating currents [7].

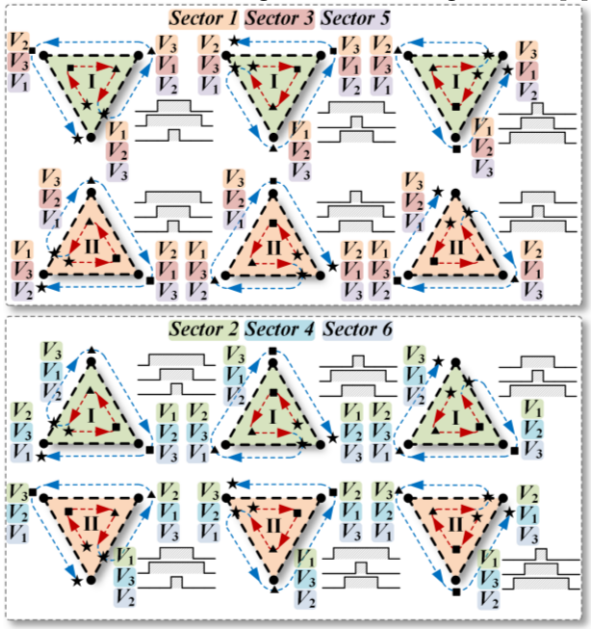

Fig. 9. Symmetric SSs subject to the chosen vectors.

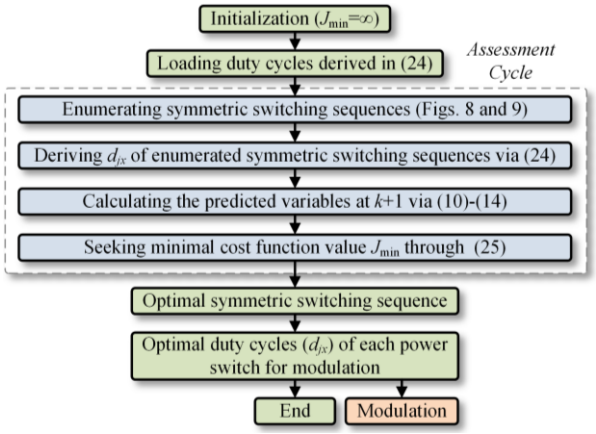

Fig. 10. Flowchart of the optimal SS selection.

IV. Experimental Results

To evaluate the proposed HMV-MPC in a real-world scenario, an all-SiC scaled-down prototype is developed using the discrete SiC MOSFETs (Wolfspeed: C2M0160120D, 1.2 kV, 18 A, 160 mΩ) [39]. The system parameters are listed in Table IV. Fig. 12 shows the experimental rig. The control algorithm is conducted in the dSPACE MicroLabBox, while the gate pulses are generated by an Intel Max-10 FPGA. The optic fibers are used to enhance the noise immunity. To avoid

the infeasibility caused by tremendous computational burden, a modified C-MPC, which only assesses three vectors that encompass the reference vector [18], is used for comparison. Table V summarizes the average switching frequency and current THD comparison. As shown, the HMV-MPC at 8 kHz sampling rate even has lower average switching frequency than the C-MPC at 15 kHz sampling rate does, which hence, can be used as a benchmark for fair comparison. In addition, the operation limitation analysis of the nine-level IHMC with both the C-MPC and the proposed HMV-MPC is conducted through simulation study (since the resistive-inductive load is the only load we have) [13], [18]. All other parameters are the same as Table IV. The power factor is regulated through changing the load resistance, while the reference current is adjusted correspondingly based on the load impedance calculation at the same time. Whenever the inner circulating currents or floating capacitor voltages cannot be mitigated or balanced, the system is considered unstable. In this regard, the operation limitations are demonstrated in Fig. 13. As shown, for the vast majority of the operating points, the system is stable. Specifically, for all the circumstances enclosed by the solid line, the inner circulating currents or floating capacitor voltages can be mitigated or balanced, while for the conditions beyond the solid line, these control objectives cannot be guaranteed, thus, the converter system is unstable.

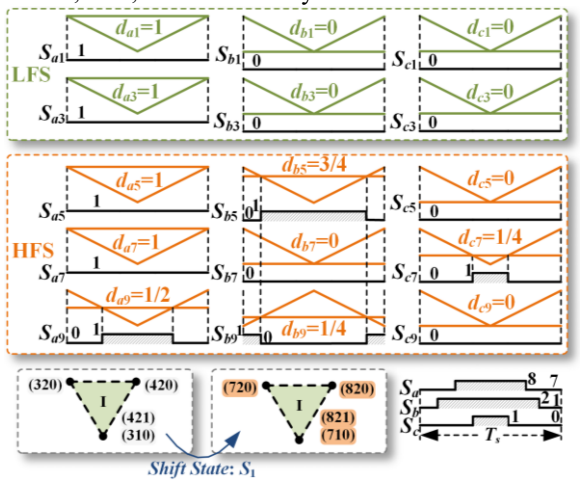

Fig. 11. Modulation of one specific symmetric SS.

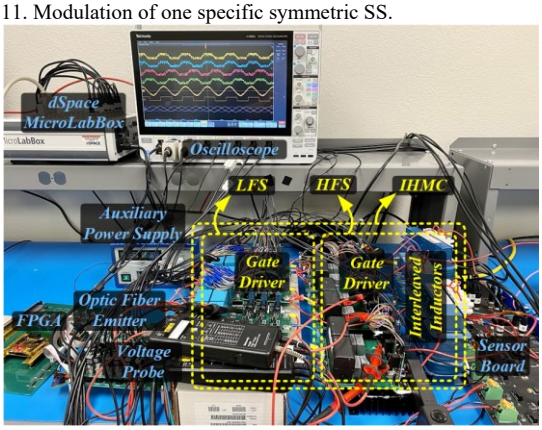

Fig. 12. Experimental rig.

Fig. 14 shows the steady-state waveforms, where the pulse trains of S_{a1} of the proposed HMV-MPC unfold fundamental-frequency patterns, which are in line with the control objective. On the contrary, the C-MPC reveals a relatively high-frequency patterns for pulse trains of S_{a1}. As set forth in Section III, the low-frequency pulse trains can enable fewer switching actions than the high-frequency ones and thus, results in lower switching losses. In addition, since the proposed HMV-MPC is actually based on the line-to-line voltage control from the SVD point of view, the equivalent line-to-line voltage v_{ab} shows a clear sinusoidal shape, which also possesses more voltage levels than the phase voltages do.

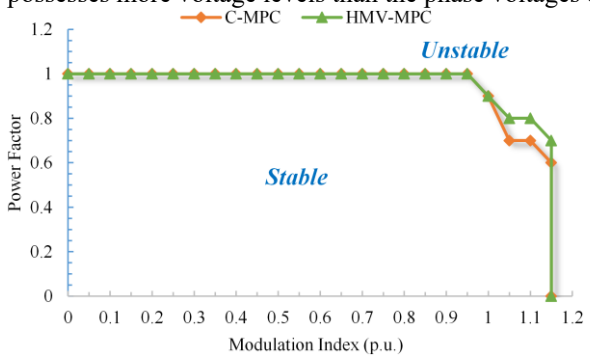

Fig. 13. Experimental rig.

Fig. 15 exemplifies Phase A to exhibit the steady-state performances of both control strategies. As it can be seen, even though the circulating current under the proposed HMV-MPC appears to have slightly larger ripples than the C-MPC does, the output current waveform of the proposed HMV-MPC at 8 kHz sampling rate is smoother than those of the C-MPC at both 8 kHz and 15 kHz sampling rate. Therefore, the main control objective, the current tracking, is better safeguarded by the proposed HMV-MPC. The dc voltages are all well-regulated under both control strategies. Fig. 16 demonstrates the waveforms at transient-state. As shown, all the dc voltages are well-regulated to their reference despite some trivial surges, which are caused by the inner-regulation of the dc power source. It also noteworthy that proposed HMV-MPC and the C-MPC at 8 kHz sampling rate have approximately the same responding time, while the C-MPC at 15 kHz has shorter responding time due to a higher sampling rate. In a nutshell, the responding time at all scenarios is relatively fast and the proposed HMV-MPC retains the fast dynamics nature of the MPC, while improves the current tracking performance at the same time. Furthermore, as it can be observed from the phase voltages, the C-MPC has a relatively higher dv/dt especially at the lower modulation range, where the phase voltage may shift more than one unit voltage step ($U_{dc}/4$), which is caused by the concurrent switching action among power devices and may exacerbate the noise immunity of gate drivers. On the contrary, the HMV-MPC unfolds lower dv/dt due to the decoupling of the LFS and HFS, which shows another superior aspect over the C-MPC.

To further showcase the current THD improvement of HMV-MPC, the current spectra comparison based on the collected oscilloscope data are depicted in Fig. 16. It can be observed in Fig. 16 that the proposed HMV-MPC at 8 kHz

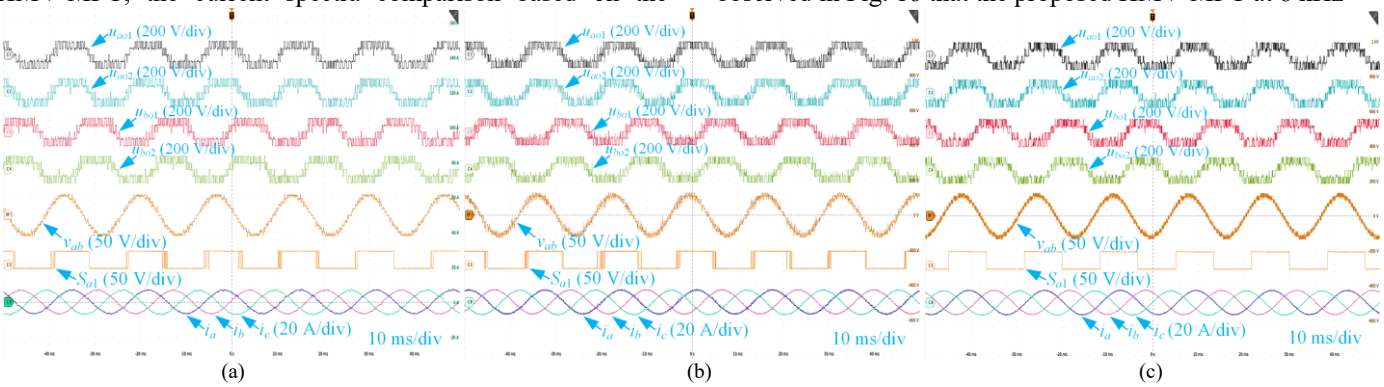

Fig. 13. Waveforms of steady-state. (a) C-MPC at 8 kHz sampling rate. (b) C-MPC at 15 kHz sampling rate. (c) HMV-MPC at 8 kHz sampling rate.

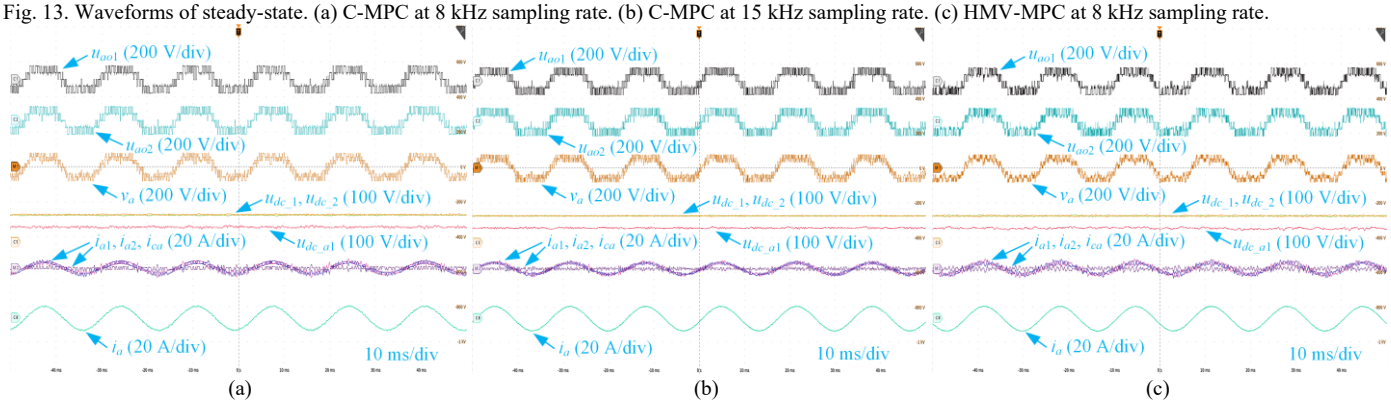

Fig. 14. Waveforms of steady-state. (a) C-MPC at 8 kHz sampling rate. (b) C-MPC at 15 kHz sampling rate. (c) HMV-MPC at 8 kHz sampling rate.

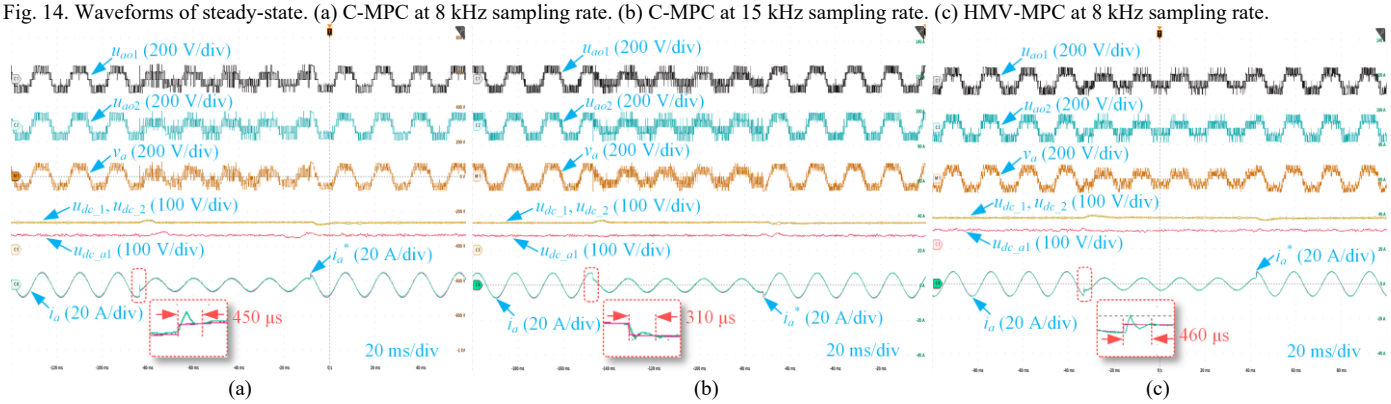

Fig. 15. Waveforms of transient-state. (a) C-MPC at 8 kHz sampling rate. (b) C-MPC at 15 kHz sampling rate. (c) HMV-MPC at 8 kHz sampling rate.

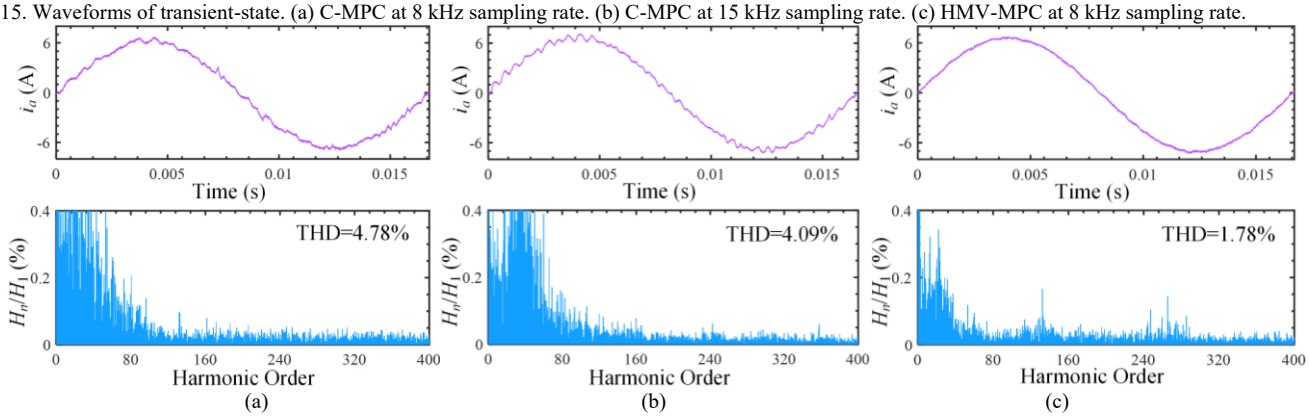

Fig. 16. Current spectra comparison. (a) C-MPC at 8 kHz sampling rate. (b) C-MPC at 15 kHz sampling rate. (c) HMV-MPC at 8 kHz sampling rate.

sampling rate has much lower current THD than the C-MPC does at both 8 kHz and 15 kHz sampling rate. In addition, there are concentrated harmonic groups around 8 kHz, 16 kHz, and so on, in the output current spectra under the proposed

HMV-MPC, while the current spectra of C-MPC at both 8 kHz and 15 kHz exhibit more widespread fashions.

Fig. 17 depicts the comparison of the current THD versus amplitude by using the data in Table V. As shown, the current THD of the proposed HMV-MPC at 8 kHz sampling rate is lower than those of the C-MPC at both 8 kHz and 15 kHz sampling rate. Thus, it can be interpreted that the proposed HMV-MPC has better current tacking performance than the C-MPC does with even lower average switching frequency. Further, Fig. 18 shows the turnaround time comparison between the two algorithms, where the turnaround time is calculated in dSPACE using the real-time mode. Apparently, the proposed HMV-MPC enables approximately 34% turnaround time reduction, which indicates another advantage of the proposed HMV-MPC in addition to the current THD reduction.

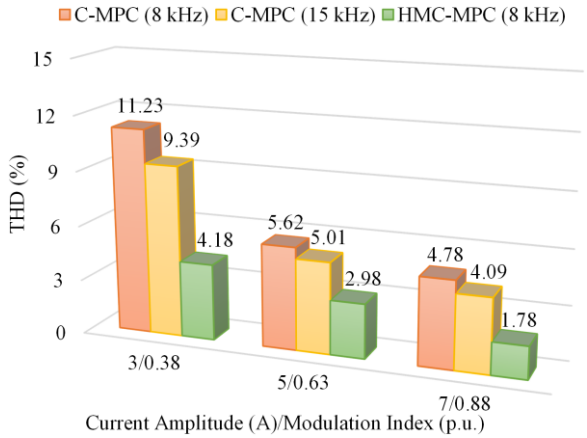

Fig. 17. Current THD comparison.

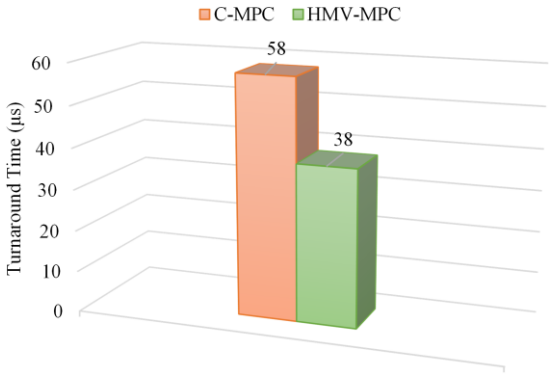

Fig. 18. Turnaround time comparison.

TABLE IV
SYSTEM PARMETERS

Variable Description	Symbol	Value
Interleaved inductance	L_0	2.5 mH
Load inductance	L	1.5 mH
Load resistance	R	10 Ω
DC-link capacitance	C	240 μF
Floating capacitance	C_1	200 μF
Floating capacitor voltage	U_{dc}	160 V
H-bridge dc voltage	$u_{dc\ j1}$	40 V
Dead time	T_d	1 μs
Fundamental frequency	f	60 Hz

TABLE V
THD AND SWITCHING FREQUENCY VERSUS CURRENT AMPLITUDE

Current Amplitude (A)	Control Method/ Sampling Rate	Average Switching Frequency (kHz)	THD (i_a, %)
3/0.38	C-MPC/8 kHz	2.552	11.23
	C-MPC/15 kHz	4.141	9.39
	HMV-MPC/8 kHz	**3.344**	**4.18**
5/0.63	C-MPC/8 kHz	2.254	5.62
	C-MPC/15 kHz	3.727	5.01
	HMV-MPC/8 kHz	**3.147**	**2.98**
7/0.88	C-MPC/8 kHz	1.708	4.78
	C-MPC/15 kHz	3.238	4.09
	HMV-MPC/8 kHz	**3.017**	**1.78**

V. CONCLUSION

This article brings forward an HMV-MPC for a nine-level IHMC. The performance of the HMV-MPC is studied through comprehensive experiments, where the results substantiate the following aspects:

1) The proposed method enables the independent operation of the LFS and HFS, which leads to the reduction of the average switching frequency and may further pave the way for the hybrid use of SiC metal-oxide semiconductor field-effect transistors (MOSFETs) to the HFS and silicon (Si) insulated-gate bipolar transistors (IGBTs) to the LFS, to significantly enhance the cost-effectiveness and efficiency of the system.
2) The proposed method cuts down both the calculation burden and output current THD while retaining the fast dynamics nature of the MPC simultaneously.
3) The proposed method achieves a constant equivalent switching frequency and overcomes the variable switching frequency associated with the C-MPC, which further facilitates the filter design.
4) The dc capacitor voltage balancing and circulating current suppression are independent from the current tacking and therefore, has no impact on it.

REFERENCES

[1] J. Liu, D. Dong, and D. Zhang, "A hybrid modular multilevel converter family with higher power density and efficiency," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9001-9014, Aug. 2021.
[2] Y. Li, Y. Wang, and B. Q. Li, "Generalized theory of phase-shifted carrier PWM for cascaded H-bridge converters and modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 589-605, Jun. 2016.
[3] F. Diao, Y. Li, Z. Wang, Y. Wu, and Y. Zhao, "A computational efficient space-vector modulation scheme for a hybrid seven-level converter for medium voltage grid-tied applications," in *Proc. IEEE APEC*, pp. 1786-1790, 2020.
[4] J. Liu, D. Dong, and D. Zhang, "Hybrid modular multilevel rectifier, a new rectifier topology for HVDC power delivery," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8583-8587, Aug. 2021.
[5] H. Tian and Y. W. Li, "An active capacitor voltage balancing method for seven-level hybrid clamped (7L-HC) converter in motor drives," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2372–2388, Mar. 2020.
[6] Y. Li *et al*., "Distributed generation grid-connected converter testing device based on cascaded H-bridge topology," *IEEE Trans. Ind. Electron*., vol. 63, no. 4, pp. 2143-2154, April 2016.
[7] Y. Li and Y. Zhao, "A virtual space vector model predictive control for a seven-level hybrid multilevel converter," *IEEE Trans. Power Electron*., vol. 36, no. 3, pp. 3396-3407, March 2021.
[8] Z. Quan and Y. W. Li, "Multilevel voltage-source converter topologies with internal parallel modularity," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 378-389, Jan.-Feb. 2020.

[9] S. Xu, J. Zhang, G. Ma, Z. Sun, K. Liu, and C. Yao, "Operation of a seven-level T-type active neutral-point-clamped converter with modified level-shifted PWM," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2020.3038067.

[10] K. Wang, Z. Zheng, L. Xu, and Y. Li, "An optimized carrier-based PWM method and voltage balancing control for five-level ANPC converters," *IEEE Trans. Ind. Electron*., vol. 67, no. 11, pp. 9120–9132, Nov. 2020.

[11] T. T. Davis and A. Dey, "Investigation on extending the DC bus utilization of a single-source five-level inverter with single capacitor-fed H-bridge per phase," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2914–2922, Mar. 2019.

[12] Y. Li, F. Diao, and Y. Zhao, "A generic multi-vector model predictive control with symmetric pulse pattern for hybrid multilevel converters," *IEEE Trans. Ind. Electron.*, to be published, doi: 10.1109/TIE.2020.3040691.

[13] M. Saeedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 452-466, Feb. 2009.

[14] J. Rodriguez and P. Cortes, *Predictive control of power converters and electrical drives*, Chichester, West Sussex, UK: Wiley, 2012.

[15] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935-947, Feb. 2017.

[16] A. Dekka, B. Wu, V. Yaramasu, R. L. Fuentes, and N. R. Zargari, "Model predictive control of high-power modular multilevel converters—an overview," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 7, no. 1, pp. 168-183, March 2019.

[17] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," *IEEE Trans. Power Electron*., vol. 35, no. 7, pp. 7434–7450, 2020.

[18] Y. Li, F. Diao, and Y. Zhao, "Simplified two-stage model predictive control for a hybrid multilevel converter with floating H-bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4839-4850, April 2021.

[19] J. Huang, *et al.*, "Priority sorting approach for modular multilevel converter based on simplified model predictive control," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4819-1830, Jun. 2018.

[20] Y. Li, Y. Zhao, and F. Diao, "High-efficiency model predictive control for star-connected cascaded H-bridge STATCOM under unbalanced conditions," in *Proc. IEEE APEC*, pp. 982-988, 2020.

[21] M. Vatani, B. Bahrani, M. Saeedifard, and M. Hovd, "Indirect finite control set model predictive control of modular multilevel converters," *IEEE Trans. Smart Grid*, vol. 6, no. 3, pp. 1520-1529, May 2015.

[22] T. Geyer and D. E. Quevedo, "Performance of multistep finite control set model predictive control for power electronics," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1633-1644, March 2015.

[23] C. Qi, X. Chen, P. Tu, and P. Wang, "Cell-by-cell-based finite-control-set model predictive control for a single-phase cascaded H-bridge rectifier," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1654-1665, Feb. 2018.

[24] T. Dragičević, "Model predictive control of power converters for robust and fast operation of AC microgrids," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6304-6317, July 2018.

[25] J. Lee, J. Lee, H. Moon, and K. Lee, "An improved finite-set model predictive control based on discrete space vector modulation methods for grid-connected three-level voltage source inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1744-1760, Dec. 2018.

[26] I. Osman, D. Xiao, K. S. Alam, S. M. S. I. Shakib, M. P. Akter, and M. F. Rahman, "Discrete space vector modulation-based model predictive torque control with no suboptimization," *IEEE Trans. Ind. Electron*., vol. 67, no. 10, pp. 8164-8174, Oct. 2020.

[27] W. Alhosaini, F. Diao, M. H. Mahmud, Y. Wu, and Y. Zhao, "A Virtual Space Vector-Based Model Predictive Control for Inherent DC-Link Voltage Balancing of Three-Level T-Type Converters," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 9, no. 2, pp. 1751-1764, April 2021.

[28] P. Cortes, J. Rodriguez, D. E. Quevedo, and C. Silva, "Predictive current control strategy with imposed load current spectrum," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 612-618, March 2008.

[29] M. Aguirre, S. Kouro, C. A. Rojas, and S. Vazquez, "Enhanced switching frequency control in FCS-MPC for power converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2470-2479, March 2021.

[30] Y. Zhang, Y. Peng, and H. Yang, "Performance improvement of twovectors-based model predictive control of PWM rectifier," *IEEE Trans. Power Electron*., vol. 31, no. 8, pp. 6016-6030, Aug. 2016.

[31] S. Kang, J. Soh, and R. Kim, "Symmetrical three-vector-based model predictive control with deadbeat solution for IPMSM in rotating reference frame," *IEEE Trans. Ind. Electron*., vol. 67, no. 1, pp. 159-168, Jan. 2020.

[32] C. B. Barth *et al*., "Design and control of a GaN-based, 13-level, flying capacitor multilevel inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2179-2191, Sept. 2020.

[33] P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 2005, pp. 2296–2301.

[34] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 689–702, Jan. 2018.

[35] L. Delmas, G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): control and natural balancing," in *Proc. IEEE 33rd Annu. IEEE Power Electron. Spec. Conf*., Jun. 2002, pp. 689–694.

[36] C. Xu, L. Lin, T. Yin, and J. Hu, "An improved phase-shifted-carrier technique for hybrid modular multilevel converter with boosted modulation index," *IEEE Trans. Power Electron*., vol. 35, no. 2, pp. 1340-1352, Feb. 2020.

[37] L. Harnefors, "Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2239–2248, Aug. 2007.

[38] Y. Nesterov, "A method of solving a convex programming problem with convergence rate O ($1/k^2$)," *Sov. Math. Dokl*., vol. 27, no. 2, pp. 372–386, 1983.

[39] Wolfspeed. "Datasheet C2M0160120D Silicon-Carbide Power MOSFET," 2019, [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C2M0160120D.pdf.

Yufei Li (Member, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2009, where he was subsequently given the exam-exemption for outstanding undergraduates to pursue the M.S. degree and pivoted to directly pursue the Ph.D. degree in 2011, and received the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2016.

From 2016 to 2017, he was an Electrical Engineer with State Grid Corporation of China, Xi'an, China. From 2017 to 2019, he was an Assistant Professor with the Department of Electrical Engineering, Northwestern Polytechnical University, Xi'an, China. From 2019 to 2021, he was a Postdoctoral Fellow with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA. Since September 2021, he has been with the Department of Electrical and Computer Engineering, Princeton University, Princeton, NJ, USA, where he is currently an Associate Research Scholar. His research interests include power converter control, multilevel converters, machine learning methods for power electronics, and wide bandgap power device applications.

Fei Diao (Student Member, IEEE) received the B.E. and M.E. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA.

In 2020 and 2021, he was a Summer Intern with Eaton Corporation, Menomonee Falls, WI, USA. His main research interests include modulation and control of multilevel converters and wide bandgap power device applications.

Yue Zhao (Senior Member, IEEE) received a B.S. degree in electrical engineering from Beijing University of Aeronautics and Astronautics, Beijing, China, in 2010, and a Ph.D. degree in electrical engineering from the University of Nebraska-Lincoln, Lincoln, USA, in 2014.

He was an Assistant Professor in the Department of Electrical and Computer Engineering at the

Virginia Commonwealth University, Richmond, USA, in 2014-2015. Since August 2015, he has been with the University of Arkansas, Fayetteville, USA, where he is currently an Associate Professor in the Department of Electrical Engineering. He also serves as the site director for National Science Foundation (NSF) Center for GRid-connected Advanced Power Electronic Systems (GRAPES). His current research interests include electric machines and drives, power electronics, and renewable energy systems. He has 4 U.S. patents granted and co-authored more than 100 papers in refereed journals and international conference proceedings.

Dr. Zhao is an Associated Editor of the IEEE Transactions on Industry Applications and IEEE Open Journal of Power Electronics. He was a recipient of 2018 U.S. National Science Foundation CAREER Award, the 2020 IEEE Industry Applications Society Andrew W. Smith Outstanding Young Member Achievement Award and the 2020 UA College of Engineering Dean's Award of Excellence.