PAPER

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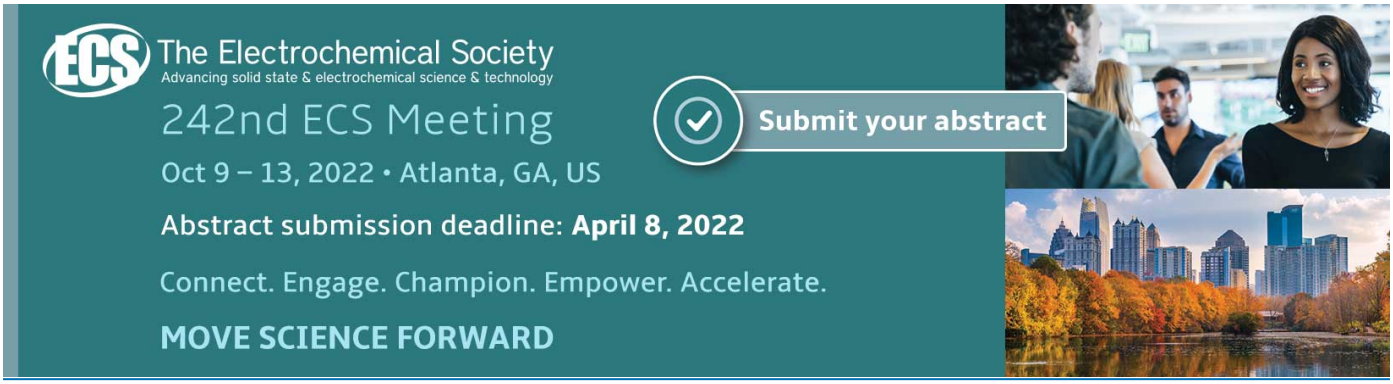

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Analysis of Schottky barrier heights and reduced Fermi-level pinning in monolayer CVD-grown MoS_2 field-effect-transistors

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Abstract

Chemical vapor deposition (CVD)-grown monolayer (ML) molybdenum disulfide (MoS_2) is a promising material for next-generation integrated electronic systems due to its capability of high-throughput synthesis and compatibility with wafer-scale fabrication. Several studies have described the importance of Schottky barriers in analyzing the transport properties and electrical characteristics of MoS_2 field-effect-transistors (FETs) with metal contacts. However, the analysis is typically limited to single devices constructed from exfoliated flakes and should be verified for large-area fabrication methods. In this paper, CVD-grown ML MoS_2 was utilized to fabricate large-area (1 cm × 1 cm) FET arrays. Two different types of metal contacts (i.e. Cr/Au and Ti/Au) were used to analyze the temperature-dependent electrical characteristics of ML MoS_2 FETs and their corresponding Schottky barrier characteristics. Statistical analysis provides new insight about the properties of metal contacts on CVD-grown MoS_2 compared to exfoliated samples. Reduced Schottky barrier heights (SBH) are obtained compared to exfoliated flakes, attributed to a defect-induced enhancement in metallization of CVD-grown samples. Moreover, the dependence of SBH on metal work function indicates a reduction in Fermi level pinning compared to exfoliated flakes, moving towards the Schottky–Mott limit. Optical characterization reveals higher defect concentrations in CVD-grown samples supporting a defect-induced metallization enhancement effect consistent with the electrical SBH experiments.

Supplementary material for this article is available online

Keywords: molybdenum disulfide, MoS_2, transition metal dichalcogenides, monolayer, FET, Schottky barrier, Fermi-level pinning

(Some figures may appear in colour only in the online journal)

Introduction

The emergence of graphene, transition metal dichalcogenides (TMD), black phosphorus, and other 2D materials has advanced basic research of monolayer (ML) crystals and has led to significant efforts towards their application in next-generation nanoscale electronic devices [1–8]. Molybdenum disulfide (MoS_2) is one of the most extensively studied TMD semiconductors for use as the active channel material in field-effect transistors (FETs). In addition to having a bandgap, MoS_2 provides unique properties to achieve good electrostatic control and charge transport in FETs at the scaling limit. MoS_2 FETs have been investigated using mechanically exfoliated flakes as well as CVD-grown thin films. Several studies with exfoliated MoS_2 flakes have discussed the significant role of metal contacts (i.e. the metal–semiconductor junction) on FET operation and

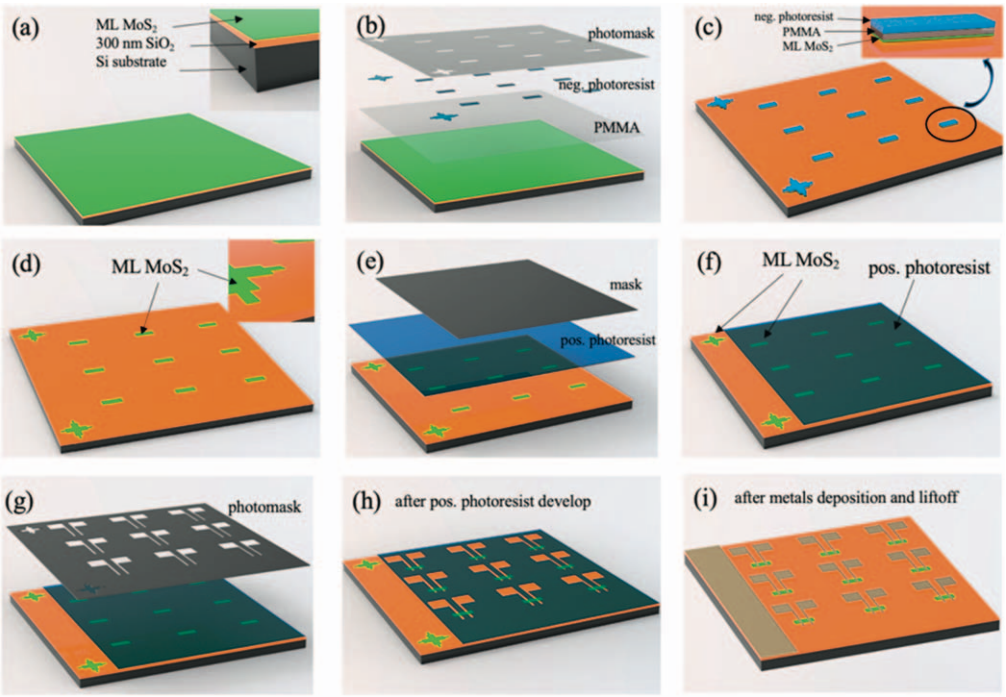

Figure 1. High-yield large-area fabrication process for ML MoS_2 FETs (see Methods in main text).

performance [9–13]. For example, Liu *et al* reported the properties of Ti contacts on exfoliated ML MoS_2, and discussed the importance of Schottky barriers in analyzing device performance [11]. Das *et al* studied the performance of FETs with different metal contacts on multilayered (e.g. 10 nm thick) exfoliated MoS_2 flakes [12]. They explained how the alignment of the Fermi level in the metal contacts with the bottom of the conduction band in the MoS_2 channel reduces the Schottky barrier height (SBH) enabling easier injection of carriers and improvements in on-state current. Moreover, the thickness-dependent and temperature-dependent transport properties in mechanically exfoliated ML and multilayer MoS_2 FETs were also explored extensively [14–18].

Those studies based on exfoliated flakes have demonstrated the potential of MoS_2, but large-area methods for ML MoS_2 are needed for practical and scalable integrated technologies. Thus, CVD-grown MoS_2 coupled with conventional photolithographic patterning techniques must pave the way for more practical applications. Recently, Kwon *et al* pointed out the lack of reports for conventional photolithographic patterning of large-area ML MoS_2 and presented a study of CVD-grown ML MoS_2 FETs [19]. Similarly, Zhang *et al* synthesized and transferred CVD-grown MoS_2 to fabricate and study FETs as a function of number of layers in the MoS_2 channel [20]. In another recent study, Xu *et al* presented results on large arrays of CVD-grown MoS_2 top-gated FETs and compared two-probe versus four-probe measurements of transport parameters [21]. These studies presented statistical analysis of CVD-grown ML MoS_2 FET parameters with histograms of threshold voltage [19–21], mobility [20, 21], and gate hysteresis [19], but did not analyze the effects of Schottky barriers at the contacts as done in previous studies of FETs with exfoliated MoS_2.

In this paper we present an examination of metal contacts on CVD-grown ML MoS_2 by electrical measurements of large FET arrays. Specifically, two large FET arrays with different source/drain metal contacts (Cr/Au and Ti/Au) were fabricated (via large-area photolithography methods) and tested. SBH were extracted based on thermionic emission theory for 2D semiconductors using temperature dependent measurements. Statistically significant extractions reveal a reduction in SBH for CVD-grown ML MoS_2 compared to values extracted from FETs with exfoliated flakes. This reduction in SBH is attributed to an enhancement in the metallization of MoS_2 by hybridization between S and the metal atoms (e.g. Ti) compared to exfoliated flakes due to a larger number of defects in CVD-grown samples [11]. Moreover, the dependence of SBH (Φ_{SB}) on the metal work function (Φ_M) indicates a reduction in Fermi level pinning (FLP) for CVD-grown samples compared to exfoliated ML MoS_2. The FLP factor ($S = |d\Phi_{SB}/d\Phi_M|$) extracted for CVD-grown samples ($S \approx 0.5$) is larger than those reported for exfoliated fakes ($S \approx 0.1$) and closer to the ideal Schottky–Mott limit ($S = 1$). Optical characterization (Raman spectroscopy) indicates a larger concentration of defects in our CVD-grown ML MoS_2 samples compared to exfoliated flakes supporting a defect-induced enhancement in the coupling between the electrodes and the channel consistent with our electrical analysis of SBH.

Methods

The fabrication of large-area ML MoS_2 FET arrays is illustrated in figure 1. Because of weak van der Waals (vdW) interaction between the substrate and the 2D material

monolayer, a strategy is needed to prevent the monolayer from peeling off, which is typically caused by a stronger cross-linking interaction between photoresist and 2D materials after the post-exposure bake in the lithography process. For example, Theofanopoulos *et al* utilized a 30 nm titanium film as sacrificial layer to protect graphene from peeling off during fabrication of devices [22]. In this work we used a PMMA sacrificial layer to prevent peeling of the 2D material monolayer during photolithography processing. A 1 cm-by-1 cm CVD-grown ML MoS_2 on 300 nm SiO_2/Si (figure 1(a)) was ordered from SixCarbon Technology (Shenzhen) and processed directly on the original substrate. A thin PMMA layer (5000 rpm for 30 s; 100 °C for 1 min) and negative photoresist (LOR3A, 5000 rpm for 30 s, 180 °C for 2 min; AZ5214, 4000 rpm for 30 s, 95 °C for 90 s) were spun coat on top. Then, the photomask for patterning the channel regions and aligners were positioned over the substrate. After UV light exposure and post-exposure bake (50 mJ cm^{-2}, 115 °C for 60 s; flood exposure: 150 mJ cm^{-2}, no bake) the negative photoresist was developed by 300MIF for 1 min. After developing, the photomask pattern was transferred into the negative photoresist as shown in figure 1(b). Dry etching was then used to remove the unmasked regions (SF_6: 20 sccm, Ar: 5 sccm, 10 mTorr, 75 W for 2 min), as shown in figure 1(c). Next, the negative photoresist and PMMA were removed by remover PG at 80 °C exposing pristine ML MoS_2 patterns as illustrated in figure 1(d). Subsequently, positive photoresist (LOR3A, 5000 rpm for 30 s, 180 °C for 2 min; AZ3312, 5000 rpm for 30 s, 100 °C for 60 s) was spun coat on the patterned ML MoS_2, and a second photomask was used on the MoS_2 channel regions. After exposure and post-exposure bake (30 mJ cm^{-2}, 110 °C for 60 s), the positive photoresist was developed by 300MIF for 1 min to expose the ML MoS_2 aligners (figure 1(f)). These were then used for the alignment of the source and drain metal contacts (figure 1(g)). After exposure, bake, and develop, the source/drain metal contacts (5 nm Cr/35 nm Au or 5 nm Ti/35 nm Au) were deposited via electron beam evaporation (figure 1(h)). Finally, the liftoff process was performed in Remover PG at 80 ºC. The final image of the fabricated CVD-grown ML MoS_2 FETs array is shown in figure 1(i).

Results

Two separate arrays of ML MoS_2 FETs, each with different type of metal contacts, were fabricated and tested. The starting material is a continuous CVD-grown ML MoS_2 film (see supplementary information figure S1 (available online at stacks.iop.org/NANO/33/225702/mmedia)). Optical images near the edges of the sample reveal large crystal grains as shown in figure 2(a). The AFM image of an MoS_2 crystal grain and the step height measurement are shown in figures 2(b) and (c). A picture of the full FET array sample is shown in figure 2(d), and a micrograph of a single MoS_2 FET is shown in figures 2(e) and (f) (closer view of the FET channel region). To verify the quality and the number of MoS_2 layers we conducted Raman spectroscopy in the channel region of five randomly selected fully fabricated FETs. Figure 2(g) plots the Raman spectra where the first and second peaks, centered at 385 cm^{-1} and 405 cm^{-1} respectively, correspond to the to E_{2g} and A_{1g} modes, which have been demonstrated to be sensitive to the number of MoS_2 layers [23–25]. A difference in the peak positions of $\sim$20 cm^{-1} confirms the monolayer MoS_2 channels. An AFM image of the FET and height measurement across the channel region are shown in figures 2(h) and (i) where the step observed in height includes the MoS_2 ML thickness as well as etching into the SiO_2 substrate.

The fabricated arrays include FETs with various channel widths (W) and lengths (L). Typical drain current (I_d) versus gate voltage (V_g) characteristics measured at different temperatures are shown in figures 3(a) and (b) for FETs with Cr/Au and Ti/Au contacts respectively (more I_d–V_g measurements at different temperatures in supplementary information figure S3). Dual V_g sweeps show negligible hysteresis at all temperatures indicating minor contribution from near interfacial traps and adsorbates on the surface of the MoS_2 channel [26–29] (samples were annealed *in situ* at 375 K under high vacuum $\sim$3E-7 Torr for 24 h, see supplementary information figure S2). For the range of V_g in figures 3(a) and 3(b), I_d goes down with decreasing temperature consistent with charge transport limited by thermionic emission over the Schottky barriers at the interface between metal contacts and the MoS_2 channel. In figure 3(c) we plot I_d at $V_g = 50$ V (normalized by W) as a function of L for both Cr/Au and Ti/Au FETs. These results shown correspond to mean values (symbols) and standard deviation (error bars) from over 20 FETs tested for each L (>100 FETs tested overall). We note that except for a few devices that failed during liftoff in the fabrication process, over 80% of the devices showed good field-effect characteristics (I_d–V_d characteristics were also verified, see supplementary information figures S4 and S5). Further statistical analysis is provided with histograms of important FET electrical parameters for both Cr/Au and Ti/Au devices. These include threshold voltage (figure 3(d)), subthreshold swing (figure 3(e)), and on/off ratio (figure 3(f)). Similar distributions of the parameters are observed for Cr/Au and Ti/Au samples, except for a wider distribution of threshold voltages (V_{th}) in Cr/Au devices. This may be attributed to variation in fixed oxide charge. The Cr/Au and Ti/Au FET arrays were fabricated on different CVD-grown samples on Si/SiO_2 wafers with different distributions of oxide charge. We note that for back-gated FETs with thick SiO_2 gate oxides (300 nm in this case) small changes in fixed oxide charge can lead to large threshold shifts (e.g. a difference of $\sim 7 \times 10^{11}$ cm^{-2} can result in $\sim$10 V shift in threshold voltage). The large values for subthreshold swing (SS) are also due to a having a thick gate dielectric. It is well established in the literature that to achieve a near-ideal SS of 60 mV/dec the effective oxide thickness (EOT) must be scaled down to a few nanometers [30].

The energy band diagrams in figures 3(g)−(i) illustrate the charge transport mechanisms of Schottky-barrier MOSFETs (SB-MOSFETs) similar to the MoS_2 devices reported in this work. The band diagrams are shown for a positive

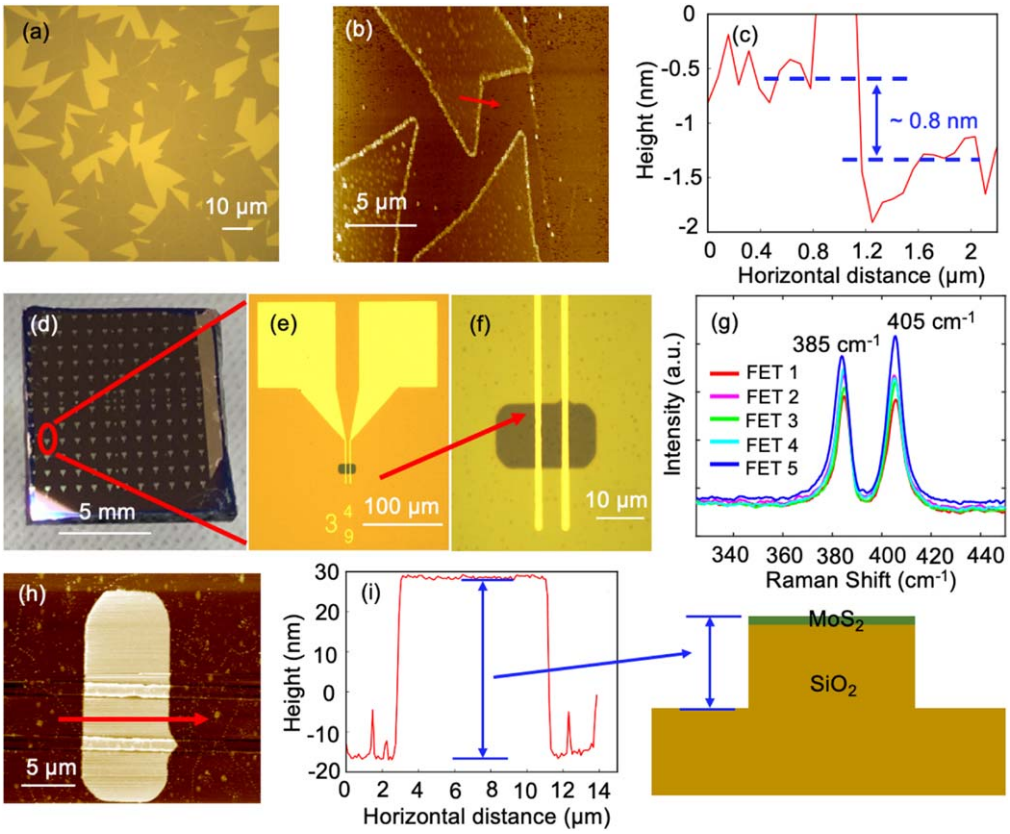

Figure 2. (a) Optical image of the CVD-grown MoS_2 film (image shows edge of mostly uniform film). (b) Atomic force microscopy (AFM) image of CVD-grown MoS_2 film. (c) Line scan on AFM image revels the step height on the CVD-grown MoS_2 film. (d) Picture of one sample showing the large array of MoS_2 FETs. (e) Micrograph of an MoS_2 FET. (f) Higher magnification image of the MoS_2 device. (g) Raman spectrum from the channel region of five different FETs selected randomly. (h) AFM image of the fabricated ML MoS_2 FETs. (i) AFM heigh profile across the channel region of the MoS_2 FET (step includes etching of SiO_2 as illustrated by the schematic).

drain-to-source voltage (V_{ds}) and correspond respectively to biasing conditions with V_g below the flat band voltage (V_{FB}), $V_g = V_{FB}$, and $V_g > V_{FB}$. For $V_g < V_{FB}$ a large (wide) energy barrier between the contacts and the channel limits the injection of carriers to thermionic emission processes. As V_g increases towards V_{FB} the energy bands in the channel are pulled down in energy reducing the barrier height for electron injection from the source into the channel. At the flat band condition ($V_g = V_{FB}$) the energy barrier height for electron injection from source to channel is equivalent to the Schottky barrier (labeled as Φ_{SB}). Further increase in V_g will not change the Schottky barrier height. However, as V_g increases above V_{FB} the barrier becomes triangular its width decreases with increasing V_g. As a result, thermally assisted tunneling of electrons through the barrier sets in for $V_g > V_{FB}$. In a device with good electrostatics, increasing V_g significantly above V_{FB} would result in narrow Schottky barriers that would allow efficient electron tunneling. As explained by Illarionov *et al* [30], strongly scaled insulators enhance gate control over the channel, thereby reducing the impact of the Schottky barriers. When this is true, the limiting charge transport mechanism becomes the scattering effects in the channel rather than thermionic emission at the contacts. When current flow is limited by charge scattering in the channel, the FET mobility can be extracted to characterize the transport properties and quality of the MoS_2 channel. The devices studied in this work do not have strongly scaled insulators (these are back-gated FETs with 300 nm SiO_2 gate dielectrics) so the limiting transport mechanism must be verified.

To better investigate the transport properties in the MoS_2 FETs a subset of the samples was remeasured at different temperatures and sweeping V_g to higher voltages. Figure 4(a) plots the transfer characteristics for several FETs with Cr/Au contacts at different temperatures ranging from 10 K up to 300 K and V_g swept up to 150 V (similar results for FETs with Ti/Au contacts in the supporting information and in figure S6). For a fixed V_g, the temperature dependence of I_d is a good indicator of the limiting charge transport mechanism [31]. I_d increasing with temperature is indicative of thermionic emission (dominated by the contacts), while I_d decreasing with temperature is indicative of scattering (dominated by the channel). In figures 4(b) and (c) we take a closer look at the statistics of I_d temperature dependence. Figure 4(b) plots the scattered data of I_{off} (I_d at $V_g = 50$ V) versus I_{on} (I_d at $V_g = 100$ V) for each temperature (circles). The scattered data shows more overlap in I_{on} compared to I_{off} between the different temperatures. The overlap is more pronounced when plotting the case of I_{on} corresponding to $V_g = 150$ V (triangles). The same trend can be observed by plotting drain current as a function of temperature for different V_g as shown

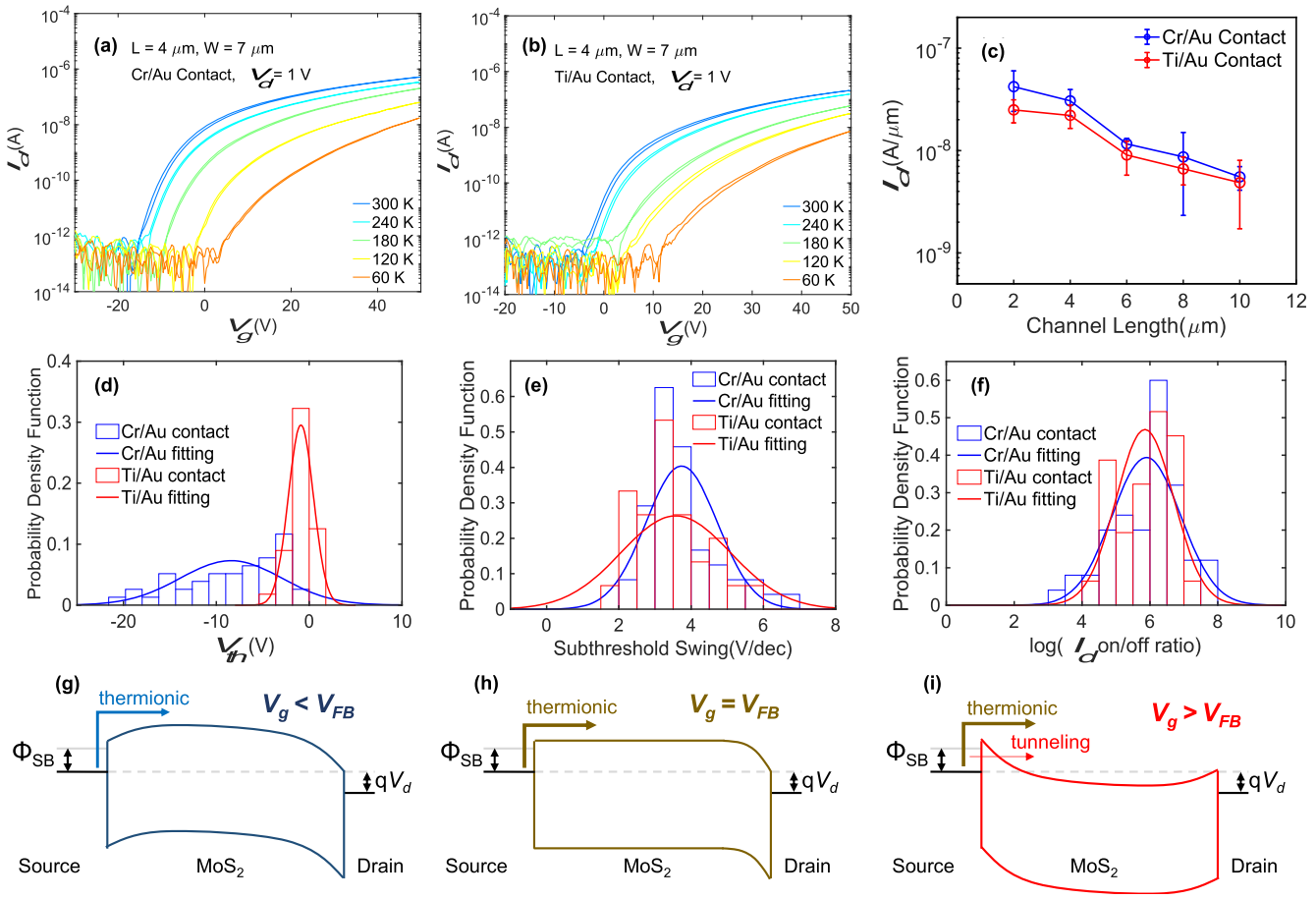

Figure 3. Transfer characteristics at different temperatures for CVD-grown ML MoS_2 FETs with (a) Cr/Au contacts and (b) Ti/Au contacts (both devices have channel width $W = 7$ μm and length $L = 4$ μm). (c) L-dependence of current for Cr/Au and Ti/Au FETs (symbols are mean, error bars are standard deviation from over 100 devices tested). (d)–(f) Histograms of threshold voltage, subthreshold swing, and on/off ratio for both Cr/Au and Ti/Au FETs at room temperature and $V_d = 1$ V (over 100 devices tested). (g)–(i) Energy band diagram for the MoS_2 FETs for biasing conditions corresponding respectively to gate voltage $V_g < V_{FB}$, $V_g = V_{FB}$, and $V_g > V_{FB}$.

in figure 4(c). The top panel is for FETs with Cr/Au contacts, and the bottom panel is for FETs with Ti/Au contacts. At the lower gate voltages I_d clearly increases with temperature (i.e. consistent with thermal activation of carriers). As V_g increases the dependence of I_d begins to transition, but even at $V_g = 150$ V we do not see a full transition (I_d does not decrease with temperature). We conclude that for back-gated FETs with thick gate oxides the gate control over the channel is not sufficient to render the Schottky barriers negligible. Therefore, extractions of mobility are not useful as the transport properties of the FETs are affected by the contacts even for large V_g. Instead, we focus on the properties of the Schottky barriers and metal contacts to the CVD-grown monolayer MoS_2 and compare these to exfoliated MoS_2.

We can perform a statistical analysis of Schottky barrier height (SBH) from the off-state measurements (e.g. for $V_g < 50$ V). Previous works on exfoliated MoS_2 [11, 12, 32] (both monolayer and multilayer) as well as a study on CVD-grown multilayer MoS_2 [33] have reported on the extractions of SBH, but to the best of our knowledge no reports have been published on the statistics of SBH from CVD-grown ML MoS_2 devices. Since density of states, crystallinity, surface roughness, defect density, and other physical properties are different between exfoliated and CVD-grown MoS_2 [20, 31, 34, 35], it is important to analyze the statistics of SBH at the interface between metal contacts (Cr and Ti in this paper) and ML CVD-grown MoS_2. From thermionic emission theory for 2D semiconductors the (reverse-bias) Schottky junction current is given by

$$I = WA_{2D}T^{3/2}\exp(-q\Phi_B/k_BT)[1 - \exp(-qV_{ds}/k_BT)],$$

where W is the channel width, q is the electron charge, k_B is the Boltzmann constant, Φ_B is the barrier height, $A_{2D} = q(8\pi k_B^3 m^*)^{1/2}/h^2$ is the Richardson's constant for 2D [10, 11, 37]. For a fixed V_g we extract I_d at different temperatures as shown in figure 4(d), and construct an Arrhenius plot like the one shown in figure 4(e). Using the thermionic emission current equation, we can extract barrier height as a function of V_g from the slope of the Arrhenius plot. The SBH (Φ_{SB}) corresponds to the barrier extracted at the flat band condition, which can be identified from the plot of extracted barrier height as a function of V_g (figure 4(f)) as the point where the extraction deviates from a linear dependence. In figure 4(f) we show examples of extracted SBHs for MoS_2 FETs with Cr/Au and Ti/Au contacts (more examples in supplementary information figures S7 and S8). The extracted

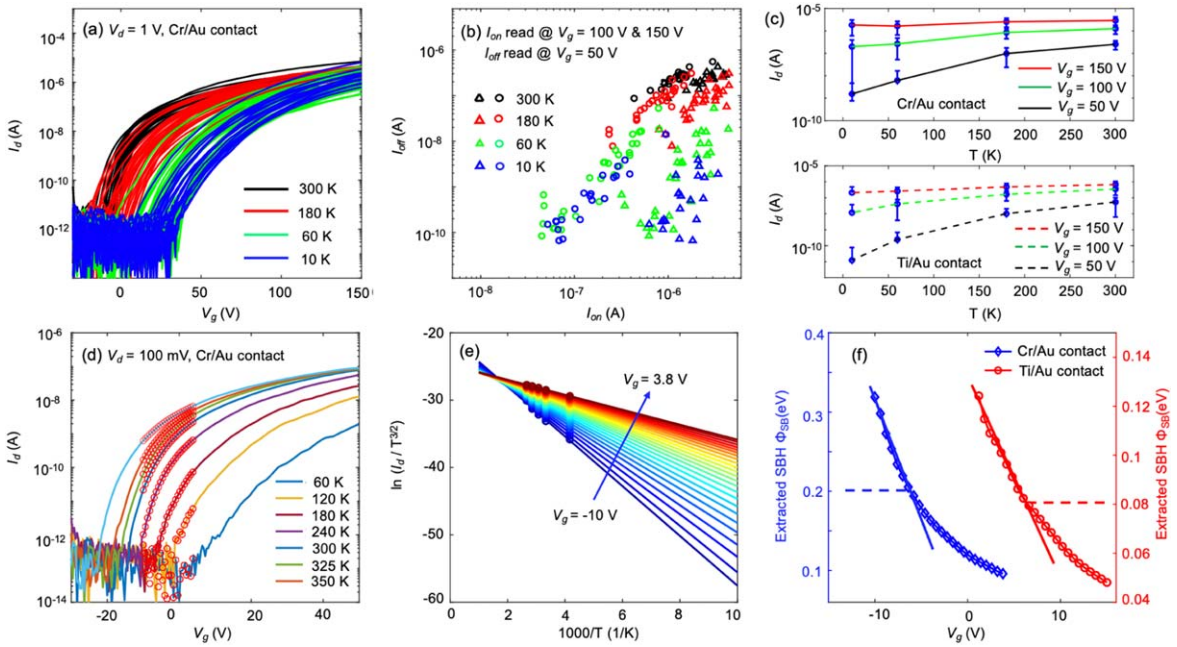

Figure 4. (a) Transfer characteristics for the ML MoS_2 FETs with Cr/Au contacts for $V_d = 1$ V and for different temperatures. (b) Scattered plot for I_{off} (I_d at $V_g = 50$ V) versus I_{on} (circles: I_d at $V_g = 100$ V; triangles: I_d at $V_g = 150$ V). (c) Drain current as a function of temperature for various V_g (circles are mean values, error bars are standard deviations). (d) Example of transfer characteristics used to extract barrier height. (e) Arrhenius plot for extraction of barrier height; (f) barrier height versus V_g, and extractions of Schottky barrier height (dashed lines) for FETs with Cr/Au (diamonds) and Ti/Au (circles) contacts.

SBH is approximately 0.2 eV for the Cr/Au device and 0.08 eV for Ti/Au (statistics in figure 5).

Figure 5(a) plots histograms of extracted SBHs for Cr/Au and Ti/Au devices. The mean and standard deviation of SBH extracted on ML MoS_2 FETs with Cr/Au contacts were respectively $\mu_{Cr} = 0.19$ eV and $\sigma_{Cr} = 0.05$, while for FETs with Ti/Au contacts $\mu_{Ti} = 0.09$ eV and $\sigma_{Ti} = 0.02$. The extracted SBH for Cr contact is higher than that of Ti contact due to the larger work function of Cr. The extracted SBH for CVD-grown ML MoS_2 FETs with Ti/Au contacts in this paper is smaller than those of exfoliated ML MoS_2 FETs reported earlier [11, 38]. A possible explanation is enhancement in metallization of MoS_2 resulting from hybridization between S and the metal atoms (e.g. Ti) compared to exfoliated flakes due to having more lattice defects in CVD-grown samples [11]. In figure 5(b) we plot the extracted SBH for CVD-grown monolayer MoS_2 (this work) as a function of the metal (contact) work function, and compare it against previous works on exfoliated monolayer MoS_2. Interestingly, an improvement (reduction) in FLP is observed for CVD-grown samples compared to exfoliated ML MoS_2. The FLP factor ($S = |d\Phi_{SB}/d\Phi_M|$) for CVD-grown samples ($S \approx 0.5$) is larger than those reported for exfoliated fakes ($S \approx 0.1$) and closer to the ideal Schottky–Mott limit ($S = 1$). The enhanced metallization of CVD-grown MoS_2 likely mitigates the effects of gap (interface) states known to be introduced during material synthesis and/or device fabrication [38, 39]. To confirm the relation between our observations of SBH in CVD-grown versus exfoliated MoS_2 and defect density we use optical characterization. Figure 5(c) plots the room temperature Raman spectra from the channel region of 5 different CVD-grown ML MoS_2 FETs. Firstly, we note that the appearance of a defect-induced peak at $\sim$225 cm^{-1} is not observed in pristine exfoliated samples [36]. Secondly, we extract and plot the full width half maximum (FWHM) for both MoS_2 prominent peaks (E^1_{2g} and A_{1g}). The FWHM are plotted in figure 5(d) and compared against typical results obtained for pristine exfoliated samples. A larger FWHM (broadened peak) indicates a larger defect density. This effect can be attributed to defect assisted broadening around the Gamma symmetry point of the phonon dispersion spectra. As such, increasing defect density leads to broader Raman FWHM. As shown, the CVD-grown ML MoS_2 samples contain a larger defect density compared to exfoliated flakes as evidenced by the larger FWHM. This supports a defect-induced enhancement in metallization of CVD-grown MoS_2, leading to improved coupling between the electrodes and the channel, as a possible explanation for our SBH observations based on the electrical analysis of CVD-grown ML MoS_2 FETs.

We note that the importance of defect on MoS_2 contact properties were studied earlier on exfoliated samples [40]. More recently, Pelella *et al* [41] reported a defect-induced lowering of contact resistance by electron beam irradiation of exfoliated samples, and Chee *et al* [42] reported the metallization of defect-containing CVD-grown MoS_2 using x-ray photoelectric spectroscopy (XPS) leading to reduced SBH and contact resistance.

Conclusion

In this paper we demonstrate a high-yield fabrication process for 2D semiconductors that is compatible with high-throughput

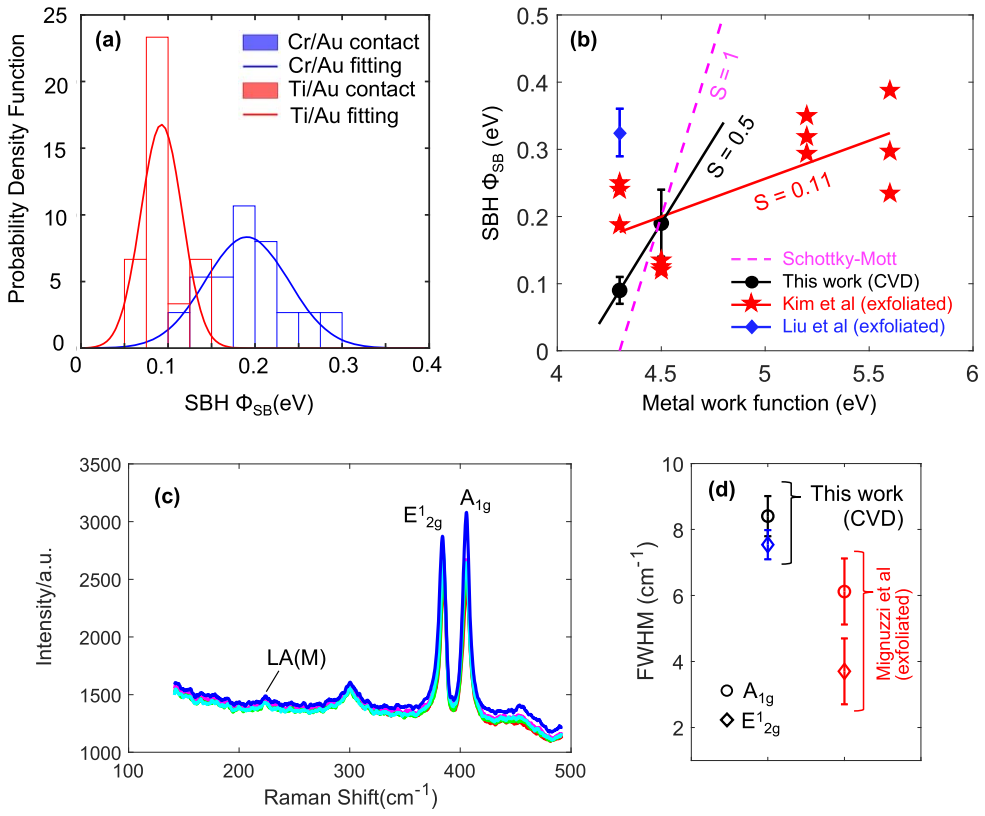

Figure 5. (a) Histograms of extracted SBH for CVD-grown ML MoS_2 FETs with Ti/Au and Cr/Au contacts. (b) SBH plotted as a function of metal work function for CVD-grown ML MoS_2 samples from this work and for exfoliated samples from Kim *et al* [22] and Liu *et al* [11]. (c) Room temperature Raman spectra from the channel region of 5 randomly selected FET samples from this work (d) extracted full width half maximum (FWHM) for both MoS_2 prominent Raman peaks from the CVD-grown ML samples (this work) compared to pristine exfoliated flakes from Mignuzzi *et al* [36].

material synthesis and with wafer-scale fabrication techniques. Based on this process, large-area CVD-grown ML MoS_2 FET arrays with Cr/Au and Ti/Au contacts were fabricated. The devices were inspected by optical images, Raman spectrum, and AFM measurements. In terms of electrical characterization and analysis, a significant advantage of this process is the ability to test multiple device samples and obtain statistics for key FET parameters (e.g. threshold voltage, on/off ratio, subthreshold swing, mobility, and Schottky barrier height). By characterizing the temperature dependence of charge transport in device with two different metal contacts, we were able to statistically verify the significant impact of Schottky barriers at the interface between the metal contacts and the monolayer MoS_2 channel. Our extractions of Schottky barrier heights for devices with Cr/Au and Ti/Au contacts on CVD-grown ML MoS_2 resulted in mean values of 0.19 eV and 0.09 eV respectively. These values are smaller compared to those previously reported on FETs with exfoliated MoS_2 channels, indicating enhancement in metallization of CVD-grown MoS_2 compared to exfoliated flakes due to larger number of lattice defects. Moreover, a reduction in FLP is observed compared to exfoliated samples and indicated better coupling between metals and the channel. While FLP is not eliminated as achieved with exfoliated/transferred van der Waals (vdW) metal–semiconductor junctions, this work provides new valuable insight about metal contacts on large-area MoS_2 processes for next-generation integrated electronic systems based on CVD-grown monolayer 2D semiconductors.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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