Optical direct write of Dolan–Niemeyerbridge junctions for transmon qubits

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ABSTRACT

We characterize highly coherent transmon qubits fabricated with a direct-write photolithography system. Multi-layer evaporation and oxidation allow us to change the critical current density by reducing the effective tunneling area and increasing the barrier thickness. Surface treatments before resist application and again before evaporation result in high-coherence devices. With optimized surface treatments, we achieve energy relaxation T_1 times in excess of 80 μ s for three dimensional transmon qubits with Josephson junction lithographic areas of 2 μ m².

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Transmon qubits are a leading platform employed in noisy intermediate scale quantum processors.^{1–4} The success of these devices has resulted from continued advances in fabrication techniques, with state-of-the-art cm-scale devices incorporating mm-, μ m-, and nmscale features. Typical fabrication utilizes multiple lithography and metalization steps. While Josephson junctions are fabricated at the smallest length scales, particularly to reduce the presence of two-levelsystem (TLS) fluctuators,^{5.6} other circuit elements are fabricated with larger feature sizes to reduce coupling^{7–10} to TLS fluctuators.^{11,12} We now understand that TLS defects primarily reside at substrate–metal, metal–metal, and metal–air interfaces.^{13–19} Careful surface cleaning has vastly improved coherence times.^{20–22}

Fabrication based exclusively on photolithography simplifies processing and reduces the need for multiple lithography steps,²³ decreasing fabrication time and cost and enabling larger scale production. Photolithography has shown consistency and uniformity across wafers, yet it is limited by its relatively large minimum feature size. Although advanced lithography techniques offer workarounds to improve the resolution limit,^{24–27} standard photolithography cannot reliably pattern features as small as typical Josephson junctions (JJs) for qubits, which have features on the scale of 100 nm.

In this Letter, we demonstrate that highly coherent transmon qubits can be fabricated with an all-optical direct-write photolithography system. Direct writing allows fast prototyping by rastering a focused optical beam across a resist-coated substrate. We test two oxidation procedures that both produce appropriate critical currents, despite large overlap areas. First, a multi-step oxidation process creates small-effective-area JJs. Second, a single-step oxidation creates JJs with large effective areas. Transmon qubits with both oxidation procedures exhibit high T_1 times, but our highest observed T_1 times come from single-step-oxidation devices. Moreover, we demonstrate the need for multiple cleaning steps to achieve low loss.

This work joins a growing body of literature studying alternative fabrication techniques for transmon qubits. Other work using photolithography^{23,28} demonstrated modest coherence times, and merged-element transmons have used large overlap areas in compact footprints.^{29,30} Our work extends elements of these studies, using photolithography to make large-overlap-area JJs for highly coherent three-dimensional transmon qubits.

We fabricate large-area JJs with aluminum double-angle-evaporated onto high-resistivity, 100-oriented silicon substrates. Our best devices result from substrate cleaning for 10 min in a 3:1 mixture of sulfuric acid and hydrogen peroxide heated to 120 °C (Piranha etch) followed by a 5-min buffered-oxide etch (BOE). These cleaning steps remove native silicon oxides and residual organics from the silicon surface. 21,22,31,32

We design a bi-layer optical resist stack to support Dolan–Niemeyer-bridge shadow mask evaporation.^{33,34} The bottom layer is a liftoff photoresist (MicroChem LOR 10B). The top layer is a high-resolution imaging photoresist (MicroChem Shipley S1805). We spin and softbake these resists to achieve 1 μ m height in the liftoff resist and 0.6 μ m in the imaging resist, as illustrated in Fig. 1(a). Our recipes are tailored for 1.5 μ m undercuts, but the liftoff photoresist supports undercuts up to 10 μ m.



FIG. 1. Fabrication method for large-area JJs. (a) A sketch of the bi-layer resist stack. The 1.5 μm undercut creates a Dolan bridge to mask double-angle-deposited aluminum. Roman numerals and dashed lines indicate resist coverage depicted in panel (b). (b) An optical image of the post-development resist stack indicates undercut regions. (c) A scanning electron microscope image of two large-area JJs in a SQUID geometry. (d) A multi-layer oxidation process achieves a thick oxide for low critical current JJs. (e) Cross-sectional TEM image of the oxidation stack. (f) Averaged EDXS abundance of aluminum and oxygen. Oxygen in the middle of the aluminum region defines the tunneling barrier.

An all-optical 375 nm direct-write-lithography system (Heidelberg DW 66+) exposes the resists by rastering a focused optical beam across the wafer. Figure 1(b) shows a patterned 1.5 μ m long and 0.8 μ m wide Dolan bridge. The dimensions are chosen to stay above the lithography system's resolution limit. Scanning electron microscope (SEM) imaging shows a typical JJ with an area of 1.5 μ m² [Fig. 1(c)]. These overlap areas are two orders of magnitude larger than JJs fabricated with electron-beam lithography that have areas ~0.01 μ m². We develop exposed resist in a metal-ion-free developer (MicroChem MF-319) and visually confirm the Dolan bridge geometry [Fig. 1(b)].

After the development, we employ oxygen plasma ashing (Plasma Etch PE 50, 20 s, 100 W, O₂ 15 cc/min) to remove any residual resist.³⁵ A 30-s BOE step removes silicon oxides that have grown on the atmosphere-exposed substrate.²² The wafer is rapidly transferred (<5 min) to an ultra-high vacuum (~5 nTorr) environment. The sample remains at low pressure for ~18 h, in order to further remove any adsorbed contaminants. We then evaporate five-nine purity aluminum onto the substrate using the Dolan bridge shadow-mask technique.³³ This evaporation consists of three primary

steps: (i) a 30 nm layer of aluminum is evaporated at 45° relative to the wafer's normal vector at a rate between 0.3 and 1 nm/s; (ii) an oxidation step, detailed below, creates the AlO_x layer for the JJ; (iii) a 60 nm layer of aluminum is evaporated at -45° , forming the JJ.

Achieving low critical currents with large-overlap-area JJs require increasing the oxide thickness. Here, we discuss a multi-step oxidation procedure to grow a sufficiently thick oxide layer, sketched in Fig. 1(d). Below we also present results based on a single oxidation step. The recipe leverages the fast initial growth of thin-film oxides predicted by Cabrera-Mott theory.³⁶ After evaporating the initial 30 nm of aluminum, we grow an oxide film with 99.9% pure oxygen at 4.3 Torr for 300 s. We then evaporate a variable number of 0.5 nm aluminum filler layers at the same evaporation angle, each oxidized under the same conditions. Multiple filler layers are usually needed to achieve suitable JJ resistances.

Cross-sectional transmission electron microscope (TEM) images [Fig. 1(e)] and energy dispersive x-ray spectroscopy (EDXS) indicate a 4.5 nm oxide-barrier thickness for the multi-step oxidation [Fig. 1(f)]. We note that this estimate is only a rough upper bound because of averaging over significant surface roughness. We also note that TEM imaging probes structural rather than electrochemical properties, this ovide barrier is significantly thicker than typical single-layer JJs.^{20,38} After liftoff of sacrificial aluminum in N-methyl-2-pyrrolidone (NMP), we probe samples with a DC voltage to infer the critical current via the Ambegaokar–Baratoff relation.³⁹

We embed two large-area JJs into a SQUID geometry with a shunt capacitor of \sim 60 fF, typical of three-dimensional transmons.⁴⁰ We place the circuit into a copper cavity and cool it in a dilution refrigerator to 10 mK. A solenoid mounted to the cavity exterior generates a DC magnetic field through the SQUID loop to tune the circuit's resonant frequency.

Two-tone spectroscopy is used to characterize the energy structure of the circuit. At high probe power, the probe excites multiphoton transitions. We measure the circuit's anharmonicity and infer the Josephson energy, E_J , and charging energy, E_C from the transmon Hamiltonian. For the devices in this study, the ratio E_J/E_C is between 20 and 70, well within the transmon regime.⁴¹ Despite the ~100-fold increase in junction area, the charging energy of the circuit remains comparable to a circuit containing only small-area junctions. We attribute this to the presence of two JJs, detailed below.

Our oxidation scheme creates two JJs between the electrodes. The first JJ forms at the bottom electrode's side face, whereas the second JJ forms at the top face [Fig. 2(a)]. The two JJs have significantly different participation because of their disparate sizes. Evaporation at $\pm 45^{\circ}$ results in filler layers only contributing to the top-face JJ. The top-face JJ has a large area and is relatively thick, due to the added filler layers. However, the side-face JJ has an area comparable to eBL JJs: its dimensions are 30 nm (the thickness of the bottom electrode) by 1.5 μ m (the length of the Dolan bridge). The side-face JJ is relatively thin, due to the self-limited growth of aluminum oxide.^{36,42,43} Because the normal resistance (and the inductance) of a tunnel barrier scales exponentially with the barrier's thickness,^{20,44–46} the participation of the thick, large-area JJ is ~1%.⁴⁷ The thin, small-area JJ dominates the circuit's inductance.

Room-temperature normal state resistance measurements verify the presence of two JJs. Figure 2(b) displays the normal-state-resistance



FIG. 2. (a) Sketch of the junction formed from metalization and oxidation at different incident angles. When electrodes are evaporated at opposing angles (top, black), filler layers do not contribute to the junction. However, when the electrodes are evaporated from the same direction (bottom, blue), filler layers grow the junction. (b) Normal state resistance of devices with varying number of additional oxide layers (N_{layers}) under two separate evaporation/oxidation processes. When evaporated at $\pm 45^{\circ}$ (black), two junctions form. One junction grows slowly, dominating the net resistance. When evaporated at $\pm 24^{\circ}$ and $\pm 60^{\circ}$ (blue), a single junction of uniform thickness grows, yielding an exponential increase in the tunnel barrier's resistance. Dashed lines indicate fits to either a one-component (blue) or two-component model (black). Error bars indicate standard deviations of ~25 devices made in each batch.

vs the number of additional oxide layers. We observe an initial exponential increase that asymptotes to a steady-state value. The steadystate value results from the self-limited thickness of aluminum oxide.^{36,42,43} The measurements are consistent with a parallelcomponent resistance model [Fig. 2(b)].

To confirm this model, we also characterize the normal state resistance of JJs formed with evaporations on the same side of the Dolan bridge (i.e., with $+24^{\circ}$ and $+60^{\circ}$ instead of $\pm 45^{\circ}$). In this configuration, filler layers cover both top- and side-faces of the bottom electrode, allowing equal growth of both JJs. For this case, Figure 2(b) shows an exponential increase in normal-state resistance with the number of oxide layers, consistent with a single JJ of constantly increasing thickness.⁴⁴

Room temperature resistance measurements also allow us to study the wafer scale uniformity of the fabrication process. Photolithography has demonstrated feature-size repeatability down to less than 2% relative standard deviation.^{23,48,49} For qubit fabrication, careful treatments of every processing step, including lithography, development, ashing, and oxidation, has shown relative standard deviations in resistance of 3.5%.³⁵ For our process, we have optimized to 8% variation in resistance across a 2-in. wafer. We identified non-uniformity of the resist stack as a major source of this variation. In particular, by fabricating 16 junctions within a ~100 × 100 μ m² area and repeating this pattern across the wafer, we separate wafer-scale variation from local repeatability, which exhibited a variation of 5%.

Having demonstrated that these fabrication methods produce normal state resistances indicative of JJs appropriate for transmon qubits, we now turn to measurements of device coherence times, where we study devices JJs fabricated with $\pm 45^{\circ}$ evaporations and either single layer or multi-layer oxidation steps. In Fig. 3(a), we show T_1 measurements for multiple devices fabricated with either (i) no substrate cleaning (besides plasma ashing), (ii) BOE cleaning before spin coating and before evaporation, or (iii) Piranha and BOE cleaning before spin coating and BOE cleaning before evaporation. The Piranha solution's strong reaction to organic materials precludes cleaning of the developed resist stack. We see nearly a fivefold increase in coherence times of devices with multiple cleaning steps compared to devices without cleaning. For devices fabricated under various cleaning procedures, we monitor T_1 over hourslong timescales.^{50,51} Figure 3(b) shows time-stability histograms of T_1 for these devices. Despite increases in T_1 times with cleaning, we observe significant time variability of T_1 , which is a measure of the density of weakly coupled TLS fluctuators,^{51–53} indicating that there are opportunities to further reduce the TLS density and improve T_1 .

We utilize two-tone spectroscopy to probe the transmon frequency as a function of applied flux. The presence of strongly coupled TLS defects results in an avoided crossing in the transmon spectrum [Fig. 3(c)]. Using such measurements, we can directly count the number of strongly coupled TLS defects. For devices with no substrate cleaning, we observe an average of 1 TLS per device, with each device measured over a range ~1 GHz. For 3 out of 4 devices with substrate cleaning, we observed no strongly coupled TLS over a frequency range of ~1 GHz/device. However, the fourth device ($T_1 = 84 \, \mu$ s) with substrate cleaning showed six defects in a 600 MHz range. While substrate cleaning exhibits a clear improvement in average T_1 times, we did not observe a significant change in the average number of strongly coupled TLS fluctuators.

Quarter wave coplanar waveguides (CPWs) were used to minimize sources of loss originating from the materials that were used in transmon qubits in this study. Prior to beginning production of the transmon qubits, microwave CPWs were fabricated to test materials



FIG. 3. (a) T_1 values for different substrate cleaning treatments. Devices represented as red points received no surface cleaning prior to spinning resist. Devices represented as black points were first cleaned with a BOE before spinning and before evaporation. Devices represented as blue points were first cleaned with Piranha, then BOE as above. Circular markers received multiple oxidation layers, and square markers received a single, long oxidation. Dashed lines indicate constant quality factors, $Q = \omega_{01}T_1$, of 2, 1, and 0.1 million (top to bottom). Error bars on select points indicate standard deviations for hours-long repeated measurements, as in panel (b). (b) Histograms of repeated T_1 measurements for each of three cleaning procedures. Measurements are repeated every 30 s over the course of 2 h. Averages of T_1 measurements are indicated for each cleaning method. (c) An example of avoided crossings as a qubit transition frequency comes into resonance with a strongly coupled TLS. The coupling strength is given by the maximal separation, 2 g, as indicated. The qubit is the 14 μ s sample from panel (b) (maximum frequency 5.650 GHz, see the supplementary material).

and fabrication techniques. Native oxide was removed from the Si(100) substrate by a 3-min BOE prior to evaporation of Al.¹⁴ Aluminum films were patterned by selective etching with aluminum etchant type A (Transene Co.) at 50 °C. A vector network analyzer was used to measure the transmission, S_{21} , of CPWs using the same experimental setup, as discussed previously.^{14,54} Resonators were designed⁵⁵ with a center width of 3 μ m and gap of 2 μ m, to maximize TLS interaction with the device.¹³ The internal quality (Q_i) factor, as a function of power, was fit to extract filling-factor-adjusted loss tangent *F* tan δ_{TLS} , where *F* is the filling factor and tan δ_{TLS} is the internal loss tangent of the material where the TLSs are located. Pappas *et al.*⁵⁶ discuss the method for extracting *F* tan δ_{TLS} using a power fit of Q_i in detail. High-power measurements of the evaporated Al resonators yielded a Q_i of over 1.2×10^6 and a lower power Q_i of over 3.0×10^5 . We extract *F* tan $\delta_{TLS} = 2.6 \times 10^{-7}$ from a fit of $1/Q_i$ to the power-sweep data.^{14,56,57}

Quasiparticle tunneling is another dominant loss mechanism in state-of-the-art transmon qubits.^{58–62} Despite our use of infrared-photon filters,^{63,64} our qubits tend to have high effective temperatures (~80 mK), indicating an imperfect high-frequency shielding (see the supplementary material for details on qubit thermometry). However, we observe that removing the shielding and other lossy filters does not significantly affect T_1 times, indicating that quasiparticles do not yet significantly limit these devices.

Our study has focused on characterizing and optimizing the T_1 time of fabricated qubits; however, the coherence time T_2 is also a

critical factor in qubit performance. We have evaluated the Ramsey decay T_2 time for select devices attaining high T_1 times, achieving $T_2^* = 19 \,\mu s$ and $T_2^e = 25 \,\mu s$ under optimized line filtering (see the supplementary material for details on measurement filtering and device parameters). Further improvement of T_2 will likely require better filtering to remove intracavity photons^{65,66} and investigate the role of vortex trapping.^{60,67–70}

We have demonstrated a method for fabricating JJs with large lithographic areas. We have studied coherence of devices based on varying oxidation schemes that achieve suitable critical current densities. One scheme utilizes multiple oxidation deposition steps to create a multi-junction device with small junction areas similar to electronbeam lithography processes, and an alternate scheme utilizes a single long oxidation step. Highest coherence devices utilized a single long oxidation step. With appropriate surface cleaning, devices exhibit long energy decay coherence times. Our work, therefore, demonstrates photolithography as a viable fabrication approach for high-coherence superconducting quantum devices.

See the supplementary material for details about qubit parameters and the measurement setup as well as further information on qubit thermometry.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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