

Low-Energy and CPA-Resistant Adiabatic CMOS/MTJ Logic for IoT Devices

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Abstract—The tremendous growth in the number of Internet of Things (IoT) devices has increased focus on the energy efficiency and security of an IoT device. In this paper, we will present a design level, non-volatile adiabatic architecture for low-energy and Correlation Power Analysis (CPA) resistant IoT devices. IoT devices constructed with CMOS integrated circuits suffer from high dynamic energy and leakage power. To solve this, we look at both adiabatic logic and STT-MTJs (Spin Transfer Torque Magnetic Tunnel Junctions) to reduce both dynamic energy and leakage power. Furthermore, CMOS integrated circuits suffer from side-channel leakage making them insecure against power analysis attacks. We again look to adiabatic logic to design secure circuits with uniform power consumption, thus, defending against power analysis attacks. We have developed a hybrid adiabatic-MTJ architecture using two-phase adiabatic logic. We show that hybrid adiabatic-MTJ circuits are both low energy and secure when compared with CMOS circuits. As a case study, we have constructed one round of PRESENT and have shown energy savings of 64.29% at a frequency of 25 MHz. Furthermore, we have performed a correlation power analysis attack on our proposed design and determined that the key was kept hidden.

Index Terms—Adiabatic Logic, Magnetic Tunnel Junction, Correlation Power Analysis, Side-channel Attacks, Internet of Things (IoT).

I. INTRODUCTION

The age of portable devices has resulted in a sharp upward trend in Internet of Things (IoT) devices. IoT devices are typically battery-operated, and thus the need for energy-efficient processors is high. Furthermore, many IoT devices store and transmit sensitive data and thus the security of IoT devices should not be neglected [1]. In this paper, we look to create a secure device against power analysis attacks without suffering from energy efficiency degradation. To remain secure against power analysis attacks and consume lower energy we look to both non-volatile memory in the form of Spin Transfer Torque Magnetic Tunnel Junction (STT-MTJ) [2] and a low energy design technique known as adiabatic logic.

STT-MTJ has numerous advantages over common memory technologies such as extremely low standby power, non-volatility, easy compatibility with CMOS, and high integration density [3]–[5]. MTJs can be combined with standard CMOS devices to create low-energy circuits [6].

While MTJ based circuits reduce standby power, adiabatic-based circuits can reduce overall energy consumption. Adiabatic logic is an emerging design technique to design low energy and secure circuits. Adiabatic logic recycles energy

from the load capacitor back into the clock generator to reduce energy consumption [7].

When reducing the energy consumption of a device, security should not be neglected. The threat vector of IoT devices continues to grow thus defenses against these attacks should be developed. One such security threat that IoT devices can experience is a class of hardware attacks known as side-channel attacks. Side-channel attacks look to retrieve hidden information through a device's side-channel such as power consumption [8], circuit timing [9], etc. Side-channel attacks are a dangerous threat to device functionality and vital device information such as encryption keys. One particular side-channel attack we will focus on is the Correlation Power Analysis Attack (CPA) [10]. This attack looks to correlate power with bits to retrieve hidden information.

In this paper, we look to combine the emerging technology of STT-MTJs with the emerging design technique of adiabatic logic to design ultra-low energy circuits while also remaining secure against power analysis attacks. To demonstrate energy savings, we have constructed one round of the PRESENT encryption algorithm using our proposed hybrid adiabatic-MTJ architecture [11]. Our simulations show that when compared with CMOS our designs save 64.29% at 25 MHz. To demonstrate secure operations, we also performed a CPA attack on the PRESENT Substitution Box (S-Box). When performing the attack on the CMOS implementation we were able to retrieve the secret encryption key. However, when performing the attack on our hybrid adiabatic-MTJ design we were not able to steal the key thus demonstrating its resilience against CPA attacks.

II. BACKGROUND

A. Magnetic Tunnel Junction

Magnetic Tunnel Junction (MTJ) consists of two ferromagnetic (FM) layers and an oxide layer that serves as a barrier between the two ferromagnetic layers [12]. The magnetization of one of the FM layers is fixed in most circuit applications of MTJs, while the other FM layer is free to take either a parallel or antiparallel magnetization [13]. This can be seen in Figure 2 as the bottom layer of the MTJ is fixed and the top layer is free to take a direction. If the MTJ shows a parallel magnetization (R_P) then it will have lower resistance than when it has an antiparallel magnetization (R_{AP}). [14]. The MTJ structure and two configurations are shown in Figure

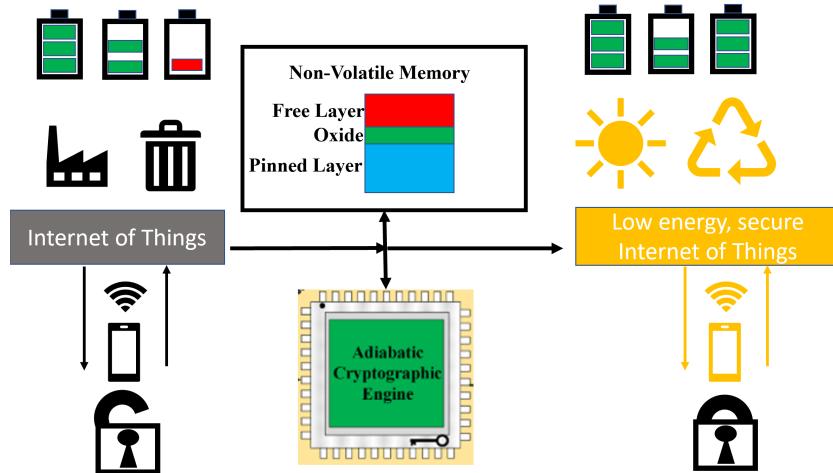


Fig. 1: Hybrid adiabatic-MTJ circuits can introduce a golden age to IoT devices.

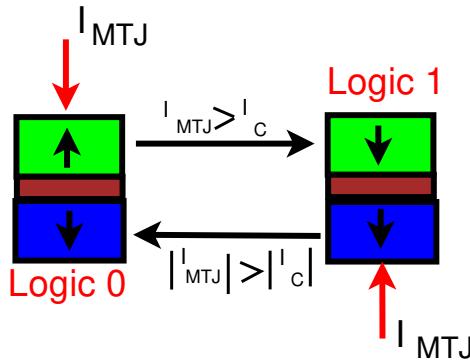


Fig. 2: Structure of Magnetic Tunnel Junction with Spin Transfer Torque (STT) switching.

2. The difference in resistance between the two states of the MTJ devices is given by the tunnel magnetoresistance ratio $TMR = (R_{AP} - R_P)/R_P$. MTJ devices with higher TMR ratios have been shown to have higher reliability [15].

B. CMOS-MTJ Hybrid Circuits

Figure 3 shows the general structure of an existing version of a Logic-In-Memory (LIM) based CMOS-MTJ circuit. The LIM architecture consists of a Pre-Charged Sense Amplifier (PCSA) circuit consisting of MP1, MP2, MN1, and MN2. A dual-rail NMOS only logic tree (T1-T4) evaluates the inputs and the non-volatile MTJs store data. The write circuit is used to switch the MTJs when the respective input is switched.

The operation of the PCSA can be explained through the existing PCSA based CMOS/MTJ XOR gate (Figure 6) [3] [16]. The PCSA, which uses a CLK signal, operates in two phases. The outputs are pre-charged to "1" when CLK is set to "0" and the output voltages begin to discharge to ground when CLK is set to "1". The discharge speed will be different for each branch due to the difference in resistance of the different MTJ configurations (parallel and antiparallel). For

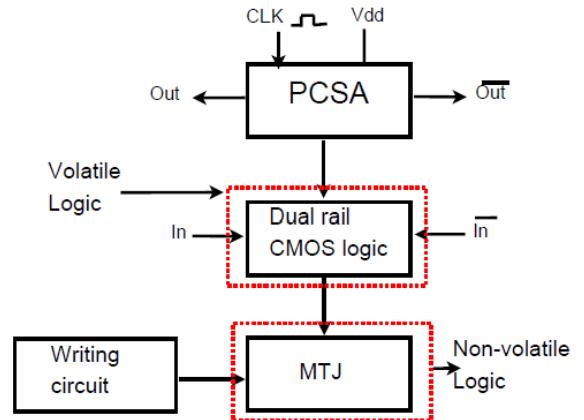


Fig. 3: General structure of Hybrid CMOS-MTJ circuits.

example, if MTJ1 is configured in parallel mode and MTJ2 is configured in antiparallel mode, then $R_{MTJ2} > R_{MTJ1}$. Due to the difference in resistances between R_{MTJ1} and R_{MTJ2} , the discharge current through MTJ1 will be greater than MTJ2. When XOR reaches the threshold voltage of MP1, XNOR will be charged to "1" and XOR will be discharged to "0".

C. Adiabatic Logic

Adiabatic logic is a circuit design technique for designing ultra-low-energy circuits [17]. Adiabatic logic reduces the energy of a circuit by recovering the energy stored in the load capacitor at the end of each clock cycle. The recovered energy is stored either through magnetic energy in clock inductors or through an electric charge in the clock capacitance. The recovered energy is then reused in the next cycle to reduce energy consumption. The energy dissipated in an adiabatic circuit is given by:

$$E_{diss} = \frac{RC}{T} CV_{dd}^2 \quad (1)$$

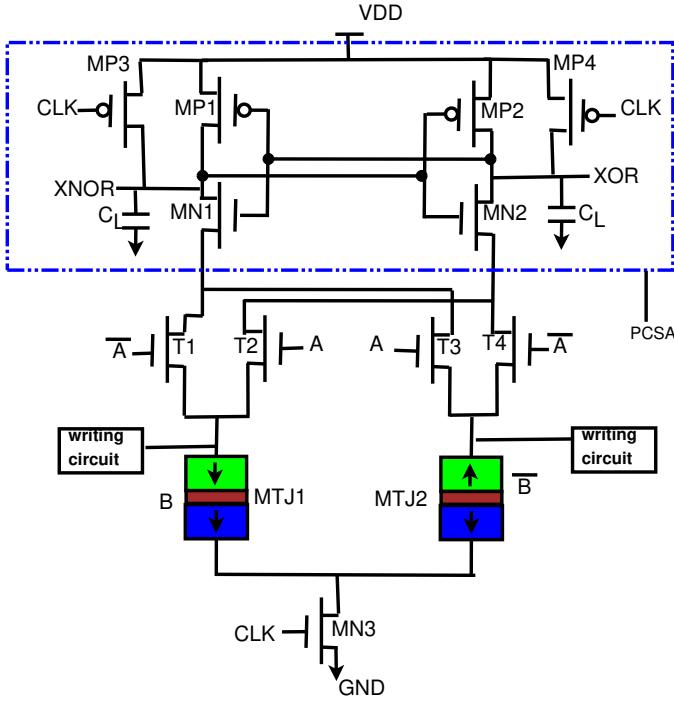


Fig. 4: Hybrid CMOS-MTJ XOR circuit [3] [16].

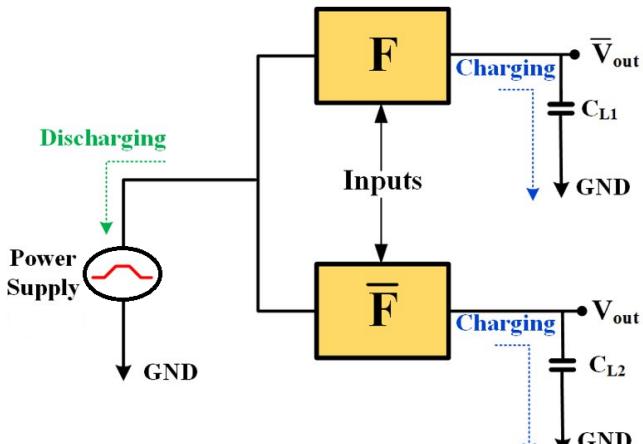


Fig. 5: Adiabatic charging and recovery principle.

Where T is the charging period of the capacitor, C is the output load capacitor, V_{dd} is the full swing of the power clock. If the charging time $T > 2RC$, then the energy dissipated by an adiabatic circuit is less than a conventional CMOS circuit. Figure 5 illustrates the principle of energy recovery within an adiabatic system.

III. PROPOSED SECURE HYBRID ADIABATIC-MTJ CIRCUIT

In this section, we will review the structure of our proposed hybrid adiabatic-MTJ circuit. The proposed XOR/XNOR gate circuit can be seen in Figure 6. We can see that the structure consists of a 2 PMOS and 2 NMOS (2P2N) Pre-Charged

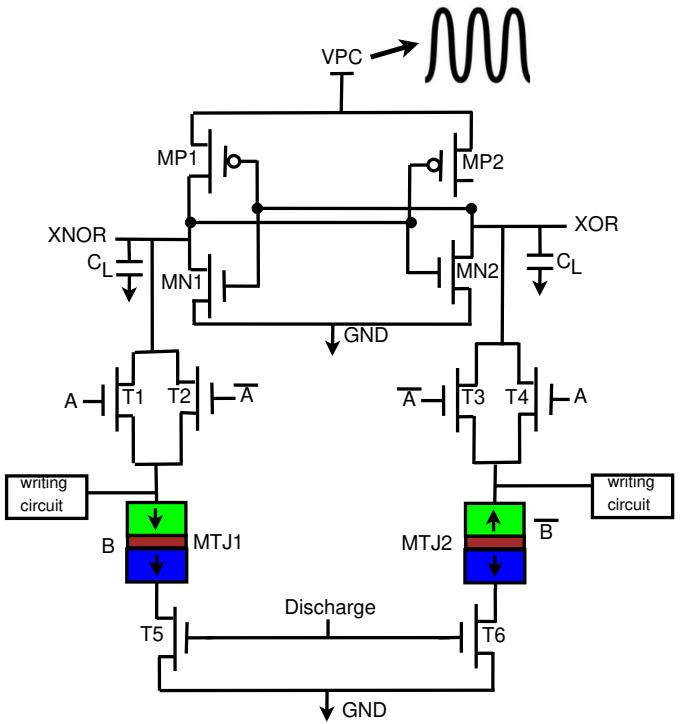


Fig. 6: Proposed low energy and secure adiabatic-MTJ XOR/XNOR gate.

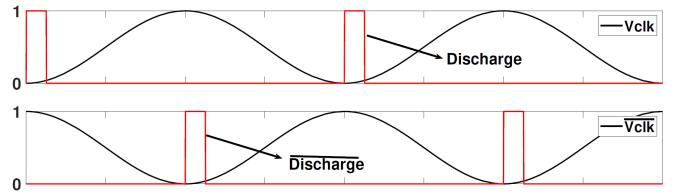


Fig. 7: CPA-resistant two-phase adiabatic logic clocking scheme.

Sense Amplifier (PCSA). There is also a dual-rail evaluation network that consists of only NMOS transistors connected to two MTJs with opposite configurations. Finally, two NMOS transistors are used to discharge the outputs before the next clock cycle begins. Our proposed hybrid adiabatic-MTJ uses a two-phase clocking scheme consisting of two sinusoidal clocks 90° out of phase as well as two discharge signals in phase with the respective clocks. The clocking waveform for two-phase adiabatic logic can be seen in Figure 7.

A. Proposed Hybrid Adiabatic-MTJ PRESENT Implementation

PRESENT [11] is an ultra-lightweight block cipher. PRESENT has low area when compared with other block ciphers which makes it a strong choice for implementation in area constrained IoT devices that look to be resilient against CPA attacks. In this paper, we intend to use the 80-bit version of PRESENT.

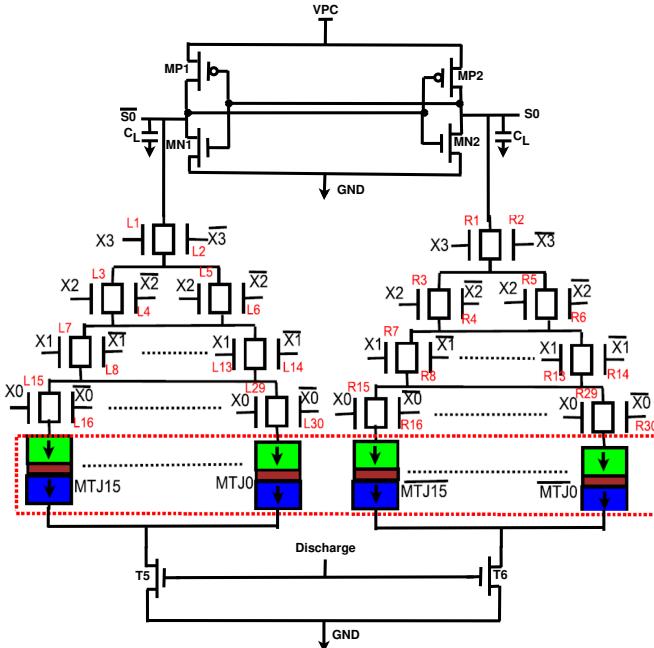


Fig. 8: Proposed hybrid adiabatic-MTJ S-box LUT.

One of the components of PRESENT is the substitution box (S-box) which performs a non-linear substitution. When constructed with CMOS, the S-box consumes high energy and is prone to Correlation Power Analysis Attacks (CPA) thus we look to construct the S-box using our hybrid adiabatic-MTJ circuit. When constructing the S-box circuit using our proposed design we intend to limit the switching of MTJs to reduce energy consumption. To do this, we construct the S-box using a Look-Up-Table (LUT) based method in which the MTJs are written only once so that the output of the S-box is stored within the MTJs. Figure 8 illustrates our proposed S-box.

Another component of PRESENT is the XOR gate. As mentioned previously, MTJ circuits consume high power when there is frequent switching thus the XOR circuit cannot be designed with the proposed adiabatic-MTJ circuit. Instead, we have designed our XOR gate using 2-EE-SPFAL [18]. 2-EE-SPFAL has been shown to be CPA-resistant and low energy which allows the implementation of PRESENT to also be secure and low-energy. The complete implementation of PRESENT can be seen in Figure 10. The XOR gate can be seen in Figure 9.

IV. SIMULATION RESULTS

The simulation results of the proposed hybrid adiabatic-MTJ based circuits are presented in this section. Simulations are performed using Cadence Spectre simulator with 45nm standard CMOS technology with perpendicular anisotropy CoFeB/MgO MTJ model [19]. Because we do not switch our MTJs, we model the device using a basic resistor. The resistance values are calculated based on our MTJ parameters which are listed in Table I.

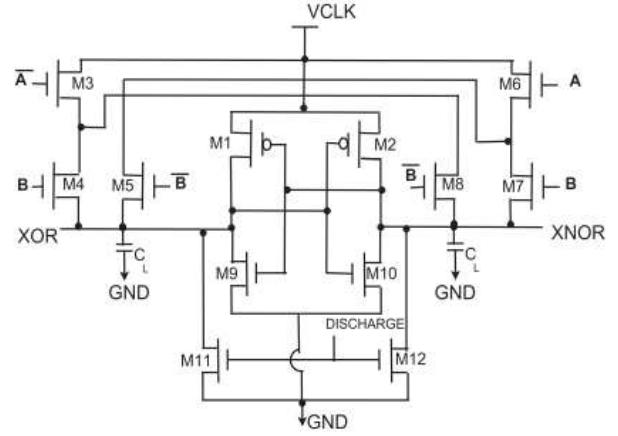


Fig. 9: 2-EE-SPFAL XOR Gate used to implement PRESENT.

TABLE I: NED and NSD values for hybrid adiabatic-MTJ S-box.

Parameter	Description	Value
t_{sl}	Thickness of free layer	1.3nm
a	Length of surface long axis	40nm
b	Width of surface short axis	40nm
t_{ox}	Thickness of the Oxide barrier	0.85nm
TMR	0.Tunnel Magneto Resistance ratio	150%
RA	Resistance Area Product	$5\Omega\mu^2$
Area	MTJ layout surface	40nm x 40nm x $\pi/4$
R_p	Parallel resistance	6.21 k Ω
R_{ap}	Antiparallel resistance	18.64 k Ω

A. Normalized Energy Deviation and Normalized Standard Deviation

The two criteria we will use to evaluate the security of our proposed design are Normalized Energy Deviation and Normalized Standard Deviation. The criteria Normalized Energy Deviation (NED) is defined as $(E_{max} - E_{min})/E_{max}$. NED is used to determine the percent difference between the minimum and maximum energy consumption. A second parameter, Normalized Standard Deviation (NSD), is defined as $\frac{\sigma_e}{\bar{E}}$ where σ_e is the standard deviation of the energy dissipated by the circuit per input transition and \bar{E} is the average energy dissipation. Both NED and NSD are important criteria when determining circuit resilience to CPA attacks. The lower the NED and NSD value the more uniform the power consumption and therefore the more secure a circuit is.

In this paper, we have calculated the NED and NSD values for our proposed S-box. Table II shows the NED and NSD values for our proposed design as well as a standard CMOS-based S-box as a base value to compare. From Table II we can see that our proposed design has lower average energy consumption than the CMOS-based S-box. Furthermore, our proposed S-box has lower NED and NSD values pointing towards its ability to defend against power analysis attacks.

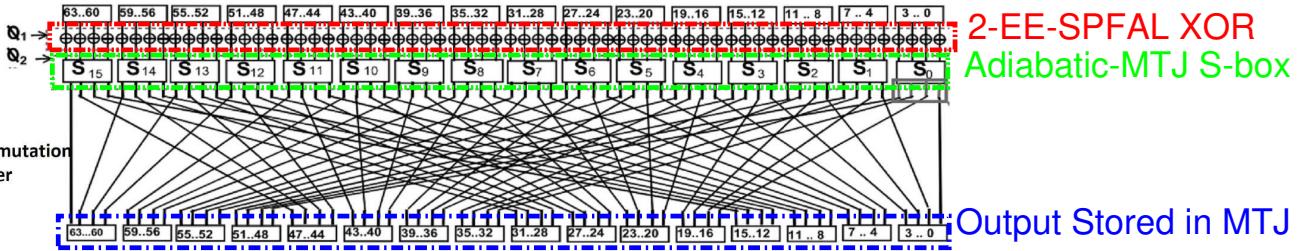


Fig. 10: Complete structure of 1-Round of PRESENT implemented with 2-EE-SPFAL [18] and hybrid Adiabatic-MTJ.

TABLE II: NED and NSD values for hybrid adiabatic-MTJ S-box.

Parameter	Proposed S-box	CMOS
$E_{min}(fJ)$	33.7	7.1
$E_{max}(fJ)$	34.0	102.0
$E_{avg}(fJ)$	33.9	54.8
NED(%)	0.80	93.0
NSD(%)	0.18	42.0

B. Hybrid Adiabatic-MTJ Case Study: 1-Round of PRESENT

A PRESENT S-box implemented with a hybrid adiabatic-MTJ circuit consumes uniform power and is therefore secure against Correlation Power Analysis (CPA) Attacks. Uniform power consumption from 1 round of PRESENT can be seen in Figure 11. The uniform power consumption is an indicator that the circuit is secure against a CPA attack as we will see when one is performed. MTJs are non-volatile memories that store data within the MTJs therefore, as a fair comparison we have added 64 Flip-Flops to the CMOS implementation to synchronize the inputs and store the output. Figure 12 and Table III shows the energy per cycle of the proposed hybrid adiabatic-MTJ circuit and CMOS implementations of 1 round of PRESENT. From Figure 12 and Table III we can see that our proposed design consumes 0.50 pJ/cycle at 5 MHz while the CMOS implementation consumes 0.80 pJ/cycle resulting in a 36.6% reduction in energy. At 50 MHz, our proposed design consumes 0.25 pJ/cycle while the CMOS implementation consumes 0.78 pJ/cycle resulting in a substantial energy reduction of 67.2%.

TABLE III: Energy per cycle of Present-80 implemented with CMOS and hybrid Adiabatic-MTJ

Energy Per Cycle (pJ/Cycle)	5 MHz	10 MHz	12.5 MHz	25 MHz	50 MHz
CMOS	0.80	0.79	0.79	0.78	0.78
Adiabatic-MTJ	0.50	0.37	0.30	0.28	0.25
Energy Reduction (%)	37.6	53.5	61.8	64.2	67.2

C. CPA Attack on PRESENT-80

Previously we have shown our proposed hybrid adiabatic-MTJ based implementation of PRESENT to consume less energy when compared to CMOS. While reducing the energy consumption of a circuit we must also ensure the resilience of a circuit against side-channel attacks. The S-box of PRESENT

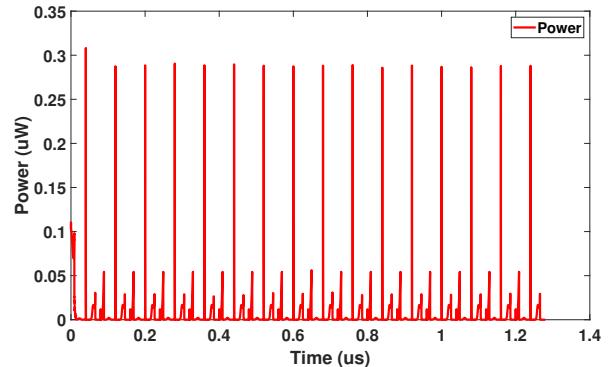


Fig. 11: Proposed hybrid adiabatic-MTJ S-box LUT uniform power consumption.

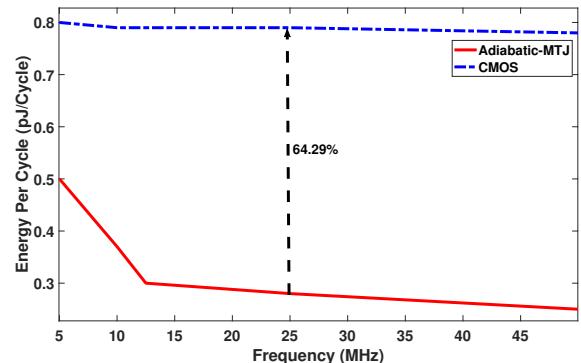
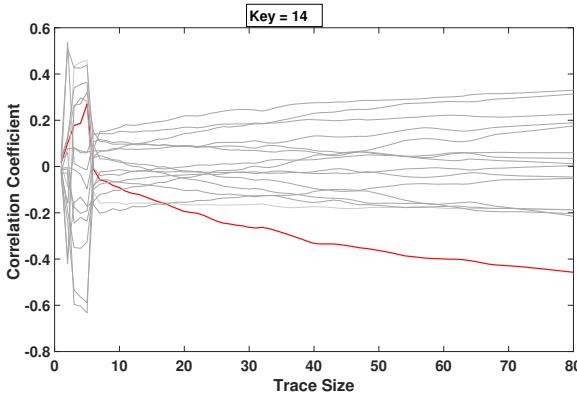
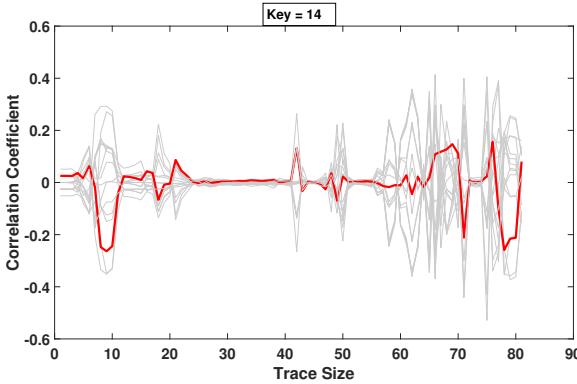


Fig. 12: Energy per cycle of hybrid adiabatic-MTJ and CMOS implementations of PRESENT.

will be the attack point in the Correlation Power Analysis (CPA) attack. The CPA attack is performed by following the steps described in [10]. The simulation was performed at 12.5 MHz with a 10fF load. Practical CPA attacks usually require a large amount of traces to steal encryption keys. However, we are performing a simulation without electrical noise and therefore we require much fewer traces to steal the encryption key. In our attack, we have chosen 80 samples per clock period thus we will sample every 1ns. Using 5120 input traces, we were able to steal the encryption key in the CMOS-based design of PRESENT-80. Figure 13a shows a successful CPA attack on a CMOS implementation of PRESENT-80.



(a) Successful CPA attack on CMOS based implementation of PRESENT S-box.



(b) Unsuccessful CPA Attack on hybrid adiabatic-MTJ based implementation of PRESENT S-box.

Fig. 13: Correlation power analysis performed on both CMOS and hybrid adiabatic-MTJ implementation of PRESENT-80.

While the CMOS key was revealed in 5120 traces, the hybrid adiabatic-MTJ implementation of the PRESENT S-box did not reveal the key in greater than 12,000 traces. Figure 13b shows an unsuccessful CPA attack against the hybrid adiabatic-MTJ implemented PRESENT S-box. This case study demonstrates our circuits resistance against CPA attacks and shows it is a promising candidate to design secure and low-energy IoT devices.

V. CONCLUSION AND FUTURE WORK

A novel hybrid adiabatic-MTJ circuit was presented in this paper. The novel circuit provides substantial energy savings and is also resistant to Correlation Power Analysis Attacks. As a case study, we constructed one round of PRESENT and demonstrated that it consumed lower energy when compared to its CMOS counterpart. Furthermore, we have performed a Correlation Power Analysis Attack on both implementations of the S-box and determined that we could retrieve the key from the CMOS implementation but not from the hybrid adiabatic-MTJ implementation. As future work, a reliability analysis will need to be conducted to determine the usefulness of the circuit under a variety of variations.

ACKNOWLEDGMENT

This work is partially supported by National Science Foundation CAREER Award No. 1845448.

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