A 1.15µW 5.54mm^3 Implant with a Bidirectional Neural Sensor and Stimulator SoC utilizing Bi-Phasic Quasi-static Brain Communication achieving 6kbps-10Mbps Uplink with Compressive Sensing and RO-PUF based Collision Avoidance

Baibhab Chatterjee, Gaurav Kumar K, Mayukh Nath, Shulan Xiao, Nirmoy Modak, Debayan Das, Jayant Krishna and Shreyas Sen
Purdue University, West Lafayette, IN, USA. email: {bchatte, shreyas}@purdue.edu

Abstract

To solve the challenge of powering and communication in a brain implant with low end-end energy loss, we present Bi-Phasic Quasi-static Brain Communication (BP-QBC), achieving < 60dB worst-case channel loss, and ~41X lower power w.r.t. traditional Galvanic body channel communication (G-BCC) at a carrier frequency of 1MHz (~6X lower power than G-BCC at 10MHz) by blocking DC current paths through the brain tissue. An additional 16X improvement in net energy-efficiency (pJ/b) is achieved through compressive sensing (CS), allowing a scalable (6kbps-10Mbps) duty-cycled uplink (UL) from the implant to an external wearable, while reducing the active power consumption to 0.52µW at 10Mbps, i.e. within the range of harvested body-coupled power in the downlink (DL), with externally applied electric currents < 1/5th of ICNIRP safety limits. BP-QBC eliminates the need for sub-cranial interrogators, utilizing quasi-static electrical signals for end-to-end BCC, avoiding transduction losses.

Introduction and Motivation

Traditional brain-machine interfaces (BMIc) with tethered data transmission/powering increases risks of cortical scarring, gliosis, infection, and cerebrospinal fluid (CSF) leakage. Recently, untethered miniaturized wireless neural sensors [1-3] and stimulators [4-6] have been demonstrated with various data/power transmission modalities as shown in Fig. 1. RF [1,7] suffers from increased tissue absorption, requiring large Tx power (0.5W in [1,7] which exceeds ICNIRP safety guidelines [8] by ~10X). Optical (OP) [2] and Ultrasonic (US) [3] telemetry are safer, at the cost of significant loss due to scattering and skull absorption (110dB loss in [3]), requiring a sub-cranial interrogator which needs to be surgically placed, and reduces end-to-end efficiency. Magneto-Electric (ME) [4] methods exhibit low tissue-absorption but has large transduction loss (0.1mT magnetic field, equivalent to ~300kV/m electric field requirement in [4] for iso-energy-density). As an alternative, Fig. 1 describes BP-QBC for communication in a neural implant. The implant can sense and transmit information to a wearable headphone-shaped hub through the UL. The hub sends power and configuration/scan bits to the implant through the DL. Both UL and DL use fully electrical signals to avoid transduction losses (a challenge in OP, US and ME systems). The UL use MHz-GHz narrow-band frequencies to (1) avoid interfering with physiological signals and (2) avoid stimulating the brain tissue with low-frequencies. For traditional G-BCC, the electrodes on the implant are shorted through the low-impedance (~kΩ) tissue/fluids in the body, resulting in high DC power consumption. A DC-blocking capacitor in the signal path for BP-QBC creates a bi-phasic output that eliminates the DC power going into the tissue and maintains ion balance.

System on a Chip (SoC) Architecture and Implementation

The implemented BP-QBC SoC in 65nm CMOS (Fig. 2, top) features (1) a 52pJ/b, duty-cycled, OOK-based scalable UL Tx with on -chip clock, CS and collision avoidance, (2) a 31nW DL Rx to receive system configuration bits and control signals, (3) a 89.2% efficiency (I_{Stim}/I_{DC}) bi-phasic stimulator and (4) a 30-stage RF-rectifier (RR) based energy-harvester [9], capable of generating 1V supply with ~70mV$_p$ input. Dual supply domains are utilized: 0.4V for low-leakage/low-power in always-on timer/controller modules, and 1V for duty-cycled data transmission/stimulation. The SoC uses 1:1000 duty cycling with a 100ms transmit phase (TP) + 100ms stimulation phase (SP) within 100s. Additional modes with 1:100 and 1:10 duty cycling can be configured through DL control bits. A 13nW reference (0.4V, 1V) generator and two 24nW LDOs are used to supply V_{DD} for the SoC, utilizing the energy harvested from an RR. Fig. 3 shows the design details of the building blocks of the SoC. The external C_{STORE} at the output of RR is carefully optimized for a max. data rate (DR) with <<100s charging time and <100mV voltage droop during TP/SP. A 17nW charge pump generates 1.8V V_{PUMP} to bias the power gates (on the supply of the duty-cycled modules) in deep-subthreshold during off-state to reduce leakage by 500X (from 0.51µW to 1nW). A ring-oscillator based Physical Un-clonable Function (RO-PUF) with a 9b-PRBS ensures that different nodes within the brain enters TP/SP in staggered timeslots, thereby enabling collision avoidance without a MAC layer. A wake-up based CS front end reduces the Tx DR, resulting in an average duty-cycled power of 1.15µW (0.52µW without leakage), at 10Mbps with CS. This results in a *>60X improvement in energy-efficiency (pJ/b)* as compared to the narrowband state-of-the-art BMIc [2]. The CS module is equipped with an on-chip 2-stage DWT-based sparsifier and dual varying-seed-PRBS sensing-matrix generator, to compress both sparse and non-sparse signals with varying compression factor (CF) from 5X to 33.33X. The BMIc Node DL Rx consists a 10.1nW Front-End (FE) amplifier, a 3.2nW 4-stage passive envelope detector and a 16.2nW fully digital oversampled CDR. The model for the BMIc channel transfer function (TF) is developed analytically from dipole coupling theory and is verified with Finite Element method (FEM)-based simulations as well as IC-measurements using the implemented SoC, which enables *realistic BCC-based BMIc channel measurements for the first time* because of its small form-factor (node volume < 6mm^3).

Measurement Results

Fig. 4(a) shows the Power consumption of the Tx over 42kHz-1GHz and compares with traditional G-BCC measurements. At a nominal quasi-static frequency of 1MHz, BP-QBC offers 41X lower power than G-BCC. Fig. 4(a) also shows the randomized time slots for duty-cycled TP/SP, along with the time-domain stimulation waveforms in a 0.9% phosphate buffered saline (PBS) solution. The measurements with CS are shown in Fig. 4(b). For CF=33.33X, the 10Mbps TP power reduces from 7.23mW to 217µW, while consuming additional computation power of 212µW, resulting in overall power reduction of ~16X. The memory requirement is also reduced by >10X as compared to a 'store and send' scenario. EEG waveforms from GigaScience database are passed through the CS (CF=33.33X), and are reconstructed in MATLAB. In Fig. 5(a), the power consumption of the DL Rx is plotted w.r.t. the DR, showing an energy efficiency of < 35pJ/b at 1kbps. The charging of the C_{STORE} w.r.t. the DL input signal amplitude shows a minimum input voltage requirement of 70mV$_p$ for charging up to 1.2V. The In-vitro setup for BP-QBC channel TF measurement is shown in Fig. 5(b). Brain slices from the C57BL/6J Mouse strain are used, adhering to the overseeing Animal Care and Use Committee guidelines. 500µm-2mm thick slices are placed in a measurement dish containing artificial CSF saturated with carbogen (95% O_2+5% CO_2). Two electrodes (signal+ref) are placed on the surface of the brain slice. The Rx electrodes are placed at a distance (L) from the Tx electrodes. The experiments are repeated with PBS in a PET container with similar dimensions as that of the human skull (diameter~110mm). The channel TF shown in Fig. 5(b) exhibits a loss of ~20dB for the mouse brain and ~60dB in PBS with human-brain sized dimensions. Fig. 6 compares the SoC performance with state-of-the-art BMIc telemetry/stimulators, exhibiting (1) highest DR (3000X improvement vs. [2]) for narrowband BMIc, (2) max. channel length with (3) lowest always-on power and (4) lowest end-to-end loss (>20 dB better than prior art) due to *fully-electrical quasi-static signaling*, while demonstrating the *first BP-QBC link* with *simultaneous powering, communication, CS and stimulation*.

References

[1] J. Lee, *NER* 2019, pp.871. [2] J. Lim, *ISSCC* 2020, pp.416. [3] M. Ghanbari, *ISSCC* 2019, pp.284. [4] Z. Yu, *ISSCC* 2020, pp.510. [5] Y. Jia, *ISSCC* 2018, pp.468. [6] Y. Lo, *ISSCC* 2016, pp.382. [7] J. Lee, bioRxiv, 2020, 2020.09.11.293829. [8] ICNIRP Guidelines 2020. [9] N. Roberts, *ISSCC* 2016, pp.450.

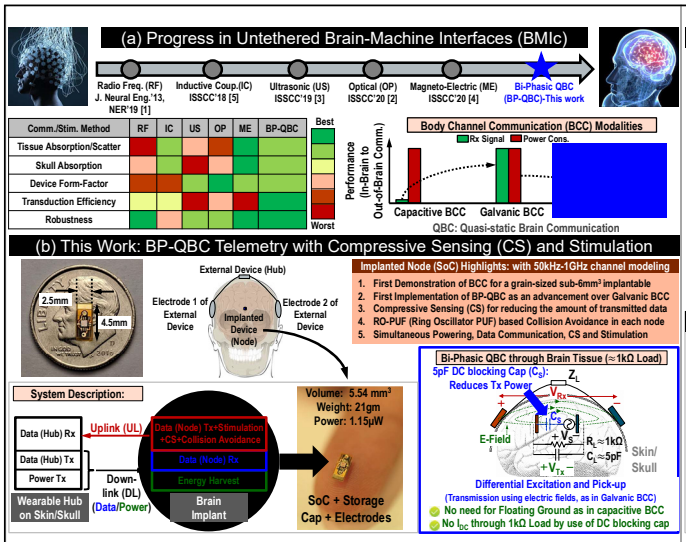

Fig.1: Bi-Phasic Quasi-static Brain Communication (BP-QBC): (a) Motivation and comparison with alternative technologies, (b) SoC Node Implementation for BP-QBC (R_L and C_L in the bottom right figure represent loading due to Brain Tissue on Tx). The 5pF DC blocking cap (C_S) in BP-QBC eliminates any DC current going into the load.

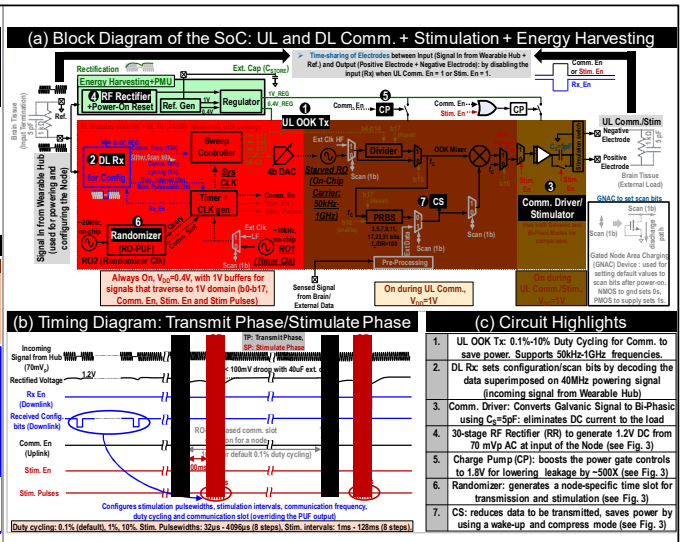

Fig.2: (a) System-level Block Diagram with (b)Timing waveforms and (c) Circuit-level highlights of the BP-QBC SoC. Once the C_{STORE} at the energy harvester is charged to 1-1.2V, the SoC can start bi-phasic comm. (MHz-GHz) and stim. (Hz-kHz pulses) for 100ms within a 100s period. GNACs are used to set default configurations at power-on.

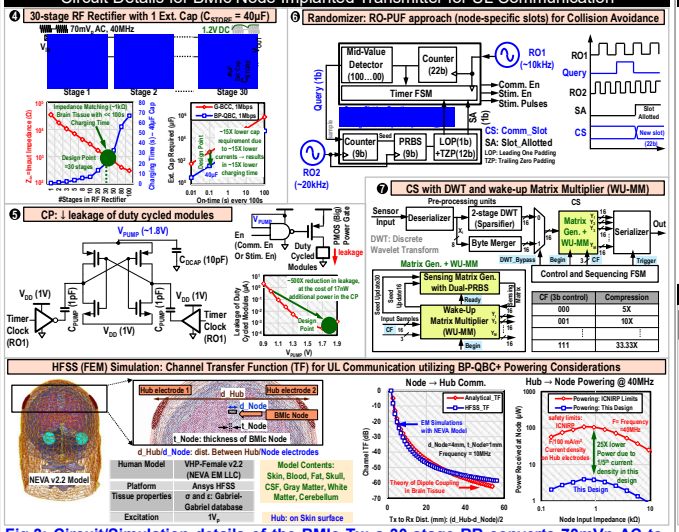

Fig.3: Circuit/Simulation details of the BMIc Tx: a 30-stage RR converts 70mVp AC to 1.2V DC. Design considerations (number of stages, output cap) are also shown. A CP reduces leakage power, and a Randomizer performs RO-PUF based transmit slot selection for collision avoidance. HFSS (FEM) simulations show channel loss < 60dB.

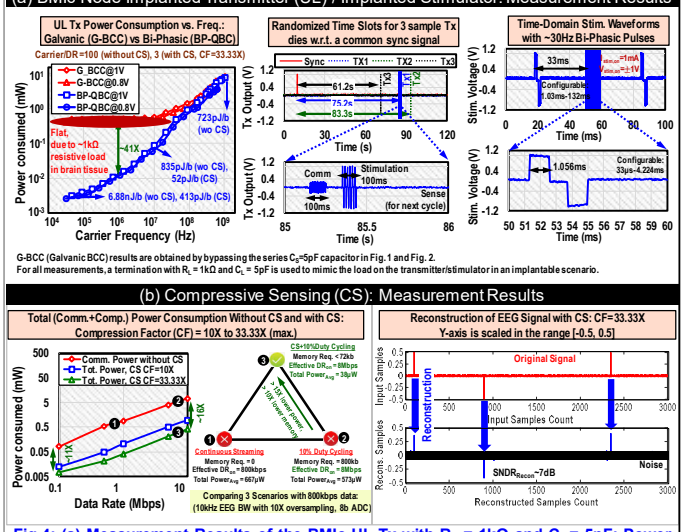

Fig.4: (a) Measurement Results of the BMIc UL Tx with R_L = 1kΩ and C_L = 5pF: Power consumption, Randomizer operation showing 3 different nodes transmitting at different time-slots, and bi-phasic stimulation waveforms, (b) Measurement results with ~16X transmit power reduction due to CS, with reconstruction of EEG waveforms.

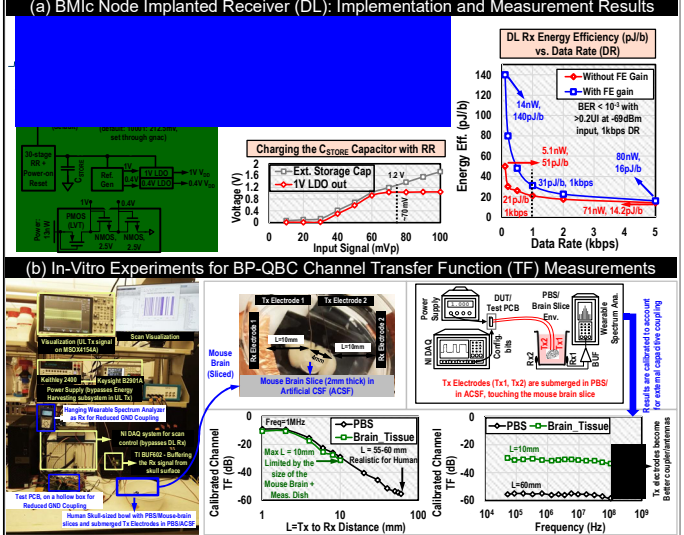

Fig.5: (a) Measurement Results of the BMIc DL Rx with input termination of R_L = 1kΩ and C_L = 5pF : energy efficiency and LDO output, (b) In-Vitro experimental setup for channel TF measurement in PBS and Mouse Brain Slice. Effect of large ground plate (table-top measurements with large setup) and capacitive coupling is calibrated out.

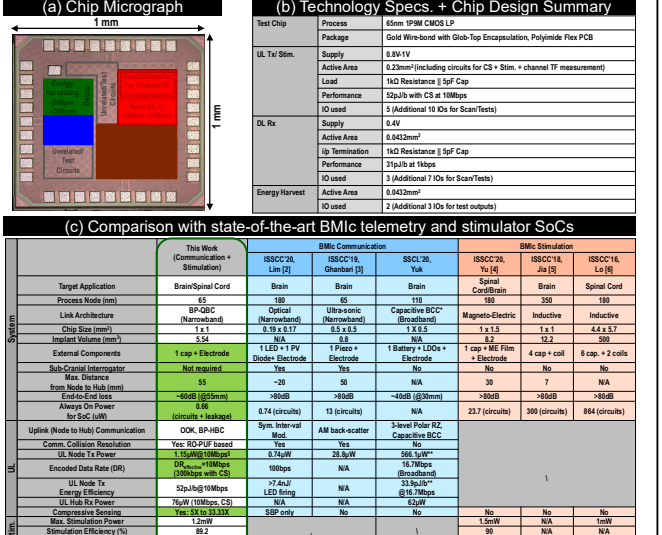

Fig.6: (a) Chip Micrograph, (b) Tech. Specs + Design Summary, (c) Comparison Table.