

Suggesting Hybrid HB and Three-Quarter-Bridge MMC-Based HVDC Systems: Protection and Synchronous Stability under DC Faults

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Abstract— The HVDC systems have been employing modular multilevel converters (MMC) due to their unique high voltage high power potential. However, the lack of fault ride-through capability imposes restrictions on MMCs that are based on half-bridge (HB) modules. Since it is necessary to limit the fault currents to protect MMCs from serious short circuit faults against pole-to-pole DC fault, several protection schemes have been introduced to deal with the DC short circuit faults. This paper proposes a new hybrid MMC protective topology consisting of a combination of the HB and three-quarter-bridge (TQB) modules. The TQB behaves like an HB under normal operation and has low power losses compared to other protective topologies. Modulation and control of this configuration are like HB-based MMC. In the proposed hybrid protective topology, during a pole to pole DC fault, the fault current can be either blocked or be limited by TQB-SMs. Both simulations and experiments were performed to verify the operation of the suggested hybrid MMC in different modes of operation.

Index Terms— DC Fault, Fault-tolerant, HVDC, MMC, nonpermanent Fault, Protection, TQB.

I. INTRODUCTION

HVDC transmission systems improve the efficiency of long transmission lines. Both sending-end station (rectifying converter) and receiving-end station (inverting converter) enable HVDC systems connection of AC grids with different frequencies (50Hz to 60Hz or vice versa) as well. This can increase the grid's stability and prevent cascading failures [1], [2]. The first HVDC system was based on Line-Commutated Converters (LCC), transmitting large amounts of electrical power, blocking current during DC short-circuit fault. The disadvantages of this type of converter are low controllability and high THD.

With the development of power electronic devices, Voltage Source Converters (VSC) has been used in high voltage applications, capable of independently control active and reactive power [3]. Therefore, they increase the power transfer capacity and the stability of the grid. As these converters' switching frequency is much higher than thyristor-controlled converters, a smaller AC side filter is required [4]. One major disadvantage of these converters is their vulnerability to DC

short-circuit fault.

Different topologies of high power VSCs could potentially be used in HVDC systems. Modular Multilevel Converters (MMCs) have better voltage quality than two-level and three-level inverters, which reduce the output filter size or even remove it. Among various multilevel converter topologies, MMC is an attractive topology for HVDC systems [5]. In addition to modularity, these converters' distinct advantage is their ability to deliver low THD high voltages. Switches with a low nominal rating and low switching frequency can also be used to build this high voltage converter [6]. Therefore, the modules' scalability and modularity make them suitable for high voltage levels [7],[8].

One major limitation for the MMC with Half-Bridge Sub-Modules (HBSM) is their vulnerability to DC short-circuit fault. Conventional HB-MMC acts as an uncontrolled rectifier during a DC link fault after blocking IGBTs. This makes the AC grid flows excessive current through freewheeling diodes to the DC fault location, damaging the switch modules. Even if the fault is nonpermanent, the fault current will not be cleared until the AC breakers are opened because the arc created in the DC section cannot be eliminated. It also takes about 10 seconds to restart the system by opening the AC breakers [9]. This causes a prolonged interruption (about 500 cycles) in the system, which is not desirable.

It is also common to parallel-connect a single thyristor across the AC port of each HBSM of the MMC converter [10]. When a DC fault occurs, all switches are blocked, and thyristors are activated simultaneously [11]. While this protects the freewheeling diodes against the fault current, it does not block the fault current which is injected from AC-side. In [10], another protection scheme against DC fault is proposed in which the back-to-back thyristors can eliminate the freewheeling diode effect, allowing the DC-link current to freely decay to zero [10]. This method is raised for protecting nonpermanent faults, as mentioned earlier. Other methods of DC fault protection using different SM topologies such as Full-Bridge SM (FBSM) [12], Clamp Double SM (CDSM) [13], Lattice Modular Multilevel Converter (LMMC) [14], Switched-Capacitor Sub-Module (SCSM) [15], unipolar-voltage full-bridge sub-module (UFBSM) [16], and other

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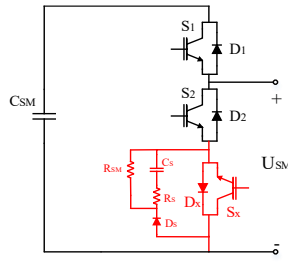


Fig. 2. Proposed TQB-SM for protecting against DC Fault.

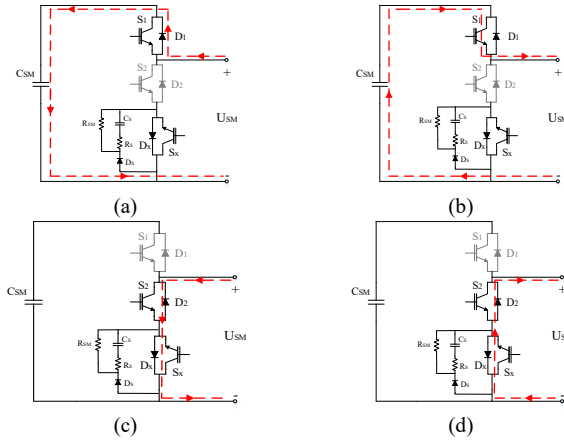


Fig. 3. The current direction of the TQB during normal operation, (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

III. DC FAULT BLOCKING MODE

The TQB uses a capacitor and a diode during the protection mode against the DC fault. Once a DC fault occurs, a capacitor with a much lower capacity than the SM capacitor (almost 5% SM capacitor) is used to prevent the current injection from the AC grid to the fault location; the diode is also used to prevent circulating current between the MMC phases. The DC faults are classified as pole-to-pole and pole-to-ground, whereas the pole-to-pole fault is considered the most severe scenario. Therefore, the DC fault blocking mechanism theory is studied under such a condition. For the pole-to-pole DC fault analysis, two stages are considered as follows:

First Stage. SM capacitor discharging mode: When a pole-to-pole DC fault occurs, the proposed MMC is still under normal operation, and TQB-HB switches are normally switched on/off. As a result, several SM capacitors (SMs with non-zero output) and diodes (SMs with zero output) are in the fault path and got discharged, as shown by the equivalent circuit in Fig. 4. In this stage, the fault current increases dramatically and can cause damage to switches and other equipment if its path is not interrupted.

Second Stage. Protection mode: As soon as the DC fault is detected, all IGBT modules are turned off, where TQB modules charge their capacitors (C_s) in blocking mode. The current path is illustrated in Fig. 5 in this stage. When the current direction is negative, as shown in Fig. 5(a), the third switch's designed RCD circuit is activated, and its capacitor (C_s) is charged through D_s . Since in this design, C_s is much smaller than C_{SM} , so it is charged quickly and provides reverse voltage to block the fault current. The diode D_s is also used to prevent circulating current between the MMC phases. It

should be noted that fault path resistance also plays a vital role in C_s charging time constant. Also, if the current direction is positive, as shown in Fig. 5 (b), the current path is closed through D_1 and C_{SM} , and the voltage of C_{SM} provides the reverse voltage to block the fault current.

Since the proposed MMC topology includes both HB and TQB, let us assume n capacitors (C_s) are in series during the protection mode due to in fault path, two arms are in the fault current path. The fault current path in the three-phase model is illustrated in Fig. 6 (a). Each phase is modeled with a capacitor, diode, and a resistor connected in series. Assuming the capacitors' voltages are equal, the equivalent capacitance in each arm is calculated as below. This circuit is the path of charging the capacitors by fault current.

$$C_{seq} = C_s / n \quad (1)$$

$$R_{seq} = nR_s + R_{fault} + 2R_o \quad (2)$$

During the blocking mode, the fault current charges C_{seq} . Finally, each arm's reverse voltage is equal to $U_{inv} = n/2 \times U_{CS}$, which causes the fault current decay to zero. Fig. 6 (b) shows the equivalent circuit of such a mode of operation. The second-order equation of the RLC circuit applying KVL is as follows. These equations hold if $0 < \omega t < \pi$.

$$\frac{d^2 u_{cs}}{dt^2} + \frac{R_{eq}}{L_{eq}} \frac{du_{cs}}{dt} + \frac{1}{L_{eq} C_{eq}} u_{cs} = 0 \quad (3)$$

$$u_{cs} = K e^{s_1 t} - K e^{s_2 t} + \frac{K'}{\omega C_{eq}} \cos(\omega t + \beta) \quad (4)$$

$$i_f = K C_{eq} S_1 e^{s_1 t} - K C_{eq} S_2 e^{s_2 t} - K' \sin(\omega t + \beta) \quad (5)$$

$$\left\{ \begin{array}{l} K = \frac{I_f}{2\sqrt{\alpha^2 - \omega_0^2}} \\ K' = \frac{V_m}{\sqrt{R_{eq}^2 + \left(\frac{\omega^2 L_{eq} C_{eq} - 1}{\omega C_{eq}}\right)^2}} \\ s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \\ \beta = \arctan\left(\frac{\omega^2 L_{eq} C_{eq} - 1}{R_{eq} \omega C_{eq}}\right) \\ \alpha = \frac{R_{eq}}{2L_{eq}} \\ \omega_0^2 = \frac{1}{L_{eq} C_{eq}} \end{array} \right. \quad (6)$$

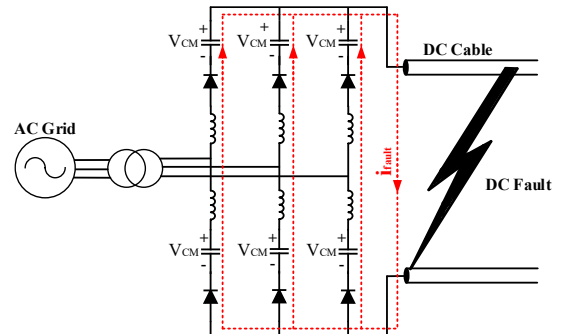


Fig. 4. Fault current crossing path during first stage.

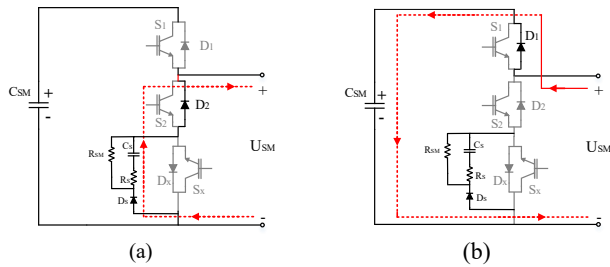


Fig. 5. Current crossing path during fault mode, (a) Mode 1, (b) Mode 2.

Where I_f represents the fault current in the blocking mode, and R_{eq} is the equivalent of series resistance during a fault condition, L_{eq} is the equivalent inductance of the DC transmission cable and arm inductance, C_{eq} equivalent capacitance of RCD which is in series during the fault. Except for the paths listed above, it is possible to feed the fault through the AC grid under certain circumstances. After blocking the switches as mentioned, the fault current charges the RCD capacitors; since the total voltage across the capacitors is higher than the maximum AC voltage, the diodes are in reverse bias, and the current path from the AC grid to the fault location is blocked.

By omitting the fault detection time and protection, the time required for nonpermanent fault resolution is approximately 150 ms to 500 ms. There are two ways to reduce the fault blocking process time as follows:

- In the TQB-SM, as discussed above, the initial fault current charges the capacitors as soon as the switches are blocked and eventually blocks the fault current. Hence, if the capacitors' values are small enough, it causes the capacitor charging time to be reduced; the capacitors can charge faster and block the fault current quicker.
- Another way to reduce the blocking time is to design a separate charger circuit for the capacitors. Therefore, as soon as the fault is detected and the protection is applied, the fully charged capacitors are placed in the current path, and immediately the current becomes zero.

IV. FAULT CURRENT LIMITER MODE

In the previous section, the DC fault blocking mode was discussed; so, the blocking mode prevents transferring power from the AC grid to the fault location, leading to frequency deviations in the AC grid that might increase frequency instability risk. As previously mentioned, the basis of operation in blocking mode is such that the capacitor always remained fully charged during the fault condition and be discharged in post fault condition slowly. This approach is appropriate for the HVDC system's inverter station but is not a proper solution for the rectifier station of the HVDC system. Due to the power transmitted outage from the AC grid, cutting off AC grid current may cause instability on the AC grid during nonpermanent and permanent DC fault while it is undesirable. For solving this problem at a rectifier station that receives its power from the AC grid, this topology has the flexibility to turn to fault current limiting instead of blocking it. For applying fault current limiter mode in rectifier station instead of blocking S_x , it should be switched on/off at a specified frequency and

constant duty cycle (50%). In this mode, half of the number of S_x switches of TQB-SMs should be turned on at any time in each phase, and the rest of the half S_x switches should be turned off. This type of switching provides a discharge path for C_s during fault to avoid getting fully charged. Consequently, the fault current is not disconnected but is limited. Fig. 7 illustrates the variation of I_{fault} versus C_{sm} and R_{sm} values. By decreasing the size of C_{sm} , the rate of limiting current increases, and power losses of R_{sm} reduces; consequently, there is no need for an extra cooling system for these resistors. Fig. 8 shows the fault current path in one cycle. As can be seen, when S_x is on, D_s is in reverse bias and preventing circulating current between the MMC phases and discharging the capacitor at its parallel resistance.

As soon as the DC fault is detected in this mode, all IGBT modules are turned off, and S_x switches are switched on/off. Hence, like the blocking mode RCD circuit is activated automatically; unlike blocking mode C_s is not fully charged such that R_{sm} acts as a virtual load for a capacitor that consumes electrical charge. In this case, during DC fault, AC current is not cut off, and the fault location is fed and limited through the RCD circuit; so, the current does not decay to zero, and consequently, the AC grid remains stable.

Since the proposed MMC topology includes both HB and TQB, let us assume n capacitors (C_s) are in series during the protection mode due to in fault path, two arms are in the fault current path. As it is illustrated in Fig. 8 the fault current flow through RCD circuit periodically, in doing so C_s is charged when S_x is off and it is discharged when S_x is on. The equivalent capacitance and resistance in each arm is calculated as below.

$$C_{seq} = 2C_s/n \quad (7)$$

$$R_{seq} = \frac{n}{2}R_s + R_{fault} + 2R_o \quad (8)$$

During the fault current limiting mode, the fault current charges C_{seq} and it is discharged by R_{SM} . The second-order equation of the RLC circuit during charging mode by applying KVL is as follows. These equations hold if $0 < \omega t < \pi$.

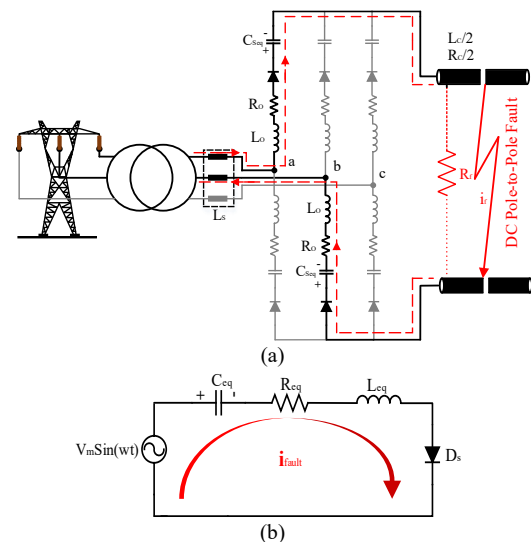
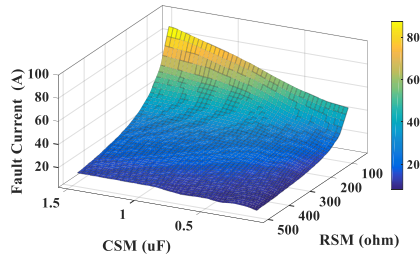


Fig. 6. The current path during the fault current blocking step, (a) Current path in three phases, and (b) equivalent circuit.

Fig. 7. Variation of I_{fault} by changing value of RCD parameter.

$$\frac{d^2 u_{cs}}{dt^2} + \frac{R_{eq}}{L_{eq}} \frac{du_{cs}}{dt} + \frac{1}{L_{eq} C_{eq}} u_{cs} = 0 \quad (9)$$

$$u_{cs} = K e^{s_1 t} - K e^{s_2 t} + \frac{K'}{\omega C_{eq}} \cos(\omega t + \beta) \quad (10)$$

$$i_f = K C_{eq} S_1 e^{s_1 t} - K C_{eq} S_2 e^{s_2 t} - K' \sin(\omega t + \beta) \quad (11)$$

Where I_f represents the fault current in the blocking mode, and R_{eq} is the equivalent of series resistance during a fault condition, L_{eq} is the equivalent inductance of the DC transmission cable and arm inductance, C_{eq} equivalent capacitance of RCD which is in series during the fault.

The first-order equation of the RCD circuit during discharging mode by applying KVL is as follows. (S_x is switched on).

$$u_{cs} = V_0 e^{-t/R_{eq}C} \quad (12)$$

$$i_f = \frac{V_0}{R} e^{-t/R_{eq}C} \quad (13)$$

$$V_0 = K e^{\frac{s_1 T_{SW}}{2}} - K e^{\frac{s_2 T_{SW}}{2}} + \frac{K'}{\omega C_{eq}} \cos\left(\frac{\omega T_{SW}}{2} + \beta\right) \quad (14)$$

$$R_{eq} = R_S + R_{SM} \quad (15)$$

Where I_f represents the fault current in the fault current limiting mode during discharging mode, in this stage capacitor is discharged through R_{SM} and R_S .

V. PROPOSED ENHANCED TQB-SM

A. Operation Principle

Another vital advantage of the proposed topology compared to other protective SMs topologies is the lower overall cost. Table I illustrates the TQB-SM overall cost increases only by 70 percent compared to HBSM, which is lower than other protective SMs topologies. This section's focus is on the enhanced TQB-SM overall cost reduction. Enhanced TQB-SM is illustrated in Fig. 9, including an additional current bidirectional IGBT switch and an RCT (Resistor, Capacitor, and Thyristor) circuit parallel with the output terminal of SM compared to those of the HB. This change reduces the voltage stress on S_x while blocking the fault current. The switch with a lower nominal voltage lies in the circuit, and the final price reduces significantly (cost of enhanced TQB-SM increases by only 40 percent compared to HBSM). Besides, by replacing the thyristor instead of the diode, it is possible to control S_x 's fault current independently by adjusting the firing angle. So, it adds more controllability to the circuit during the fault mode.

Like the TQB-SM under normal operation, S_x is always on, T_s is always off, and S_1 and S_2 act as complementary switches. Fig. 10 demonstrates different modes of enhanced TQB-SM; when S_x and T_s are respectively on and off, it works exactly like an HB. In a normal operation like TQB-SM, the power losses can be considered equal to the HBSM power losses [20].

As soon as a fault is detected, all switches of enhanced TQB-SM are blocked, T_s switched on, and the fault current starts charging C_s by passing through T_s , R_s , and R_{SM} . The fault current charges and R_{SM} discharges C_s during the fault and post-fault conditions, respectively. In one mode, the DC-link is isolated from the AC grid by fully charged capacitors, and no current is injected from the AC grid into the fault location. In the other mode, a proper selection of RCT parameters and thyristor firing angle control would limit the fault current such that the AC grid remains stable during the DC fault.

B. Fault Current Limiter Mode in enhanced TQB SM

As previously stated, to maintain the grid stability, it is necessary to avoid blocking the fault current. In such topology, to control the fault current, according to the capacitor's appropriate values and the resistance, the thyristor fire angle can be controlled. By controlling the firing angle, the capacitor's charge is controlled and prevents overcharging, and the limited current flows to the fault location. As soon as a DC fault is detected, all IGBTs will be switched off. At the same time, another control scheme is activated as illustrated in Fig. 11; the DC current traces an adjustable reference, as a desired limiting DC fault current, using the firing angle prepared by the controller. Fig. 12 illustrates the variation of firing angle and RCT capacitor value versus the fault current.

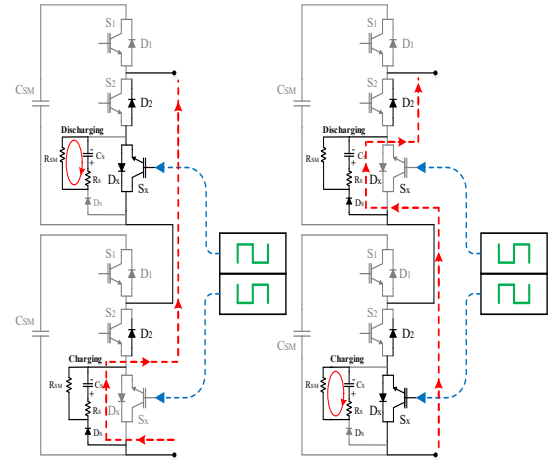


Fig. 8. Fault current path in FCL mode.

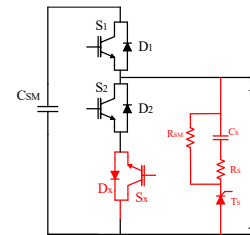


Fig. 9. Proposed enhanced TQB-SM for protecting against DC Fault.

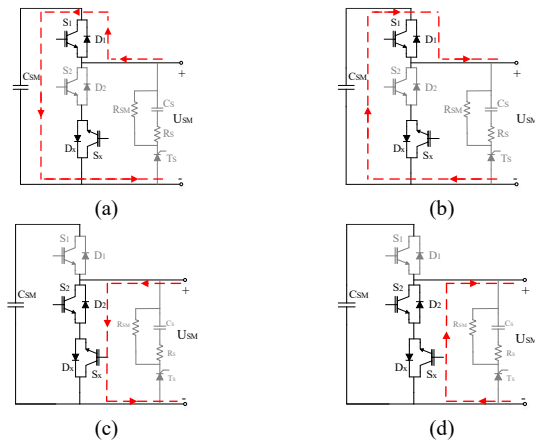


Fig. 10. Current direction of the enhanced TQB-SM during normal operation, (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

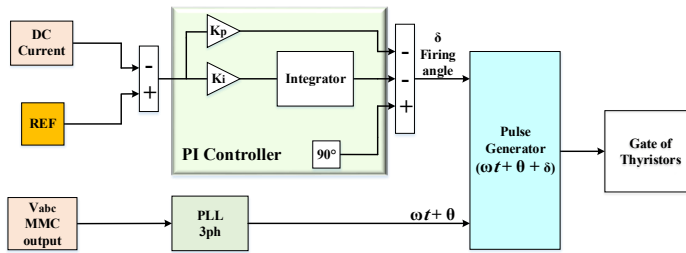


Fig. 11. Control strategy of thyristor in enhanced-TQB sub-module.

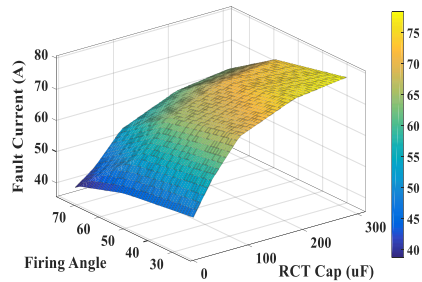


Fig. 12. Variation of I_{fault} versus changing the values of RCT parameter and the thyristor firing angle.

VI. SIMULATIONS

A full-scale simulation is performed in MATLAB/Simulink software to verify the proposed hybrid MMC's validity. The proposed hybrid MMC that is simulated in inverter mode has four sub-modules per arm, including two HBSMs and two TQB-SMs. Also, for the stability investigation of the AC grid during the fault condition, the rectifier station of HVDC is simulated and presented. In this model, the AC side of the rectifier station is connected to the AC grid fed by two turbine-generators that generate 900MVA, and a load that consumes 100MVA is connected in parallel. Also, the frequency of the grid is 60Hz (see Fig. 13). The HVDC system interconnects two AC grids with different frequencies. Considering Fig. 13, in this model it is assumed that the AC grid on the rectifier station is operating at 60 Hz, where the AC grid on the inverter station is operating at 50 Hz.

The fault detection technique is a crucial issue in fault management, and when it decays under 0.9 p.u., the fault is

detected, and the protection scheme is applied. In this regard, three scenarios are simulated. The proposed hybrid (TQB + HB) MMC is first simulated under the normal operating condition and connected to the AC grid in the inverter station. Next, the permanent pole-to-pole DC fault is applied to the proposed hybrid MMC, and a nonpermanent DC fault is applied to the HVDC system in this station. Finally, a pole-to-pole DC fault is applied to the rectifier station with TQB-SM and enhanced TQB-SM to investigate the AC grid's stability under DC fault conditions, and proposed topologies and results are compared in different modes.

A. Normal operation (Inverter Mode)

In this scenario, the proposed hybrid MMC (TQB + HB) is connected to a 6kV (50Hz) grid while the DC-link voltage is equal to 10kV. The active and reactive power produced by MMC equals 1MW and 0.5MVAR, respectively. Other parameters of the simulated system are shown in Table II.

As shown in Fig. 14 (a), the output three-phase voltage is nine levels created by each SM capacitors. Given MMC's amount of power into the AC grid, the modulation index is approximately 1. Hence, all voltage levels can be produced in the output waveform if the modulation index is reduced to less than 0.75. Since the power injected reduced power, the number of voltage levels is also reduced to seven. As can be seen in Fig. 14(b), the power losses of the HBSM and the TQB-SM are almost identical under normal operating conditions, which is one of the essential advantages of the proposed TQB-SM. The enhanced TQB-SM under normal operation has the same results as TQB-SM.

TABLE II

Simulation Parameters of Inverter Mode

Parameter	Value	Unit
L_o	1	mH
SM Capacitor	2	mF
DC Voltage	10	kV
Grid Voltage	6	kV
AC Frequency	50	Hz
Line Voltage Levels	9	-

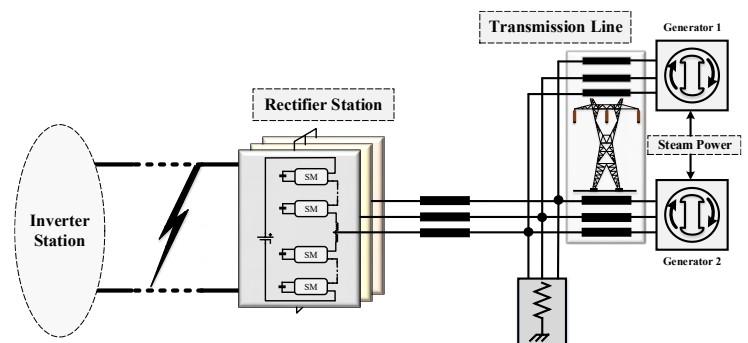


Fig. 13. Simulated rectifier station to investigate stability of AC grid during DC fault.

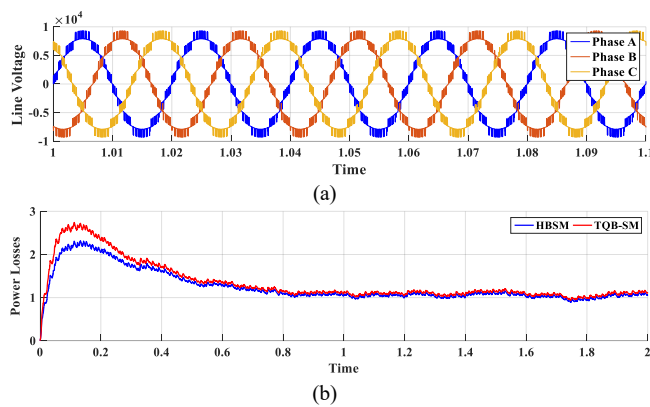


Fig. 14. Simulation results under normal operation, (a) line voltage, and (b) HBSM and TQB-SM power losses per one module.

B. Permanent DC Fault with DC Fault Current Blocking Capability (Inverter Mode)

In this scenario, the pole-to-pole DC fault occurs at 1s in (TQB+HB) hybrid topology. In this strategy, as soon as the fault occurs, to prevent SM capacitors from being short-circuited, all switches are blocked, such that the current passes through the diodes of RCD circuit and charge the C_s . By charging C_s , the AC feeding phenomenon is cut off.

Fig. 15(a) illustrates the DC-link current. MMC is under normal operation until 1s, and active power is delivered to the AC grid by this time; at this time, pole-to-pole DC fault occurs, and the central controller blocks all switches with the abovementioned fault detection. The only way to flow current is through the antiparallel diode and the RCD circuit. Hence, due to the current path, C_s is charged, and it blocks the current path. As expected, the proposed configuration is fault-tolerant, and the current is not injected into the fault location from the AC grid in this mode.

The SM capacitor voltages are illustrated in Fig. 15(b). By applying the protection scheme, these capacitors are isolated from the current path; thus, the voltages remain constant until the fault is cleared. Fig. 15(c) is illustrated C_s voltage before and during fault occurrence. As soon as a possible fault is detected, the current path flows through the RCD circuit; in this way capacitors are charged by fault current. Therefore, full charged capacitor lies in the fault current path. The results shown in this section are for 100uF C_s . Here, the effect of changing the value of the capacitor on the blocking current rate and the fault current peak is also examined. In Fig. 15(d), the waveforms of the C_s voltage rise are plotted for different values of this component. As can be seen, with increasing capacitance, the time constant of the capacitor's charge increases and blocking time of the fault current increases too. Therefore, it is proved that the C_s value needs to be much smaller than the SM capacitors (C_{SM}) to block fault current immediately at the inverter station. The fault current waveforms for different capacitance values are illustrated in Fig. 15(e). As shown above, in addition to increasing the capacitor's time constant, the current blocking process also increases sharply. As mentioned, by the increase of capacitance, in addition to the increase of the time constant of the charge of the capacitor, the

time of blocking current also increases dramatically.

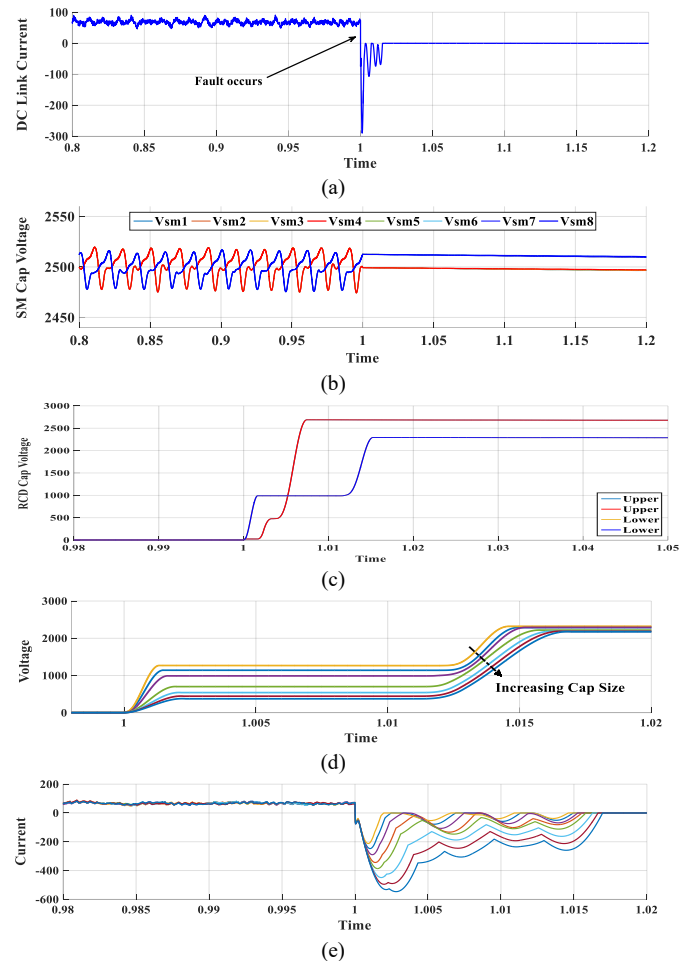


Fig. 15. Simulation results under permanent DC fault – Blocking mode, (a) DC current, (b) SM capacitor voltage, (c) RCD capacitor voltage, (d) capacitor voltage by changing the value of the RCD capacitor, and (e) fault current by changing the value of the RCD capacitor. (TQB + HB) hybrid topology.

C. DC Fault with Fault Current Limiter Capability (Inverter Station)

In this scenario, first, the pole-to-pole DC fault occurs in 0.7 Sec. and is cleared at 0.85 Sec. in (TQB+HB) hybrid topology. As Fig. 16 (a) illustrates, during the fault time, the AC current does not cut off. It flows through the RCD circuit continuously with the 2nd harmonic. C_s is not fully charged in this mode due to the switching mechanism proposed in section IV, and DC current is not cut off and limited. Fig. 16(b) shows the DC-link current before, during, and after the fault. As expected, as soon as the fault is detected RCD circuit limits the fault current, and consequently, the power grid remains stable during the fault. After the fault is cleared, the DC current slowly increases and lies in the previous point. The goal of this scheme is to keep the grid stable. As Fig. 16(c) illustrates, the three-phase grid voltages remain stable during and after the fault. As soon as the fault is cleared, the control system sends the PWM signals to follow the power reference. In this way, instantly, it decays to 2400V, and the voltage balancing algorithm keeps them in a

balanced mode. Fig. 16 (d) illustrates DC current both during normal operation and faulty condition with varying fault resistance. It can be seen that the DC fault current is increased when the fault location (resistor) gets closer to the MMC; however, the fault current limiting mode is activated in order to limit the fault current to a certain value.

Fig. 17 illustrates the variation of RCD voltage capacitor versus C_{sm} and R_{sm} values. By selecting these two parameters, the TQB-HB topology can be a current limiter during the fault condition. It can set up the value of current flows during the nonpermanent fault as well. In this paper also the enhanced TQB-SM is proposed. As mentioned in the previous section, this topology can be used to limit the DC fault current. Also, the thyristor firing angle is controlled instead of S_x . Therefore, this topology can act as TQB-SM by setting the firing angle to zero and switching S_x on/off. The proposed results show the fault current limiting by firing angle control. In this scenario, the pole-to-pole DC fault occurs in 0.6s in (enhanced TQB+HB) hybrid topology. As Fig. 18 (a) illustrates, the AC current does not cut off, and it flows through the RCT circuit such that the grid remains stable. Also, Fig. 18 (b) shows the AC grid voltage remains stable and does not decay to zero due to the DC fault. Fig. 18 (c) extends during fault condition to post-fault steady states, where the short-term (0.6 Sec. < t < 0.66 Sec.) low-magnitude (peak-to-peak smaller than 0.1 p.u.) distortions are vanished. Note that the power flow direction is reversed during the fault, i.e. from the AC grid to the HVDC-side. These short-term low-magnitude distortions are traded off for stable operation of AC power grid. Fig. 18 (d) shows the fault current variation versus firing angle. As shown by increasing the firing angle to 75 degrees, the fault current increases, and more active power is consumed. The DC-link nominal current is set to be 80A for this scenario, so the optimal value for the DC fault is 25 degrees such that the maximum current does not exceed 80 A.

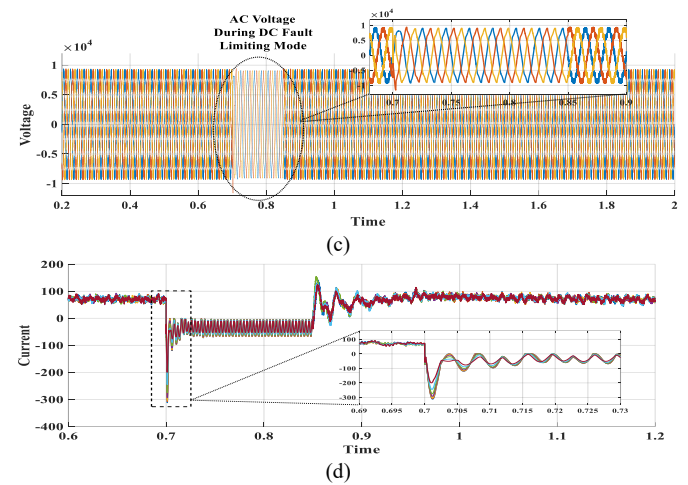
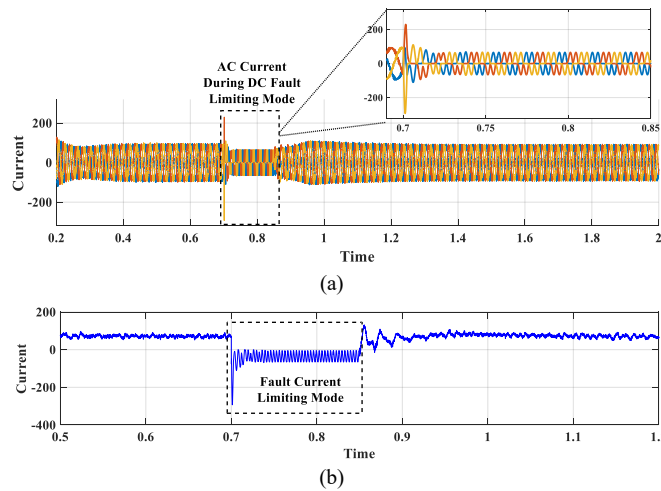


Fig. 16. Simulations under nonpermanent DC fault - Limiting mode, (a) grid current, (b) DC current, (c) line voltage, and (d) limited DC current by different fault resistances.

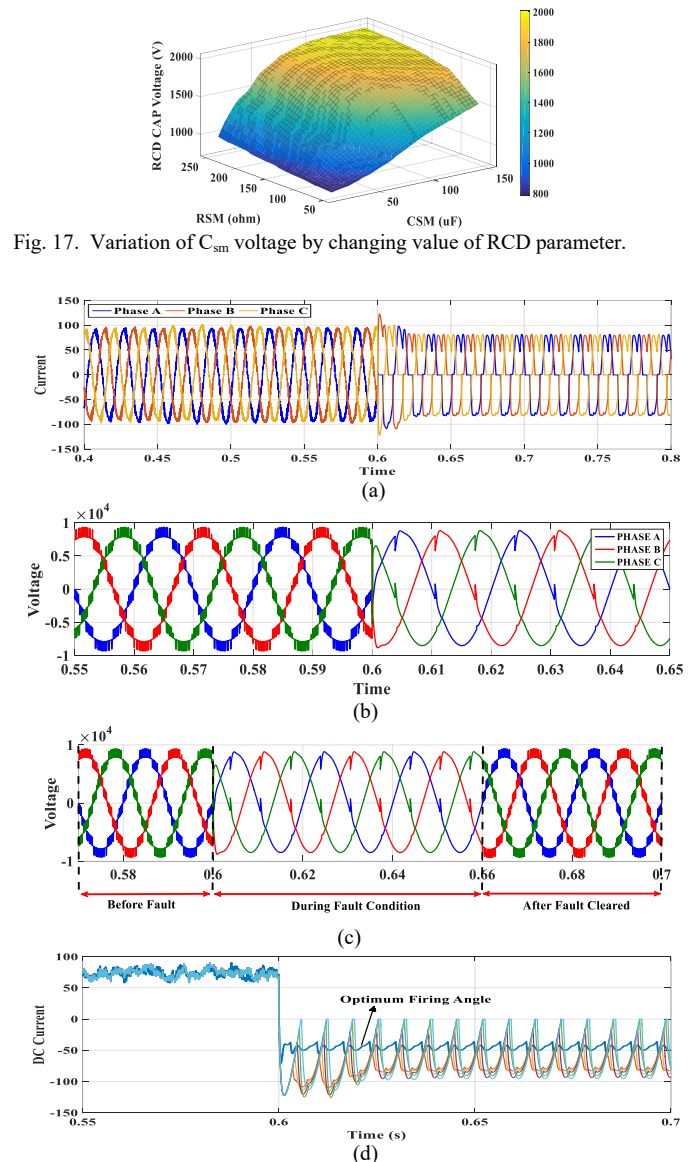


Fig. 18. Enhanced TQB + HB Simulation results under DC fault - Limiting mode, (a) AC current, (b) Line voltage, and (c) DC Link current by variation of firing angle.

D. Investigation of Grid Stability under DC fault by proposed topology (Rectifier Station)

In this scenario, as is illustrated in Fig. 13, the rectifier station's AC side is connected to the 60Hz AC grid fed by two turbine-generator that generate 900MVA respectively, and a load that consumes 100MVA is connected in parallel. In the HVDC system's rectifier station, blocking mode is undesirable in terms of frequency stability and may become unstable. So, this topology can act as a fault current limiter during the nonpermanent and permanent DC faults.

Fig. 19 shows the generators' angle variations of a 60Hz grid in three modes. As mentioned earlier, when TQB-SM blocks the fault current, the generators' angle variations parameter is increased, which means that the generators' angles relative to each other increase, which may cause network instability. However, as shown in Fig. 19, if the current fault limiting algorithm is applied, the generators' angle variations are reduced. This constant value is getting fixed in less than one second (converges to the constant value before the fault state); this means that the two generators are stable relative to each other, which ultimately causes the grid to remain stable. Also, as can be seen, the two topologies presented (TQB and Enhanced-TQB) operate in the stability region in this scenario. Fig. 20. shows the grid frequency changes for the three modes of blocking, fault current limiter, and Enhanced-TQB. As can be seen, the blocking mode's grid frequency increases by approximately 0.5Hz and remains constant; this amount of increase in the grid is not desirable. Therefore, by applying the current limiting algorithm and Enhanced-TQB, the network frequency changes are 0.1 and 0.15 Hz, respectively, which is desirable in terms of grid frequency stability. It should be noted that in the Enhanced-TQB mode, although the frequency changes are more significant than the TQB structure in the current-limiting mode, the result is very desirable due to the price reduction in the improved structure. Fig. 21. shows the DC current before and during fault occurrence. As can be seen, the fault current is limited to 80% and 50% for the TQB and Enhanced-TQB topologies, respectively, while it is zero for the TQB-Blocking topology. Fig. 22. represents the generators' load angles. After the DC fault, the second generator's load angle in the blocking mode increases and tends to a constant value. Although the generator has not entered into the unstable zone, the load angle increase is undesirable, and there is a possibility of instability. However, both generators' angles in this topology remain almost constant in current-limiting modes, and the grid maintains its previous state.

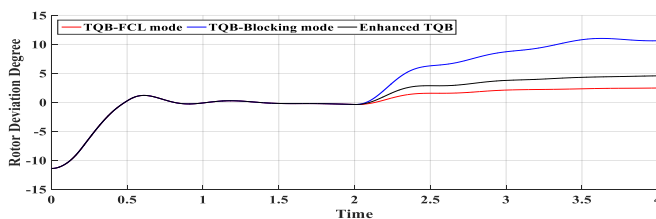


Fig. 19. Generators angle variations during fault condition for three modes.

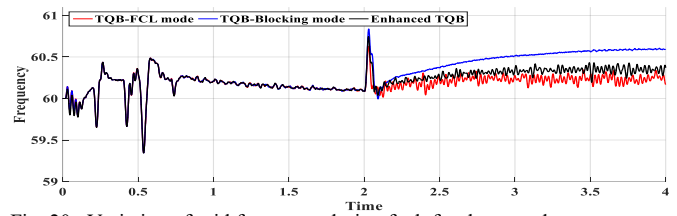


Fig. 20. Variation of grid frequency during fault for three modes.

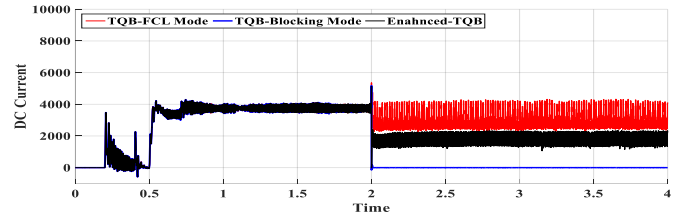


Fig. 21. DC current for three modes.

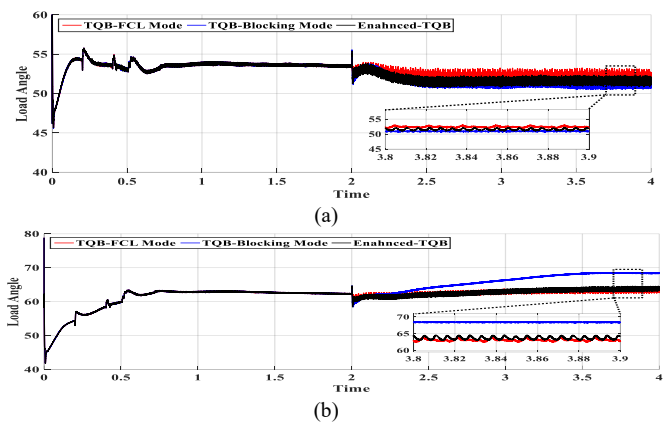


Fig. 22. Variation of load angle during fault for three modes, (a) Generator 1, and (b) Generator 2.

VII. TQB EXPERIMENTAL VALIDATION

Fig. 23(a) shows the built-in sample of the TQB module consists of several parts; the RCD circuit is close to the IGBTs, an isolated negative/positive voltage flyback converter drives IGBTs as well as monitoring circuits that balance the SM capacitor voltage and circulating current. In this prototype, two ARM-based STM32F407VGT6 microcontrollers have been used to generate the modulating pulses of the switches along with regulating SM capacitor voltages and circulating current of the MMC.

To validate the proposed protective scheme, a single phase hybrid MMC (TQB + HB) was implemented as shown in Fig. 23(b). The single phase converter includes two arms, each consists of two TQB and two HB sub-modules (totally four TQB and four HBs). The test setup specifications are listed in Table III. A single-phase AC source supplies the device, and the DC output is loaded with adjustable resistive elements.

Three different experiments were arranged in order to confirm the capability of the TQB both in full blocking and partial blocking of the DC current due to a Pole-to-pole DC fault with a small resistance (PDCFSR) (see Table III). First, the PDCFSR was applied to a fully HB-based MMC, the DC

current increased from 5A (pre-fault) to 22A (during the PDCFSR) in steady state as shown in Fig. 24 (a). Second, the fully blocking mode was tested, where four TQBs blocked the DC current during PDCFSR (see Fig. 24 (b)). In fact, the RCD capacitors of TQBs are fully charged, blocking the AC feeding phenomenon.

Third, the switch S_x of the TQBs are driven with a duty cycle of 50% to limit the fault current to a level that not harm the overall system. This limiting mode was experimented as demonstrated in Fig. 24 (c). In practice, the switching pulse width modulation of S_x avoid the RCD capacitors from full charging, providing the limited AC feeding phenomenon.

TABLE III
Experimental setup specification

Parameter	Value	Unit
L_o	1	mH
SM. Capacitor	2	mF
RCD Capacitor	400	uF
DC Voltage	100	V
AC Frequency	50	Hz

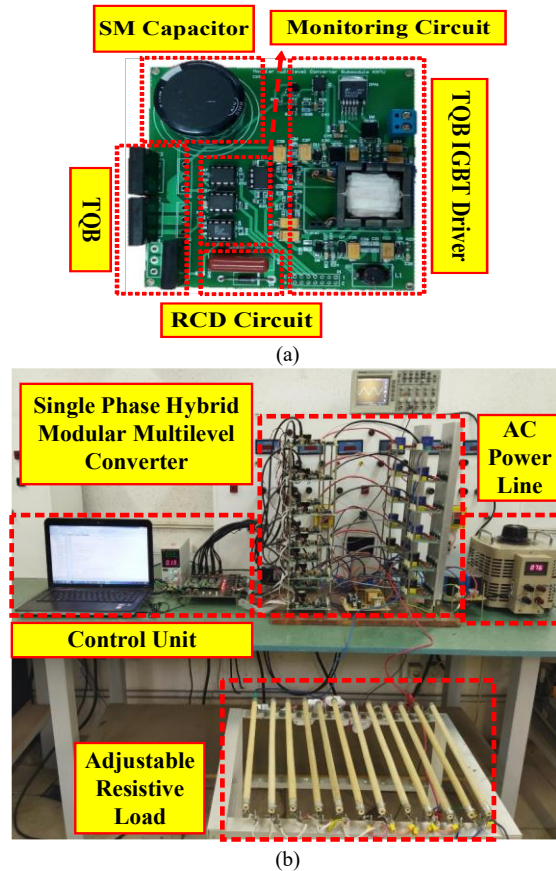


Fig. 23. DC current, (a) Experimental setup for single phase hybrid MMC, and (b) TQB Sub-Module prototype.

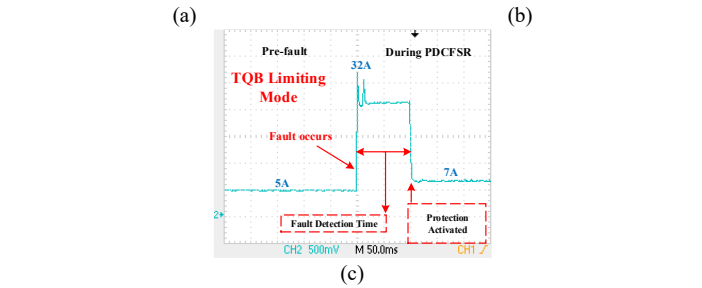
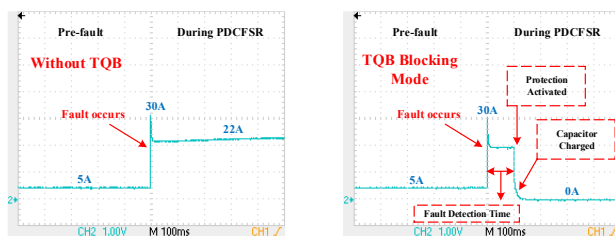


Fig. 24. DC current in fault condition, (a) HB-based MMC, (b) TQB blocking mode, and (c) TQB limiting mode.

VIII. CONCLUSION

This paper proposes a hybrid MMC topology by introducing the TQB modules alongside with conventional HB. Under normal operation, the TQB acts like the HB for the proposed hybrid MMC. While anti-parallel diodes of HB modules provide a path for the fault current during a pole-to-pole DC fault, the TQB modules could impede the fault current. Two protective modes are suggested for TQB modules; blocking and limiting modes. Each TQB module has an extra switch with a RCD circuit that contribute to performing the two mentioned modes. It can also act as a fault current limiter to improve the grid stability during a fault condition. Simulations shows the proposed hybrid MMC topology preserves advantages of conventional HB-based MMC such as low power losses. A basic experimental setup was arranged to demonstrate the protection capabilities of the hybrid MMC in comparison with the conventional HB-based MMC. Experiments show this structure impedes the fault current both in blocking and limiting modes during a pole-to-pole DC fault.

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