

A Fringe Field Shaping CMOS Capacitive Imaging Array

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Abstract—While classical electrochemical impedance spectroscopy (EIS) focuses on measurements from a single working electrode, dense active microelectrode arrays offer opportunities for new modes of sensing. Here we present experimental results with an integrated sensor array for electrochemical imaging. The system uses a 100×100 custom CMOS electrode array with $10 \mu\text{m} \times 10 \mu\text{m}$ pixels, which measures impedance at frequencies up to 100 MHz. The sensor chip is uniquely designed to take advantage of the electrostatic coupling between groups of nearby pixels to re-shape the local electric field. Multiple bias voltages and clock phases create new types of signal diversity that will enable enhanced sensing modes for computational imaging and impedance tomography.

Keywords— biosensor, capacitance, impedance, electrochemical, image sensor, CMOS, dielectric spectroscopy, array, computational image sensor

I. INTRODUCTION

Capacitive sensing and electrochemical impedance spectroscopy (EIS) serve a wide range of applications, from monitoring cell cultures [1]–[19] to measuring neuron connectivity and activity [20], [21], from industrial flow sensing [22]–[24] to landmine detection [25]. While many classical techniques measure the impedance at the surface of one working electrode at a time, more complex measurements take advantage of networks of multiple electrodes. Impedance tomography systems, for example, often interrogate pairs of elements within a small but strategically positioned electrode array [22]–[24], [26]–[29]. As larger and denser microelectrode arrays become available, more complex multi-electrode stimulation and measurement can enable new sensing modalities for impedance imaging with enhanced sensitivity and improved spatial resolution [30].

Here we propose a high-density CMOS microelectrode array, which can manipulate the fringe fields of the measured pixel by configuring the clock phases and bias voltages within a moving kernel of neighboring pixels. The circuit operates at radio frequency which extends the reach of the electric field [31] and creates opportunities to leverage complex micron-scale interactions between the electric fields of groups of nearby pixels [32]. This new design builds on our previous work [2] and it bears a relationship to both computational image sensors [33] and impedance tomography [34], [35]. The sensor can be configured to perform some *in situ* signal processing while also reshaping the local electric field to extract additional information about a sample.

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II. FRINGE FIELD SHAPING MODEL

A simplified model to analyze the fringe field shaping is shown in Fig. 1(a), where two pixels are capacitively coupled to a buffer solution. The bulk solution is biased with V_{REF} , but most of the electric fields occur within tens of microns of the sensor surface. There is significant coupling between adjacent pixels (C_M). The chip operates at MHz frequencies, where one can largely neglect Debye screening [36]. But at these frequencies, the fields are still pseudo-static and we exclude resistive elements for simplicity.

As shown in Fig. 1, during the input, both pixels connect to V_{BIAS} for one clock phase, and then to either V_{CM} or V_{STDBY} . The pixels are controlled by two pairs of non-overlapping switching clocks (Θ_1 and Θ_2) with a common frequency but independent phases. Only the charge transferred through Pixel #1 is integrated by the readout circuit. If the phases of the two pixels' clocks are the same and $V_{STDBY} = V_{CM}$, then Pixel #2 serves to shield C_M , which can have sensing benefits as previously demonstrated [7]. Under these conditions, the signal current is $I_{SENSE} = C_1(V_{BIAS} - V_{CM})f_{clk}$, where f_{clk} is the switching frequency. However, if there is a phase offset between neighboring pixels, more possibilities and complexities emerge. For example, Fig.1(b) illustrates a 90° offset between two pixels. In this scenario, the integrated current is a function of C_M ,

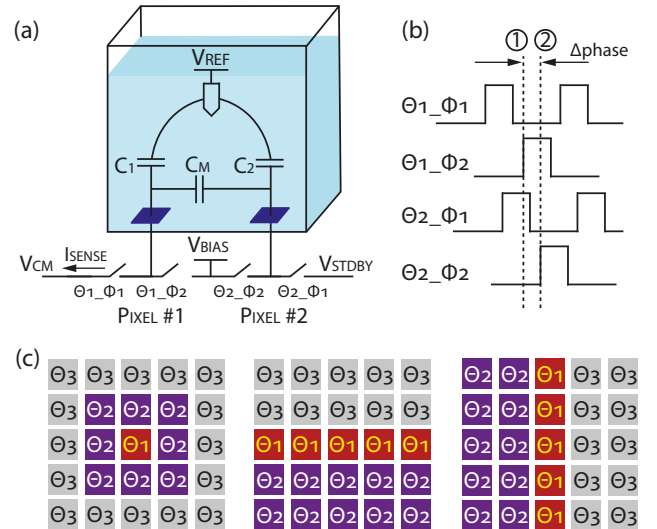


Fig. 1. (a) Two pixels with a simple capacitance model. (b) Illustration of two sets of non-overlapping clocks with 90° phase shift. (c) Neighboring 5×5 pixel blocks can be configured with three different clock phases as either radial, vertical, or horizontal shaping kernels.

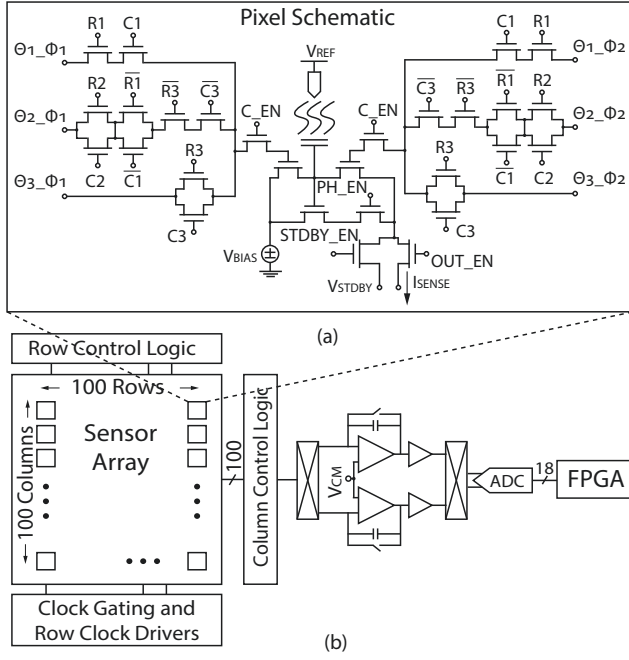


Fig. 2. (a) Pixel schematic, featuring logic to select multiple clock sources. (b) Overall architecture of the 100×100 pixel array. All of the columns are multiplexed into a common readout path.

expressed as $I_{SENSE} = [C_1(V_{BIAS} - V_{CM}) - C_M(V_{BIAS} - V_{STDBY})]f_{clk}$.

This two-pixel model can be generalized to a group of pixels driven by non-overlapping switching clocks with different phase offsets and biased by different output voltages. The prototype presented in this paper uses 5×5 pixel blocks to implement radial, vertical and horizontal kernels (Fig. 1(c)). The center pixel output is routed to the readout circuit and biased to V_{CM} , and the rest of the pixels are routed to V_{STDBY} . Physical models of these coupling capacitances will depend on the sensor parameters as well as the sample composition, and our goal is to use this complex parameter space to extract more information from spatially resolved EIS measurements.

III. CMOS SENSOR ARRAY DESIGN

The active sensing area has 10,000 pixels in a 100×100 grid (Fig. 2). Each pixel (Fig. 2(a)) can use one of three sets of non-overlapping input clocks ($\Theta_x - \Phi_1$ and $\Theta_x - \Phi_2$), which are synthesized externally. To achieve both efficient pixel area usage and flexible kernel configurations, we use a set of pre-decoded control signals to drive each row (R_x) and column (C_x), to dictate the clock selection in each pixel. All switches are NMOS pass-gates to save area. We also add a per-row clock gating for each set of switching clocks, and per-column (C_{EN}) control signals to disable pixels outside of the kernel. Bias voltages are supplied externally. Each pixel output can either be routed to the readout circuit or V_{STDBY} based on the two-dimensional row/column control. Each pixel contains an exposed electrode shared between the EIS measurement and a pH measurement with an ion-sensitive field effect transistor (ISFET). This paper focuses only on the EIS operation. To reduce 1/f noise,

(a) Radial Kernel	(b) Horizontal Kernel	(c) Vertical Kernel
$\Theta_1 \ \Theta_2 \ \Theta_3 \ R1 \ R2 \ R3$ Row 5: 0 0 0 0 0 1 Row 4: 0 0 0 0 1 0 Row 3: 0 0 0 1 1 0 Row 2: 0 0 1 0 1 0 Row 1: 0 0 0 0 1 0 $C1 \ C2 \ C3$ Col 5: 0 0 1 Col 4: 0 1 0 Col 3: 1 1 0 Col 2: 0 1 0 Col 1: 0 0 1	$\Theta_1 \ \Theta_2 \ \Theta_3 \ R1 \ R2 \ R3$ Row 5: 0 0 0 0 0 1 Row 4: 0 0 0 0 0 1 Row 3: 0 0 0 1 0 0 Row 2: 0 0 0 0 1 0 Row 1: 0 0 0 0 1 0 $C1 \ C2 \ C3$ Col 5: 1 0 0 Col 4: 1 0 0 Col 3: 1 0 0 Col 2: 1 0 0 Col 1: 1 0 0	$\Theta_1 \ \Theta_2 \ \Theta_3 \ R1 \ R2 \ R3$ Row 5: 0 0 0 0 0 1 Row 4: 0 0 0 1 0 0 Row 3: 0 0 0 1 0 0 Row 2: 0 0 0 1 0 0 Row 1: 0 0 0 1 0 0 $C1 \ C2 \ C3$ Col 5: 0 1 0 Col 4: 0 1 0 Col 3: 1 0 0 Col 2: 0 0 1 Col 1: 0 0 1

Fig. 3. Table of switching clocks and row/column controls to configure the 5×5 pixel block into radial, vertical and horizontal shaping kernels.

the output current is chopped between two integrators, and buffered for an external differential-input 500 kS/s 18-bit ADC (Fig. 2(b)).

While many different configurations are possible, here we demonstrate three 5×5 configurations implementing radial, horizontal and vertical kernels (Fig. 1(c)). The detailed control signals for each configuration are shown in Fig. 3. Often, we elect to route the center pixel to I_{SENSE} , while the surrounding pixels are routed to V_{STDBY} . On-chip logic shifts the 5×5 pattern through the 100×100 array to capture one frame, producing an image of 96×96 complete kernels.

IV. ELECTRIC FIELD SIMULATIONS

Fig. 4 presents finite element simulations (COMSOL, Burlington, MA) of the electric field for pseudo-static conditions similar to the available operating modes of the sensor. In the baseline setting (no shaping), neighboring pixels switch in phase to shield the parasitics of the measured center pixel [2]. When there is a change in the AC voltage amplitude or phase of pixels in the kernel, it affects the shape and depth of the three-dimensional sample volume over which the effective capacitance is measured.

V. MEASUREMENT RESULTS

The circuit is implemented in a 180 nm 1P6M CMOS process (Fig. 5), with an area of 2.24 mm² and power consumption of 24.5 mW while operating at 100 MHz. The chip is packaged with a simple fluidic cell, and the electrodes are post-processed to expose a titanium nitride layer using a

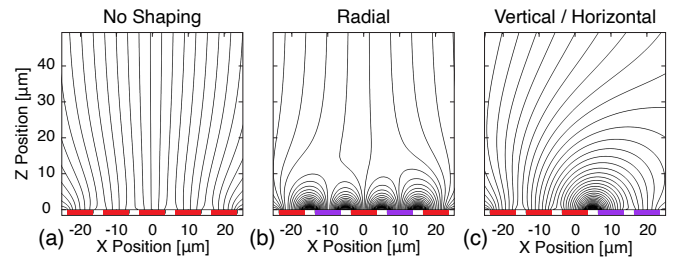


Fig. 4. Finite-element electric field simulations. (a) All 5 electrodes are biased at 100 mV. (b) Electrodes in the outer ring and center are biased at 100 mV and those in the inner ring at 0 V. (c) Left and center electrodes are biased at 100 mV and the right ones at 0 V. For all simulations, the medium is water ($\epsilon_r = 78$), $V_{REF} = 0$ V, and the reference electrode is placed 100 μ m above the sensor surface.

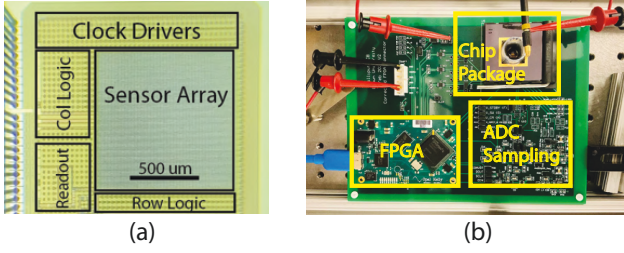


Fig. 5. (a) Micrograph of the 100×100 sensor array. (b) Photograph of the packaged chip and the data acquisition PCB.

previously described protocol [37] [38]. The integrated input-referred RMS noise for 1 kHz measurement bandwidth (1 ms/address) is 0.6 attofarads (rms))

Fig. 6 presents impedance measurements of $20 \mu\text{m}$ diameter polystyrene beads dispersed on the sensor, measured at 50 MHz in 1X PBS buffer. In Fig. 6(b), the bias voltages are equal, and the three clocks are in phase, which is comparable to a sensor without any fringe field shaping. In contrast, Fig. 6(c)(d)(e) show recordings of the same sample using three different local kernel patterns (radial, horizontal and vertical). In each measurement, only the charge from the center pixel is integrated, and the different apparent particle shapes are caused by the fringe capacitances coupling through the sample to neighboring pixels. The normalized 2D autocorrelation experimentally approximates the spatial impulse response and correlates to each programmed kernel.

In optical microscopy, spatial variance can be used as measure of image focus, and the mean-normalized variance (σ^2/μ) is a useful metric for autofocus systems [39]. While impedance imaging is based on entirely different physics, it seems reasonable to assume that images with higher pixel variance may contain more information. In Fig. 7(a), we use the normalized variance to rank the clarity of particle images across a sweep of 324 different radial field-shaping settings. During this parametric sweep, the phase of Θ_1 is fixed, and the phase offset between $\Theta_{2/3}$ and Θ_1 ranges

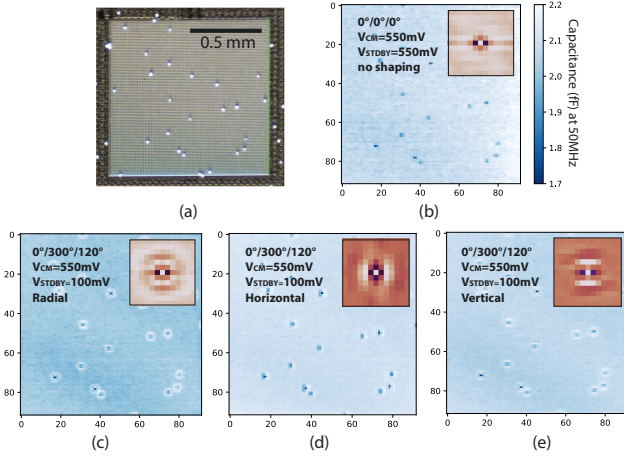


Fig. 6. (a) Microscope image of $d=20 \mu\text{m}$ polystyrene beads on the sensor. (b) Baseline measurement with all three switching clocks having the same phases and no fringe field shaping. (c) The same sample recorded with a radial field shaping kernel. (d) The image using a horizontal kernel. (e) The image using a vertical kernel. A magnified 2D spatial autocorrelation is included as an inset in each image.

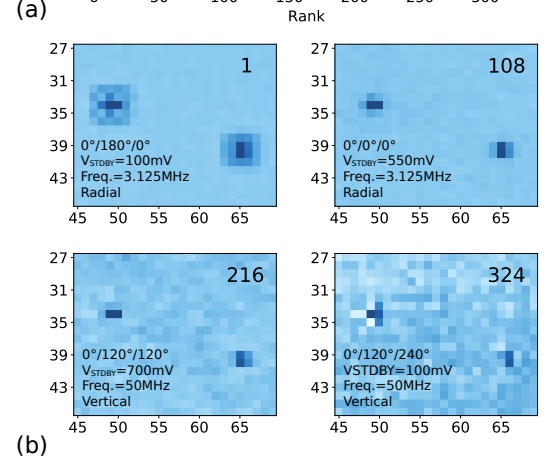
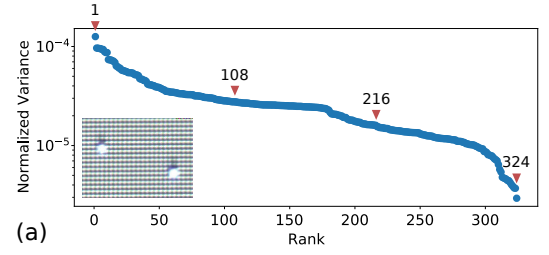


Fig. 7. (a) 324 field shaping settings (varying Φ_2 , Φ_3 , V_{STDBY} , f_{sw} , and kernel type), ranked by normalized variance (σ^2/μ). (b) Magnified portions of four images from the sweep.

from 0° to 330° with a step of 30° . V_{CM} is set to 600 mV, and V_{STDBY} ranges from 100 mV to 950 mV. Radial, horizontal and vertical kernels are used, and five switching frequencies are selected between 781.25 kHz and 50 MHz. In addition to simply detecting the beads, some settings produce qualitatively different images (Fig. 7(b)) which may correspond to sub-pixel bead locations or subtle variation between the size or shape of different beads.

Table I. Comparison with State-of-the-Art

	This work	[1]	[9]	[5]	[2]
Array Size	10,000	21,952	65,536	59,760	131,072
Pixel Size	$10 \times 10 \mu\text{m}^2$	$16 \times 16 \mu\text{m}^2$	$0.6 \times 0.89 \mu\text{m}^2$	$13.5 \times 13.5 \mu\text{m}^2$	$9.5 \times 11.5 \mu\text{m}^2$
Impedance Resolution	0.6 aF	—	0.5 – 1 aF	—	0.7 aF
Max Impedance Frequency	100 MHz	500 kHz	70 MHz	1 MHz	100 MHz
Technology	180 nm	130 nm	90 nm	180 nm	180 nm
With Fringe Field Shaping	Yes	No	No	No	No

VI. CONCLUSION

We have presented a CMOS capacitive imaging array with unique fringe field shaping capabilities to diversify pixel-scale features and improve sensing performance within spatially-resolved electrochemical impedance data. A comparison with other state-of-the-art integrated EIS arrays is shown in Table 1. Future work will include explorations of computational methods that use the signal diversity from a collection of fringe field patterns for microscale object classification and 3D shape reconstruction.

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