# Impact of Multilevel Retention Characteristics on RRAM based DNN Inference Engine

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***Abstract*—In this work, the retention characteristics of multilevel $HfO_2$ resistive random access memory (RRAM) based synaptic array was statistically measured from a 90 nm test chip and modeled at different temperatures. We found that not only the average conductance (especially at the intermediate states) drifts but also the variance of conductance exacerbates at elevated temperatures. To investigate the impact of the synaptic weight drift on deep neural network, the experimental data are modeled into the ResNet-18 simulation with 1-4 weight bit precisions. The result shows that the inference accuracy drops significantly at 55ºC or above, which implies further engineering on RRAM retention or circuit/algorithmic techniques are yet to be applied.**

***Index Terms*--multilevel RRAM, neural network, data retention.**

## I. Introduction

Deep neural networks (DNNs) have achieved significant success to various tasks such as image classification, speech recognition, and object detection. State-of-the-art deep learning algorithms are aggressively increasing the depth and size of the network to achieve the accuracy enhancement, which demands tremendous amount of computation. Consequently, the data movement between the microprocessor and off-chip memory suffers from excessive power consumption and memory bandwidth limitation in conventional von-Neumann computing architecture such as CPU and GPU. Several CMOS-based application specific integrated circuits (ASIC) accelerators such as Google TPU [1] are proposed as an alternative. However, the memory wall still becomes the bottleneck, where the weight parameters are stored in global buffer and computation is performed in separate digital multiply-and-accumulate (MAC) arrays. Frequent DRAM access is still required because of the limited global buffer capacity.

To overcome these challenges, compute-in-memory (CIM) is proposed as a promising paradigm where the weights are stored in the memory cells and the MAC operation is embedded in memory itself by the weighted sum of analog current along the columns.

Various type of NVMs have been investigated as the synaptic device for CIM application, such as resistive random access memory (RRAM) [2-3], phase change memory (PCM) [4-5], Flash memory [6-7] and ferroelectric field effect transistor (FeFET) [8]. RRAM has attracted great interest to represent the multilevel synaptic weights for accelerating DNNs [9]. Furthermore, multilevel RRAM enables larger MAC throughput with higher memory density [10]. However, multilevel RRAM based CIM for inference applications suffer from the non-ideal characteristics such as read disturb [11]. It should be noted that the requirement on the retention of synaptic weight memory for CIM is more stringent than the conventional multilevel cell (MLC) storage, because any conductance drift of the devices is summed up along the column so that the error bits can be induced at the analog-to-digital converter (ADC) quantized result, as shown in Fig. 1.

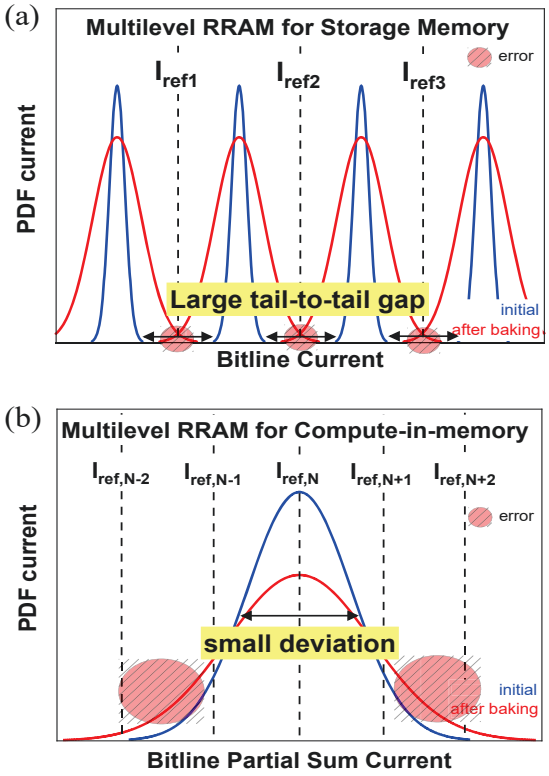


Figure 1. The requirement for multilevel RRAM cells for (a) storage memory and (b) compute-in-memory applications.

In this work, we tested the $HfO_2$ based 1T1R 64kb array fabricated at 90 nm process [12]. The retention characteristics of 2-bit RRAM cells are statistically measured and modeled.

W. Shim and J. Meng contributed equally to this work. This work is supported by ASCENT and C-BRIC, two of the SRC/DARPA JUMP Centers and NSF/SRC E2CDA program.

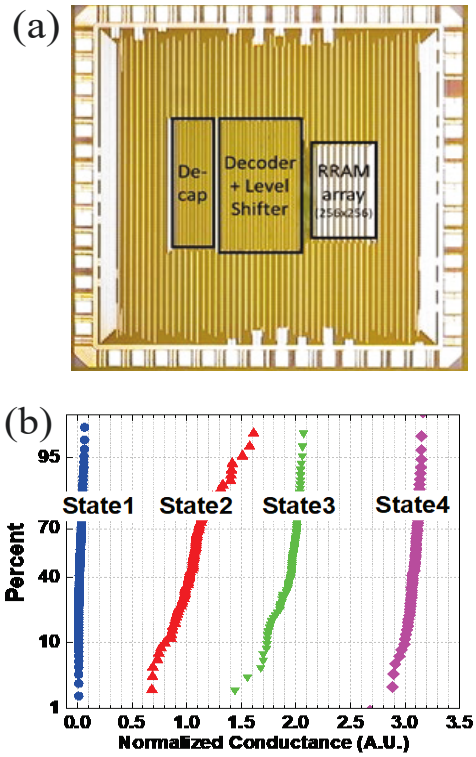


Figure 2. (a) Die photo of the measured 64kb HfO2 based 1T1R RRAM chip. (b) Initial multilevel cell conductance distribution after write verify.

The retention model is incorporated into the inference accuracy simulation of ResNet-18 model [13] on CIFAR-10 dataset.

## II. Retention Measurement and Modeling

Fig. 2(a) shows the die photo of the 256×256 1T1R $HfO_2$ based RRAM test chip with peripheral circuits. We realized the 2-bit per cell distribution with the RRAM test chip measurements. For inference operation, the weight is proportional to the conductance, thus we designed four states as follows. Fig. 2(b) shows the cumulative probability distribution of the initial conductance of multilevel states measured at room temperature (25ºC). The resistances of the State 1 cells are in high resistance state (HRS), while the resistances of the State 2/3/4 cells are in low resistance state (LRS) where each of the states' conductances are linearly spaced to represent the 2-bit weight. The initial conductance distributions were tightened with the two-step write-verify scheme [14]. The conductance of each state was controlled by SET and RESET current during the iterative SET and RESET loops. The bias conditions ($V_G$ and $V_D$) are optimized respectively for each state.

As shown in Fig. 3, the conductance drift of the RRAM cells in the test chip are measured up to 80,000 seconds at the temperature from 25ºC to 120ºC. The average conductance values are displayed for every state. The average conductance of the cells decreases over the baking time where the conductance drift rate is significant in State 2 and State 3. The State 2 and State 3 cells are the intermediate states which have relatively low stability in the viewpoint of weak filament.

The conductance not only drifts but also fluctuates over time. The ratio of standard deviation (σ) over the average conductance (μ) of the State 2 cells also increases significantly

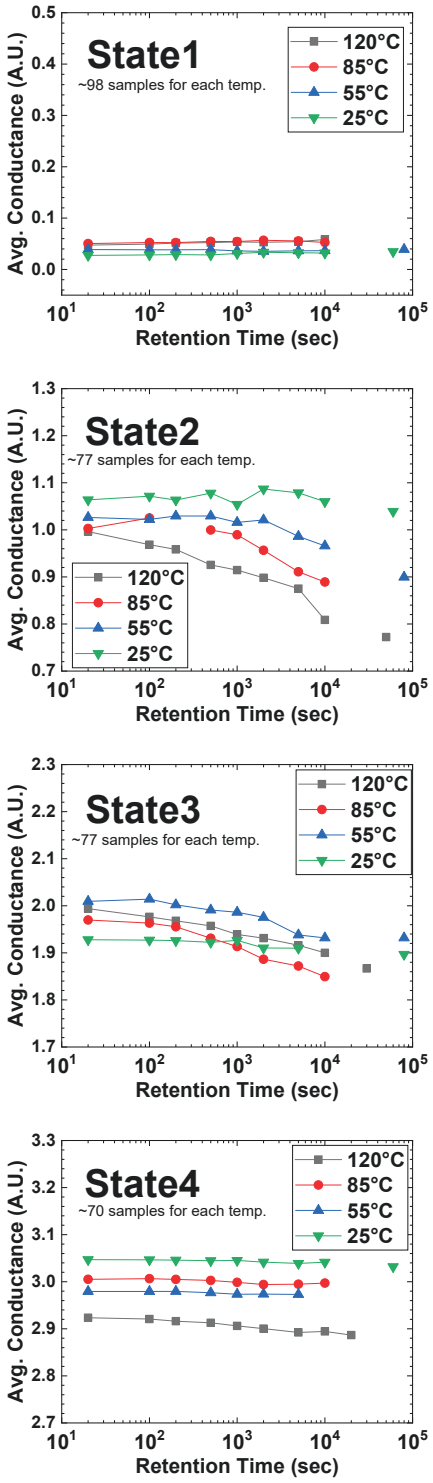


Figure 3. Measured average of conductance over time for each state at different temperatures.

over time and is accelerated by high temperature as shown in Fig. 4. Although σ/μ of the State 1 cells are very high and fluctuate over time, the conductance of the State 1 cells is several tens of times lower than that of the cells of other states.

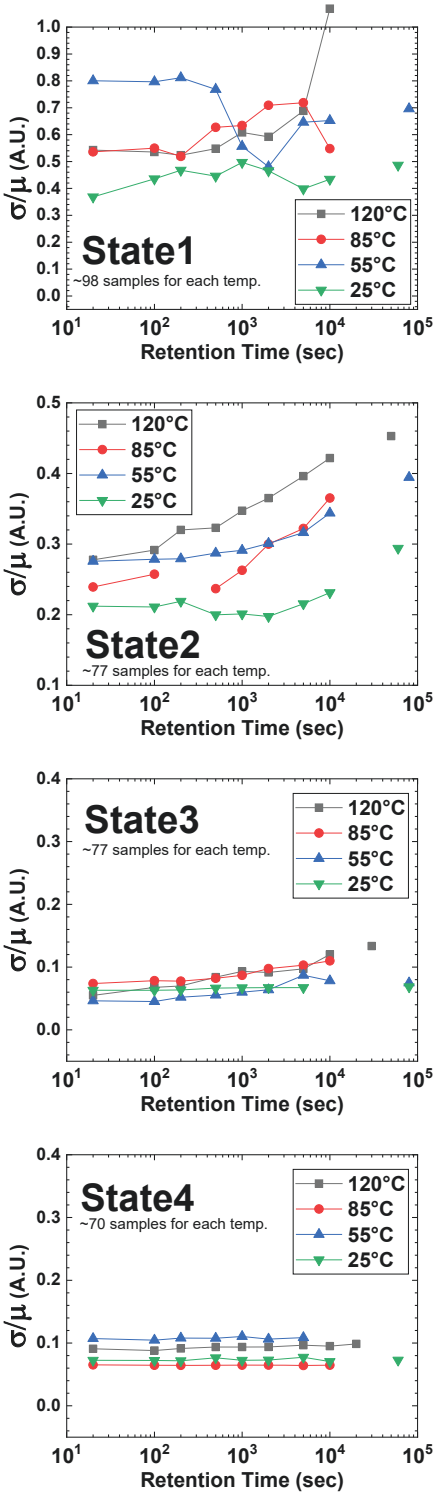


Figure 4. Measured sigma (σ) over average (μ) of conduction over time for each state at different temperatures.

Therefore, the high σ/μ ratio of State 1 cells does not significantly affect the total weighted sum current.

We modeled the measured retention characteristics in the following equations. The Δμ is fitted linearly to the logarithmic time as (1), where $A_{avg}$ is the average conductance drift rate that

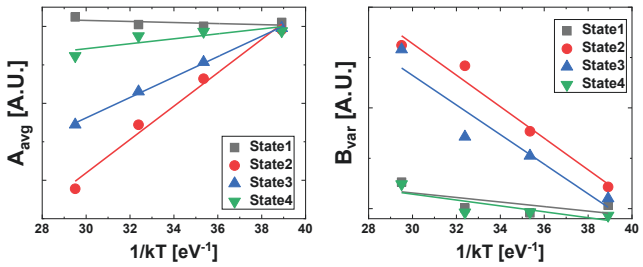


Figure 5. Temperature dependency of the conductance drift rate and fitting result on 1/kT plot for each state.

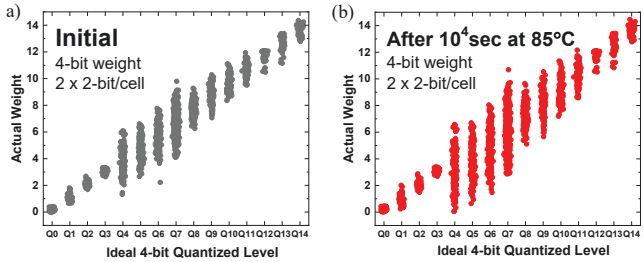


Figure 6. Weight distribution dispersion with retention model at (a) initial condition and (b) after $10^4$ sec at 85ºC for 4-bit weight precision.

depends on states and temperatures. The Δσ is also fitted as (2) with sigma conductance drift rate ($B_{var}$).

$$\Delta\mu = \mu(t) - \mu_{init} = A_{avg} \times log\, t \quad (1)$$

$$\Delta\sigma = \sigma(t) - \sigma_{init} = B_{var} \times log\, t \quad (2)$$

Fig. 5 shows the temperature dependency of the average and sigma of conductance drift rate ($A_{avg}$ and $B_{var}$). Because the cells of State 2 and State 3 are the intermediate states which have relatively low stability in the viewpoint of a weak filament, the activation energy on filament deformation is low.

## III. Inference Accuracy Simulation

We incorporated such 2-bit RRAM retention model into the ResNet-18 network to simulate the DNN inference accuracy on CIFAR-10 dataset. We adopted the PACT quantizer [15] for 2-bit/4-bit training and the BNN training [16] method to generate the pre-trained models in this work.

To implement the 4-bit weight into the RRAM array, we mapped two 2-bit per cell RRAM cells to one weight. The actual 4-bit weight has non-ideally quantized distribution as shown in Fig. 6, where the retention baking especially degrades the distribution of the quantized levels mapped with State 2 and 3. Fig. 7(a) implies that the inference accuracy drops significantly even when only the average drift model is considered. Considering the degradation of variation aggravates the accuracy further as shown in Fig.7(b).

We also simulated ResNet-18 network with 2-bit/1-bit weights as shown in Fig. 8. DNNs with lower weight precision show higher robustness and alleviate the accuracy loss, while trading off lower initial accuracy. It should be noted that the inference accuracy simulation results heavily depend on the training algorithm techniques including the neural network

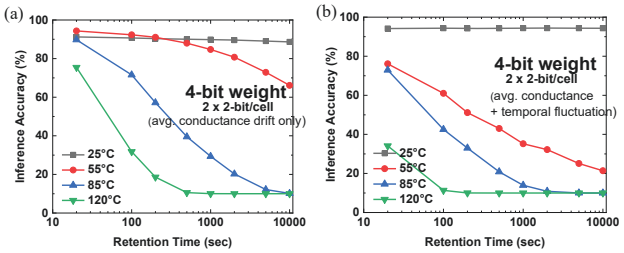


Figure 7. Simulated inference accuracy of ResNet-18 with (a) average conductance drift model only and (b) after adding temporal fluctuation model incorporated for 4-bit weight (two 2-bit per RRAM cells).

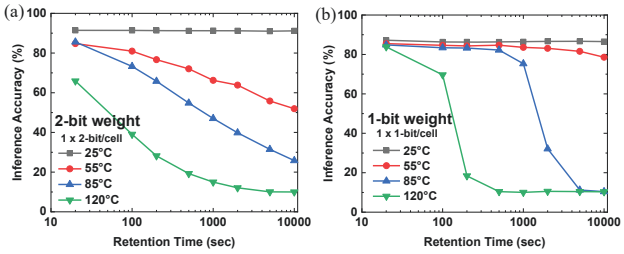


Figure 8. Simulated inference accuracy on ResNet-18 with (a) 2-bit weight (one 2-bit per cell) and (b) binary weight (one 1-bit per cell using only State 1 and 4).

topology. Different quantization schemes will also impact the distributions of the conductance states.

## IV. Conclusions

The retention characteristics of multilevel resistive random access memory (RRAM) are measured and modeled, then the effects on inference accuracy degradation are investigated. Different from the conventional MLC storage, multi-bit RRAM based inference engine requires more stringent retention characteristics to maintain the inference accuracy. While we assumed the reference voltage of ADCs are fixed in this work, reference voltage generation using dummy columns with additional RRAM cells may compensate the retention induced conductance drift (but cannot fully compensate the temporal fluctuation). Further algorithmic techniques or refresh schemes at circuit-level are also required to mitigate the accuracy drop of the CIM DNN accelerators.

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