



# Evidence for a monolayer excitonic insulator

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**The interplay between topology and correlations can generate a variety of quantum phases, many of which remain to be explored. Recent advances have identified monolayer WTe<sub>2</sub> as a promising material for doing so in a highly tunable fashion. The ground state of this two-dimensional crystal can be electrostatically tuned from a quantum spin Hall insulator to a superconductor. However, much remains unknown about the gap-opening mechanism of the insulating state. Here we report evidence that the quantum spin Hall insulator is also an excitonic insulator, arising from the spontaneous formation of electron-hole bound states, namely excitons. We reveal the presence of an intrinsic insulating state at the charge neutrality point in clean samples and confirm the correlated nature of this charge-neutral insulator by tunnelling spectroscopy. We provide evidence against alternative scenarios of a band insulator or a localized insulator and support the existence of an excitonic insulator phase in the clean limit. These observations lay the foundation for understanding a new class of correlated insulators with non-trivial topology and identify monolayer WTe<sub>2</sub> as a promising candidate for exploring quantum phases of ground-state excitons.**

Different classes of quantum phases, including Chern insulators and quantum spin Hall insulators, can be generated by various mass acquisition mechanisms of two-dimensional (2D) gapless Dirac fermions<sup>1</sup>. One such mass generation channel in a 2D Dirac semimetal, such as graphene, is the spontaneous exciton formation at charge neutrality<sup>2–5</sup>, which in principle can drive a semimetal–insulator phase transition at low temperatures. Although the observation of this excitonic gap in graphene has been long sought-after<sup>5</sup>, the real Coulomb interaction is so weak that it can only perturbatively reshape the Dirac cones rather than produce an insulating gap<sup>6</sup>. Despite continued theoretical interests<sup>7–11</sup> and despite having potential in engineering exotic states harnessing topology and fractionalization<sup>9,12,13</sup>, the experimental observation of a correlated excitonic insulator<sup>14–21</sup> has not moved beyond engineering quantum Hall bilayers<sup>22–24</sup>.

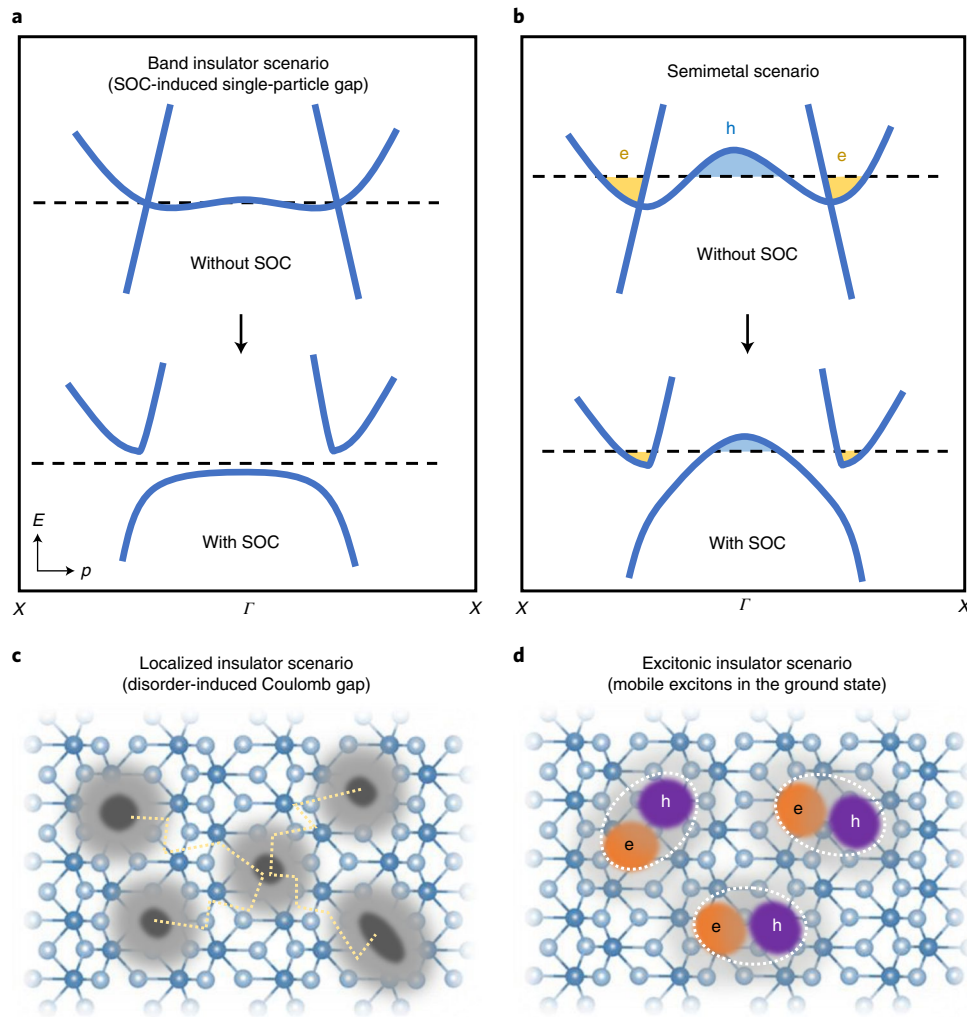
Monolayer WTe<sub>2</sub> is a highly unusual 2D crystal, where topology, correlations and spin–orbit coupling (SOC) are all simultaneously important<sup>25–30</sup>. Without SOC and interactions, a pair of tilted gapless Dirac points develop at the two sides of the  $\Gamma$  point along the  $\Gamma$ – $X$  direction in the monolayer's Brillouin zone (Supplementary Section 1), accompanied by a band inversion<sup>25,31</sup>. At low temperatures, the monolayer undergoes a semimetal–insulator transition, entering the quantum spin Hall insulator state<sup>25–28</sup>. Fundamental aspects remain unknown, including the gap-opening mechanism. Various possibilities have been suggested. Existing band structure calculations in the literature produce inconsistent results, predicting either a band insulator phase<sup>27,32,33</sup> (Fig. 1a) or a semimetal phase<sup>25</sup> (Fig. 1b). In the band insulator scenario, a single particle gap is opened via SOC<sup>25–27,32</sup>. A recent scanning tunnelling microscope (STM) experiment contradicted this picture and proposed that the

insulating state may arise due to a disorder-induced Coulomb gap<sup>34</sup> that diminishes the density of state at the Fermi surface. This is an extrinsic mechanism due to electron localization (Fig. 1c). Another possibility is the spontaneous formation of mobile excitons, resulting in an excitonic insulator phase (Fig. 1d; see Supplementary Section 1 for our theoretical modelling of this phase and also a recent proposal for relevant compounds<sup>7</sup>). Experimental evidence to uncover the true nature of the charge-neutral ground state in the clean limit of the pristine monolayer is lacking so far. In this work, by combining transport and tunnelling measurements, we uncover evidence that the WTe<sub>2</sub> monolayer supports an excitonic insulator phase in clean samples.

To reveal transport properties of the bulk of monolayer WTe<sub>2</sub>, we carefully design our devices so as to avoid transport along the conducting edge channels<sup>26,28</sup> (Fig. 2a,b). A hexagonal boron nitride (hBN) layer with patterned holes is used to cover the metal electrodes except their very ends, which are exposed to WTe<sub>2</sub>. The electrical contact to the monolayer bulk is then achieved without touching the edges. Top and bottom gates with hBN dielectric are used to tune both the carrier densities and the electric displacement field. Device details and the fabrication procedures are described in Supplementary Section 2. Figure 2c plots the measured four-probe resistance  $R_{xx}$  as a function of the top-gate voltage ( $V_{tg}$ ) and bottom-gate voltage ( $V_{bg}$ ), taken from device D1 at 70 K. The resistance exhibits a sharp peak at the charge neutrality line in the map, where the densities of electrons and holes are equal (see Supplementary Sections 3 and 4 for gate-dependent densities). Below 70 K, the peak resistance in the device is too large to be reliably measured. In Fig. 2d,  $R_{xx}$  is plotted as a function of gate-induced carrier density,  $n_g \equiv \epsilon_r \epsilon_0 (V_{tg}/d_{tg} + V_{bg}/d_{bg})/e$ , where  $e$  is

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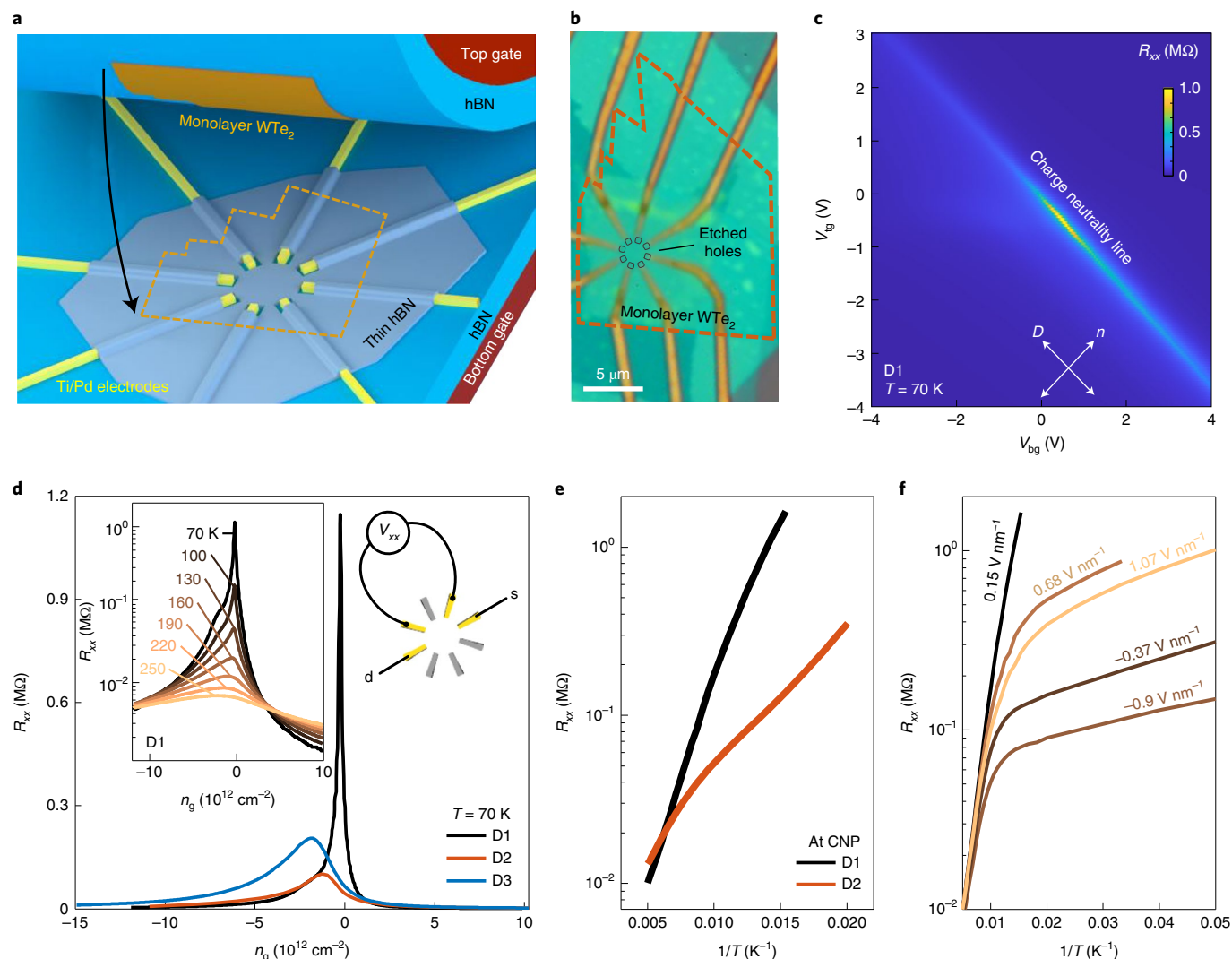
**Fig. 1 | Possible scenarios of the ground states at the charge neutrality point in monolayer  $\text{WTe}_2$ .** **a**, SOC-induced band insulator. The sketch depicts the low-energy bands with and without SOC. The axes are the momentum  $p$  and energy  $E$ . The dashed black line indicates the Fermi level. **b**, A semimetal phase is formed if the SOC cannot gap out the entire Fermi surface, resulting in one hole pocket (h) and two electron pockets (e) in the system. **c**, Electron localization can produce an insulating phase from a 2D semimetal via a disorder-induced Coulomb gap. **d**, An intrinsic excitonic insulator phase that hosts mobile excitons in the ground state.

the elementary charge,  $\epsilon_0$  is the vacuum permittivity,  $\epsilon_r$  is the relative dielectric constant of hBN and  $d_{\text{bg}}$  ( $d_{\text{tg}}$ ) is the thickness of the hBN layer associated with the top (bottom) gate. When the monolayer is doped with either electrons or holes,  $R_{xx}$  drops quickly from its maximum value (greater than  $1 \text{ M}\Omega$  at 70 K) at the charge neutrality point (CNP), before a metal–insulator transition occurs (Fig. 2d, inset). These observations are consistent with those of existing reports<sup>26,28–30</sup> on the monolayer, except that the edge state contributions are eliminated and the device quality is substantially improved here, as evidenced by the sharp CNP peak.

The exceptionally high quality of device D1 is achieved because we used a double graphite gate geometry<sup>35</sup>, a flux-grown  $\text{WTe}_2$  bulk crystal with a large residual-resistance ratio ( $\text{RRR} \approx 2,500$ ; see Supplementary section 5) and a fabrication procedure that minimizes disorder. To investigate the effect of disorder on the insulating state, we fabricated additional devices with controlled quality by altering these conditions, for example, by using a vapour-grown  $\text{WTe}_2$  bulk<sup>36</sup> with a typical  $\text{RRR} < 400$  (D2) or an air-sensitive metal  $\text{ZrTe}_2$  as the top gate (D3). The size and contact geometries of the three devices are similar. Gate-tuned resistance maps of D2 and D3

are plotted in Supplementary Section 6. A direct comparison of the three devices is shown in Fig. 2d, where  $R_{xx}(n_g)$  curves at 70 K are plotted together. Compared to that of D1, the peak of D2 or D3 is much broader and displays a notable offset from zero  $n_g$ , signifying the effect of disorder and inhomogeneity. One may treat the narrowness of the peak as an indicator of the sample cleanness; this quantity is improved by an order of magnitude in D1. In Supplementary Section 7, we plot the same data in terms of conductivity, which reveals that higher mobility is achieved for both electrons and holes in D1. All these observations confirm that D1 is much cleaner than D2 and D3, yet the resistivity of D1 at the CNP is much higher (Fig. 2d). The contrast experiments hence imply that the insulating state at the CNP is an intrinsic property of the monolayer in the clean limit. The disorder-induced Coulomb gap, as discussed previously<sup>34</sup>, is thus unsatisfactory to explain our observations.

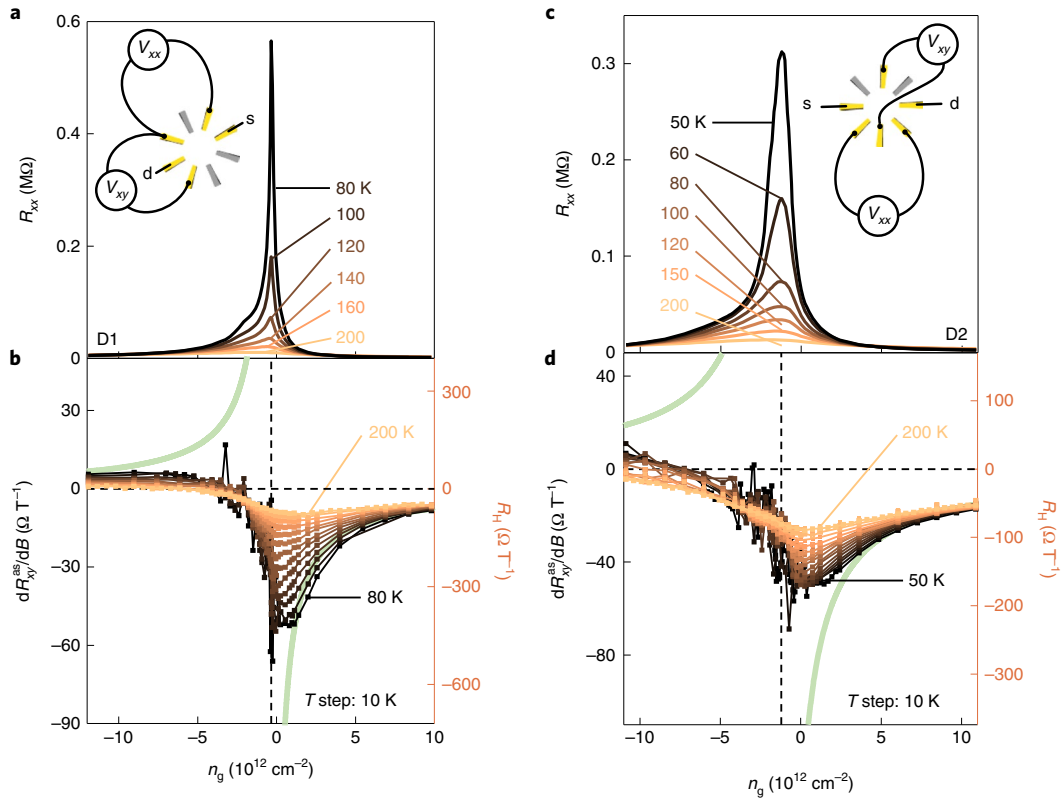
This intrinsic charge neutral insulator exhibits a strong dependence on the electric displacement field, defined as  $D = (V_{\text{bg}}/d_{\text{bg}} - V_{\text{tg}}/d_{\text{tg}})\epsilon_r/2$ . The temperature-dependent  $R_{xx}$  typically yields two regimes, separated by a temperature ( $T$ ) of nearly 100 K, as seen in the Arrhenius plot (Fig. 2e). Figure 2f plots the



**Fig. 2 | The insulating state at charge neutrality in monolayer WTe<sub>2</sub>.** **a**, Cartoon illustration of the transport device, where the electrodes contact the WTe<sub>2</sub> monolayer bulk without touching its edges. **b**, An optical image of a typical device (D1). **c**, Four-probe resistance mapped under varying top-gate voltage ( $V_{tg}$ ) and bottom-gate voltage ( $V_{bg}$ ), taken from D1 at 70 K. The measurement configuration is shown in **d**. **d**,  $R_{xx}$  as a function of gate-induced density  $n_g$  (defined in the main text) taken from three devices (D1–D3) under the same measurement configuration (right inset, s: source; d: drain). The  $n_g$  traces are selected to cross the most insulating regime in their respective dual-gate resistance maps. The displacement field is fixed for the D1 and D3 curves, whereas  $V_{bg}$  is set at 0 V for the D2 curve. The choice was made to maximize the scan range of  $n_g$  for each device. A qualitatively similar curve for D2 is obtained if the displacement field is fixed instead. Left inset: temperature effect on the  $R_{xx}$  curves of D1. **e**,  $R_{xx}$  as a function of  $T$  taken from D1 and D2 at the most insulating region in their respective resistance maps (at the CNP). **f**, Displacement field effect on the  $R_{xx}$  curve, taken from D1 along the charge neutrality line in **c**. The value of  $D$  for each curve is indicated next to it.

$T$ -dependent  $R_{xx}$  of D1 at selected points along the charge neutrality line in Fig. 2c, where  $D$  is varied. Although the effect of  $D$  in the high- $T$  range is not prominent, the curve at low  $T$  is clearly flattened by the application of a small  $D$ . Note that we present the data down to the lowest temperature below which the four-probe measurements become unreliable due to the huge resistance. Due to the lack of a well-established model for excitonic insulators, in Supplementary Section 8 we analyse the data based on both the standard activation formula expected for a conventional band insulator and the Efros–Shklovskii variable-range hopping formula expected for a Coulomb gap<sup>37</sup>. Neither formula describes the observed resistance within a decade of the temperature variation, as already reflected by the presence of the two regimes. In the scenario of a SOC gap, the observation of suppressed  $R_{xx}$  at low  $T$  would imply closing of the single-particle gap by  $D$ , which may be reasonable

as  $D$  breaks inversion symmetry and introduces spin splitting at the band edges<sup>25,33</sup>. However, we will experimentally rule out the band insulator scenario below. Our first-principle band structure calculation shows a semimetallic band structure prior to the exciton formation. It also shows that  $D$  not only introduces spin splitting but also enlarges the Fermi pockets of both electrons and holes simultaneously at charge neutrality (Supplementary Section 1). To produce a fully gapped excitonic insulator phase in the WTe<sub>2</sub> monolayer, one must gap out three Fermi pockets (two electron pockets and one hole pocket), which is different from the excitonic insulator formation in a simple two-band system with one electron pocket and one hole pocket. Our Hartree–Fock calculation shows that a full excitonic insulator gap can indeed develop in the pristine monolayer WTe<sub>2</sub> (Supplementary Section 1). Under the application of  $D$ , the enlarged Fermi surfaces are expected to reduce the excitonic gap



**Fig. 3 | Hall anomaly in the monolayer insulator.** **a**,  $R_{xx}$  as a function of  $n_g$  with fixed displacement field, taken from D1 at the various  $T$  values indicated. Inset: measurement configuration. **b**, The corresponding Hall response,  $dR_{xy}^{as}/dB$ , of the same device measured down to 80 K, below which the Hall measurement around the insulating state is no longer reliable, as indicated by the enhanced noise fluctuations at low  $T$ . **c, d**,  $R_{xx}$  and  $dR_{xy}^{as}/dB$  measured in D2 where  $n_g$  is varied by tuning  $V_{tg}$  with a fixed  $V_{bg} = 0$  V. The Hall coefficient  $R_H$  (right axis in **b** and **d**) is calibrated by a device-specific geometry factor (Supplementary Sections 3 and 4). The green lines in **c** and **d** indicate the expected  $R_H$  of a band insulator, that is,  $-1/(e(n_g - n_{g0}))$ , where  $n_{g0}$  is the location of the CNP labelled by the dashed vertical line.

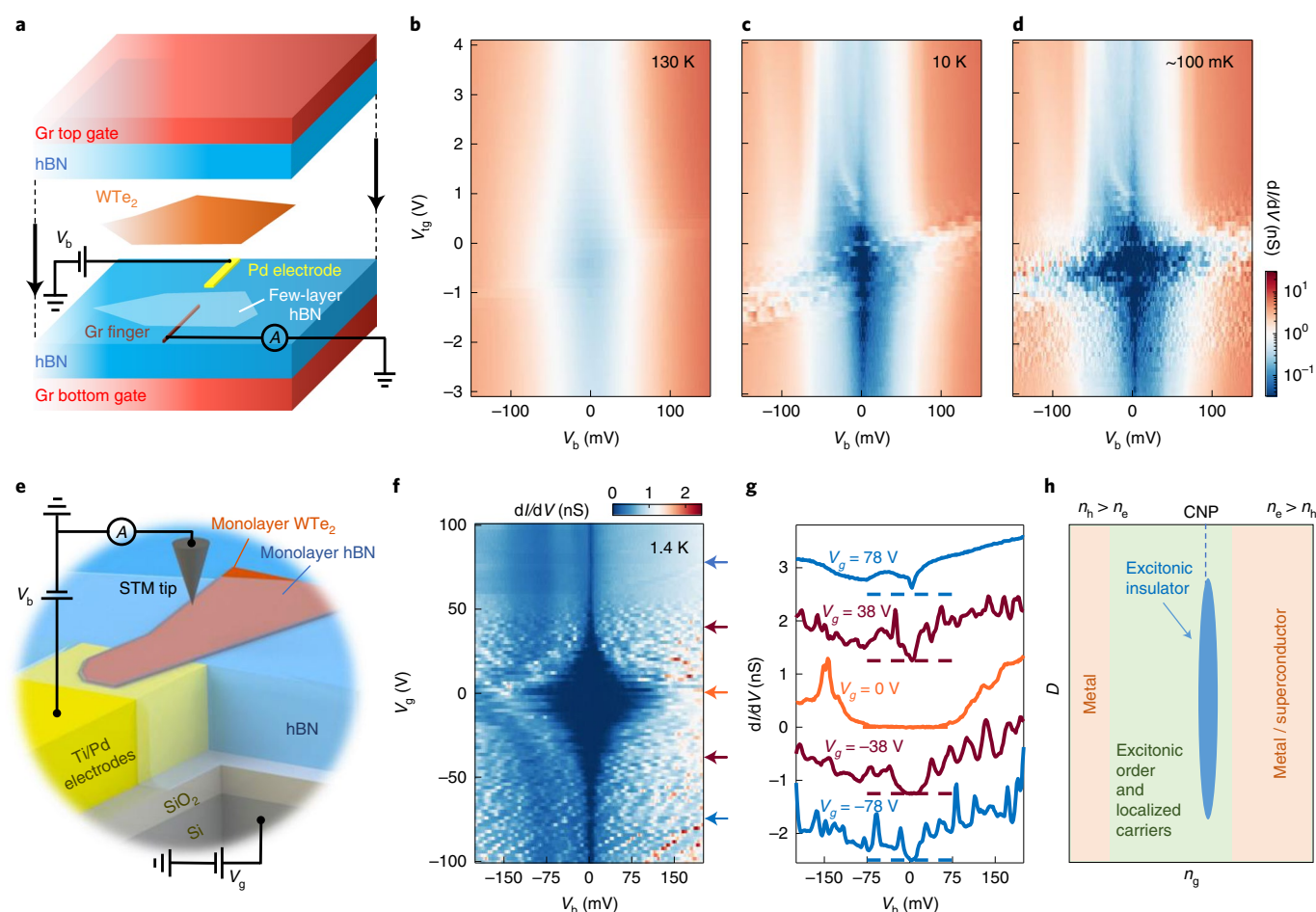
at specific spots in the Brillouin zone. For large  $D$ , small residual Fermi pockets may be created, coexisting with excitonic order. At low  $T$ , the residual pockets, if they exist, are expected to be localized.

In principle, an excitonic insulator may be distinguished from other insulators, such as band insulators or Mott insulators, by its Hall response in magnetic fields. In conventional insulators, the vanishing conductivity tensor when  $T$  is lowered corresponds to a diverging behaviour in both  $R_{xx}$  and Hall resistances ( $R_{xy}$ ). However, whereas the diverging  $R_{xx}$  is generic for an insulator,  $R_{xy}$  can deviate from such an expectation. An example is the so-called ‘Hall insulator’ observed in the vicinity of the quantum Hall liquid state, where  $R_{xx}$  diverges yet  $R_{xy}$  remains finite<sup>38,39</sup>. An excitonic insulator is another exception, which can be understood intuitively by considering an idealized case assuming that electrons and holes are symmetric. The formation of excitons will lead to a diverging  $R_{xx}$ . Yet  $R_{xy}$  in this idealized insulator is nevertheless strictly zero at all temperatures, because the contributions from electrons and holes cancel precisely. In real materials, electrons and holes may be asymmetric (for example, they have different masses or mobilities), and then a non-zero  $R_{xy}$  can develop. However, the opposite contributions from electrons and holes in the correlated system will still produce anomalous behaviours<sup>40</sup>, such as the insensitivity to the insulating resistivity over a wide range of doping and  $T$ . Despite recent progress<sup>14–20</sup> in identifying an excitonic insulator using spectroscopic approaches, as far as we know its intrinsic transport properties, including the Hall response, remain elusive. For instance, the prime excitonic insulator candidate  $\text{TiSe}_2$  is typically a semimetal even at low  $T$ <sup>41,42</sup>, preventing transport access to the insulating gap. Our

monolayer  $\text{WTe}_2$  devices are well suited for pursuing such observations as the carrier concentrations can be controlled precisely in high-quality samples.

The key findings in our Hall measurements are summarized in Fig. 3, where we plot the gate-dependent  $R_{xx}$  and the corresponding Hall coefficient  $R_H$  measured in devices D1 and D2 under decreasing  $T$ . Determining the  $R_H$  of an insulator is challenging as a slight misalignment of the Hall probes will result in strong mixing signals from  $R_{xx}$ . We apply the standard anti-symmetrization process to extract  $R_H$  by sweeping the out-of-plane field ( $B$ ) in both directions, namely,  $R_H \equiv \alpha dR_{xy}^{as}/dB$ , where  $R_{xy}^{as}$  is the asymmetric component of  $R_{xy}$  (Supplementary Section 9) and  $\alpha$  is a factor that accounts for the device geometry (Supplementary Sections 3 and 4). At high  $T$  (around 200 K), the monolayer behaves like a semimetal where a sign change of  $R_H$  occurs in the hole-dominant side away from the CNP (Fig. 3b,d), agreeing with the semiclassical expectation that  $R_H$  changes its sign at  $n_h = (u_e/u_h)^2 n_e$ . Here  $n_h$  ( $n_e$ ) is the density of holes (electrons) and  $u_h$  ( $u_e$ ) is the corresponding mobility. The anomaly is that, whereas  $R_{xx}$  rapidly increases when either  $T$  is lowered or doping is reduced to the CNP,  $R_H$  is quite insensitive to the insulating  $R_{xx}$  down to the lowest  $T$  for reliable Hall measurements. For instance, whereas the sharp  $R_{xx}$  peak reaches a value of approximately 0.6 MΩ at 80 K in D1, the overall shape and values of  $R_H$  do not deviate much from those of its semimetallic profile at high  $T$ , despite being much noisier. The behaviour is in sharp contrast to that of the  $R_H$  of a band insulator, which is expected to develop a rapid sign change accompanied with the  $R_{xx}$  peak and a diverging behaviour when approaching it from either side (see green curves in Fig. 3b,d and the





**Fig. 4 | Signature of correlations and the metal-insulator transition revealed by tunnelling spectroscopy.** **a**, Schematic for the vdW tunnelling devices used in our measurements, where a few-layer hBN flake serves as the tunnelling barrier. Top and bottom graphite gates are employed. The measurement configuration is sketched as well (A denotes a current meter). **b–d**,  $dI/dV$  tunnelling spectra as a function of sample bias  $V_b$  and top-gate voltage  $V_{tg}$ , taken from device D4 at selected  $T$ . The bottom-gate  $V_{bg}$  is fixed at 3 V to enhance the conductivity of the monolayer outside the tunnelling junction. The tilted lines that appear in the insulating regime may arise due to the effect of probe-induced doping. **e**, Schematic for the STM device (D7) used in our study, where a monolayer hBN is used to protect the  $WTe_2$  flake while allowing tunnelling experiments. A silicon bottom gate is employed. **f**, Gate-tuned tunnelling spectra taken from D7 in a 1.4 K STM system. **g**,  $dI/dV$  spectra at selected  $V_g$  indicated by the coloured arrows in **f**. The curves are shifted vertically to enhance visibility; dashed lines indicate the corresponding zero conductance for each curve. **h**, A sketch of the electronic phase diagram of the monolayer at low  $T$  under varying  $D$  and  $n_g$ . At ultralow temperatures, the metallic phase at the electron side will turn into a superconductor.

observations in gapped graphene<sup>43,44</sup>). The observed  $R_H$  approaches the green curve in the doped metallic regime, but the Hall characteristics of a conventional insulator are clearly absent in our devices. The two devices with different disorder strengths show consistent behaviours. Although disorders have produced a substantial change in  $R_{xx}$ , including an order-of-magnitude change in the peak width, their effect on  $R_{xy}$  is nevertheless not dramatic. If only the  $R_{xy}$  data (Fig. 3b,d) are considered, there is no sign of the formation of an insulator state. By contrast, the  $R_{xx}$  data have clearly shown an insulator state at a specific doping (the CNP). This Hall response of the monolayer insulator behaves like a semimetal rather than a conventional insulator. These observations of the decoupled behaviours in  $R_{xx}$  and  $R_{xy}$  suggest that the appearance of the low-temperature insulator state is not due to the depletion of carriers; instead, it is due to the correlations between electrons and holes at the CNP (that is, excitonic pairing between an exactly equal number of electrons and holes).

We further confirm the correlated nature of the insulator by gate-tuned tunnelling spectroscopy based on both van der Waals (vdW) tunnelling spectroscopy and STM. In vdW tunnelling devices,

we fabricate narrow graphite fingers (approximately 100 nm wide) underneath the  $WTe_2$  flake separated by a few-layer hBN tunnelling barrier (Fig. 4a and Fig. S4 in Supplementary Section 2). At large bias, our devices show consistent results with earlier STM studies on samples grown on graphene<sup>27,34</sup> (Supplementary Section 10). The goal here is to reliably measure the low-energy behaviour (less than 100 meV) in the pristine monolayer, which is key to understanding the insulating state. In Fig. 4b–d, differential conductance  $dI/dV$  is plotted under varying d.c. sample bias  $V_b$  and the top-gate voltage  $V_{tg}$ , measured in a vdW device (D4) at a selected  $T$ . Although almost no feature appears in the map at high  $T$  (except the gate independent phonon characteristics<sup>45</sup>; Supplementary Section 10), a tunnelling gap centred at zero bias clearly develops at low  $T$  near the CNP ( $V_{tg} \approx 0$  V). The gap, U-shaped with a size of about 47 meV (Supplementary Section 11), closes when the monolayer is doped with either electrons or holes (Fig. 4d), confirming the metal-insulator transition observed in transport.

Qualitatively similar results are observed in our STM measurements. For the STM device (D7), monolayer hBN was used to cover the  $WTe_2$ , protecting the flake but still allowing electrons to tunnel

through (Fig. 4e and Supplementary Section 2). The corresponding STM  $dI/dV$  map and typical spectra taken at selected gate voltages ( $T=1.4\text{ K}$ ) are presented in Fig. 4f,g. At high doping, the spectra feature a V-shaped linear suppression of the  $dI/dV$  signal towards Fermi energy, consistent with the presence of a Coulomb gap<sup>37</sup> in the metallic regime due to finite disorders in the sample. As the doping is reduced towards the CNP, the linear suppression consolidates so that  $dI/dV$  at zero bias reaches zero and then transforms into a fully depleted U-shaped hard gap at the CNP with a size of about 91 meV, again signifying the metal–insulator transition (Fig. 4g). Consistent results are observed when the STM tip is engaged at different sample locations (Supplementary Section 12), as well as in two additional vdW tunnelling devices (D5 and D6; Supplementary Section 13). Our data are distinct from those of the previous STM study<sup>34</sup> on the  $\text{WTe}_2$ /graphene stacks with doping controlled by atomic dopants, where a different screening environment and strong disorders are expected. There, a V-shaped soft gap was observed at all doping levels and no clear signature of the metal–insulator transition was seen<sup>34</sup>. We note that the graphene substrate is known to greatly reduce exciton binding energy, as demonstrated for optical excitons in 2D semiconductors<sup>46</sup>. Our tunnelling experiments on pristine monolayer  $\text{WTe}_2$  demonstrate a clear contradiction to any band insulator scenario, including a strain-induced band insulator<sup>47</sup>, as a conventional band gap, with or without a correlation-modified gap size, will shift its bias position when the Fermi level is tuned away from the gap. Our data reveal a correlation-induced gap that is always pinned at zero bias. This observation, together with the gate-induced metal–insulator transition, is consistent with the presence of an intrinsic excitonic insulator gap at the CNP (see Supplementary Section 14 for further discussion).

We summarize our observations by sketching a low- $T$  electronic phase diagram of the monolayer under varying  $D$  and  $n_g$  (Fig. 4h). Metallic phases reside at high doping levels in either the electron- or hole-dominant side, whereas reducing  $n_g$  leads to insulating behaviours. Our systematic transport and tunnelling experiments on samples of controlled quality imply an intrinsic correlated insulator phase at the CNP in the clean limit of the pristine  $\text{WTe}_2$  monolayer. The results rule out the scenario of a band insulator and support the presence of an excitonic insulator phase. Electron localization fails to account for the observations at the CNP, yet it likely plays a role in real samples and may coexist with the excitonic order in the intermediate regime of the diagram. Our results call for future efforts in further understanding the nature of the ground states in monolayer  $\text{WTe}_2$ , where the interplay between the excitonic insulator phase and topology, as well as superconductivity, may open a new avenue for exploring correlated quantum states. The observations also identify the  $\text{WTe}_2$  monolayer as a promising material platform for constructing quantum devices that use coherent excitons in the ground state.

## Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at <https://doi.org/10.1038/s41567-021-01422-w>.

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## Methods

**Crystal growth and sample fabrication.** The vapour-grown  $\text{WTe}_2$  bulk crystals were grown using methods that were described in earlier studies<sup>36</sup>. The flux-grown crystals were synthesized by a solid-state reaction using Te as the flux. The starting material Te (99.9999%, Alfa Aesar) was first purified to remove oxygen contaminations and then mixed with W (99.9%, Sigma-Aldrich) in a molar ratio of 98.8:1.2. The raw materials mixture was sealed in an evacuated quartz ampoule and heated to 1,020 °C over a period of 16 h, then slowly cooled down to 700 °C at a rate of 1.2 °C h<sup>-1</sup> and then to 540 °C at a rate of 2 °C h<sup>-1</sup>. The crystals were obtained by a decanting procedure in a centrifuge. The detailed 2D device fabrication procedures and parameters are described in Supplementary Section 2.

**Transport and vdW tunnelling measurement.** The transport and vdW tunnelling measurements were performed in a Dynacool or Opticool Quantum Design system, or in a dilution refrigerator (Bluefors LD400). The dilution refrigerator was equipped with low-pass RC (resistor–capacitor) filters at room temperature and low-pass LC (inductor–capacitor) filters (Mini-Circuits VLFX-80+) at the mixing chamber stage. The measurement was conducted with standard lock-in technique at a low frequency (2–15 Hz). The a.c. excitation current used in transport measurement was on the order of 1 nA.

**Scanning tunnelling microscope measurement.** After the chip was swiftly mounted onto the sample holder, the sample was transferred into an ultrahigh vacuum chamber (<10<sup>-10</sup> torr) and baked at 350 °C overnight to remove residues from the surface of the vdW stack. The device was then installed into a lab-built 1.4 K STM and the measurement was performed with a tungsten tip prepared on a Cu(111) surface. The differential conductance was acquired by using the standard lock-in techniques with an a.c. excitation voltage at a frequency of 4,000 Hz.

## Data availability

The data that support the plots within this paper are available at <https://doi.org/10.7910/DVN/FFGQOX>. Other data that support the findings of this study are available from the corresponding authors upon reasonable request.

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## Author contributions

S.W. supervised transport and vdW tunnelling studies. A.Y. supervised STM studies. P.W. and G.Y. fabricated transport devices. Y.J. fabricated the vdW tunnelling devices, assisted by P.W., G.Y., M.O., N.F. and B.J. Y.J., P.W., and S.W. performed transport and vdW tunnelling measurements and analysed data. C.-L.C., Y.J., P.W. and X.L. fabricated the STM device. C.-L.C., G.F., X.L. and B.J. performed STM measurements and analysed data. Z.S., F.X., Y.X. and B.A.B. provided theoretical support. S.L., S.K., L.M.S., F.A.C. and R.J.C. grew and characterized bulk  $\text{WTe}_2$  crystals. K.W. and T.T. provided hBN crystals. All authors discussed the result and contributed to the writing of the paper.

## Competing interests

The authors declare no competing interests.

## Additional information

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