

A CMOS Dual-Mode Brain-Computer Interface Chipset with 2-mV Precision Time-Based Charge Balancing and Stimulation-Side Artifact Suppression

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Abstract—This article presents a multipolar neural stimulation and mixed-signal neural data acquisition chipset for fully-implantable bi-directional brain-computer interfaces (BD-BCIs). The stimulation system employs four 40-V compliant current-stimulators, each capable of sourcing/sinking maximum 12.75-mA stimulation current, connected to sixteen output channels through a high-voltage (HV) switch fabric. A novel time-based charge balancing (TBCB) technique is introduced to reduce the residual voltage on the electrode-electrolyte interface during the inter-pulse time interval, achieving 2-mV charge balancing precision. Additionally, an analytical study of the charge balancing accuracy for the proposed technique is provided. The recording system incorporates a dual-mode data acquisition architecture that consists of a 32-element front-end array and a mixed-signal back-end including analog-to-digital converters (ADCs) for both training (i.e., full-band) and decoding (i.e., base-band) operations. Leveraging the flexibility of the multipolar operation, stimulation-side contour shaping (SSCS) artifact cancellation is adopted to significantly suppress stimulation artifacts by up to 45 dB. SSCS method prevents the recording front-ends from saturation and greatly relaxes the dynamic range requirement of the recording system, enabling a truly bi-directional operation. The prototype chipset is fabricated in an HV 180-nm CMOS process and demonstrates a significant performance improvement compared to the prior art.

Index Terms—Bi-directional brain-computer interface (BD-BCI), stimulator, time-based charge balancing (TBCB), multipolar, stimulation-side artifact cancellation, dual-mode data acquisition, feature extraction, ultralow power.

I. INTRODUCTION

AN estimated half a million people worldwide suffer from spinal cord injury (SCI) [1] and its lifelong complications each year, and currently no biomedical solution exists to restore motor and sensory functions after SCI. Implantable bi-directional brain-computer interfaces (BD-BCIs) are emerging platforms that could enable future closed-loop therapeutic devices to restore sensorimotor function. Such BD-BCIs are required to perform two major concurrent tasks: stimulation

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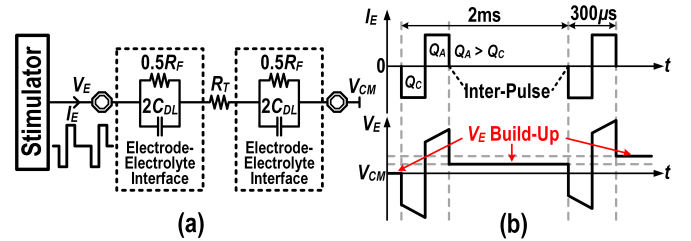


Fig. 1. (a) Brain stimulation electrical model, assuming electrode-electrolyte interfaces have the same impedance. (b) Typical waveforms of the stimulation current through the electrode, I_E , and the voltage appearing on electrode, V_E .

and recording. Electrical brain stimulation technique excites neurons in the brain by injecting current pulses through electrodes. To accommodate different modalities, stimulators are required to be highly configurable, especially in terms of stimulation current and voltage compliance. For instance, cortical stimulation using electrocorticography (ECoG) grids requires up to 10 mA of current to elicit artificial sensation, whereas deep brain stimulation (DBS) needs only a few hundreds of μA [2], [3]. Furthermore, the required voltage compliance must account for the tissue impedance for the maximum stimulation current, which can be as high as few k Ω [4]. Thus, stimulators, in principle, require high-voltage (HV) programmable supplies ranging from few volts to a few tens of volts.

The brain stimulation electrical model is shown in Fig. 1(a). The brain tissue is represented by a resistor, R_T , and each electrode-electrolyte interface is modeled as a double-layer capacitor, $2C_{DL}$, in parallel with a Faradaic resistor, $0.5R_F$ [5]. Fig. 1(b) shows the typical waveforms of stimulation current, I_E , and voltage, V_E , appearing on the electrode. V_{CM} denotes the body's quiescent potential. Because of the mismatch between positive and negative current pulses, a voltage build-up may occur on the electrode, as depicted in the inter-pulse time interval. The voltage across double layer capacitors slowly decays through each Faradaic resistor during this interval, leading to long-term unidirectional charge transfer. Consequently, this charge accumulation on the electrode leads to voltage build-up, causing electrode corrosion and tissue damage [5]. To solve this issue, several charge balancing techniques have been introduced by prior works. Passive charge balancing [6] performs electrode shortening by turning on a low resistive discharge path between V_E and V_{CM} in

the inter-pulse time interval to remove the residual charges in the interfaces. However, the discharging current is not well-controlled and determining the resistance of the discharge path requires a-priori knowledge of the interface characteristics. The charge-pack injection (CPI) technique [7]–[11] uses well-controlled charge packs to remove the residual voltage on the stimulating electrode following each stimulation, while avoiding false sensation. However, it requires a predefined charge for each pack, which highly depends on the interface characteristics. In addition, CPI suffers from a strict trade-off between compensation time (i.e., shorter compensation time with larger pack) and accuracy (i.e., higher accuracy with smaller pack). Dynamic current mirrors (DCMs) [12]–[14] monitor and balance the anodic and cathodic charges during stimulation. However, its charge balancing accuracy is limited due to the absence of closed-loop monitoring of the residual voltage and the inability to capture current transient mismatches. Offset regulation (OR) technique [6], [8], [15] creates a compensating current continuously injected to the interface as an offset current in the background. Although it monitors the voltage on the electrode in a closed-loop fashion, OR is unable to remove the residual charge after each stimulation pulse and requires a long settling time when the stimulator initially starts or the stimulation waveform changes. Other charge balancing approaches, such as inter-pulse charge control (IPCC) [6], do not incorporate well-controlled compensation current and pulse-width, thus leading to false sensation. Based on the work presented in [16], this paper presents a time-based charge balancing (TBCB) technique capable of establishing both closed-loop monitoring of the residual voltage and well-controlled charge injection to avoid false sensation. Additionally, TBCB breaks the tight trade-off between compensation time and accuracy, and performs effective charge balancing without requiring a-priori knowledge of the interface characteristics.

When being used to realize the closed-loop operation in BD-BCIs, electrical brain stimulation induces undesired artifacts in the neural recordings. The presence of artifacts imposes excessive dynamic-range requirement on the recording sub-system, which calls for artifact cancellation techniques. Recently, several studies [17]–[19] have demonstrated the significance of localizing tissue activation by shaping the electric field within the brain. In practice, the geometry of electrode grids poses a strict constraint on the location of brain stimulation. In addition, voltage distributions created by monopolar or bipolar stimulation cannot be confined completely to the vicinity of stimulating electrodes [20]. As such, these stimulations tend to cause severe artifacts, which may result in performance degradation or even saturation of the analog recording front-ends in a BD-BCI system. By employing multipolar and multi-site stimulation, the electric field potential changes induced by the current injections are localized [17], [18] and the stimulation artifacts propagating to the recording side are significantly suppressed [20], [21]. The proposed stimulation system is designed to accommodate multipolar and multi-site configuration as a way to localize neural activation, thereby achieving significant artifact suppression. It is worth noting that this multipolar stimulation requires each stimulator to

have independent cathodic and anodic currents, which cannot be merely realized by conventional H-bridge-based topologies [7], [22]–[24] despite the fact that they tend to exhibit less anodic and cathodic mismatch. This charge imbalance induced by mismatch is mitigated by the proposed TBCB technique, as will be explained in Section III-A.

Existing neural recording architectures based on conventional approach of acquiring brain signals with maximum frequency content are ill-suited for high channel-count real-time processing, as they consume significant power, thereby limiting the longevity of implantable BD-BCIs. One particular neural recording modality of interest is the minimally-invasive ECoG that is specifically useful for therapeutic implants targeting individuals with SCI condition. It has been observed that high spatiotemporal resolution ECoG recordings from primary motor cortex, M1, contain rich movement information (i.e., duration and speed) related to upper and lower extremities in γ -band, and in particular, high- γ (~ 80 – 160 Hz) band [25]–[29]. Hence, this notion inspires cognitive-driven signal acquisition and processing architectures that could potentially offer power-saving advantage by exploiting the intrinsic characteristics of neural signals, thus enhancing the system longevity. A plausible approach is to employ a dual-mode analog signal processing method in the neural data acquisition system, which facilitates extracting low-bandwidth neural features from high- γ band at the early stages of signal acquisition prior to digitization [30]. As a consequence, the dual-mode operation avoids the unduly high data processing rates and associated power dissipation in the digital back-end.

To realize a clinically-viable implantable BD-BCI, the aforementioned challenges are addressed in this work by introducing (1) precision time-based charge balancing, (2) stimulation-side contour shaping artifact cancellation, and (3) ultralow power (ULP), mixed-signal, dual-mode neural data acquisition. The rest of this paper is organized as follows. In Section II, the top-level description of the proposed BD-BCI system is provided. The intuition behind time-based charge balancing, stimulation-side contour shaping artifact cancellation, and ULP, mixed-signal, dual-mode neural acquisition are described in Section III. The circuit implementations of the stimulation and recording systems are illustrated in Sections IV and V, respectively. The complete measurement results are presented in Section VI, and finally, the concluding remarks are given in Section VII.

II. TOP-LEVEL DESCRIPTION OF THE PROPOSED BD-BCI

The proposed BD-BCI chipset consists of a stimulation and a recording system, as indicated in Fig. 2. Each system is designed to interface with the ECoG grid placed over the motor and sensory cortices. In order to establish a bi-directional link between the BD-BCI chipset and end-effectors (e.g., base-station and exoskeleton), the proposed BD-BCI system is envisioned to incorporate additional modules such as digital signal processor (DSP) and transceiver (TRX), as depicted in Fig. 2. In the next two subsections, each individual system and its high-level implementation is further described.

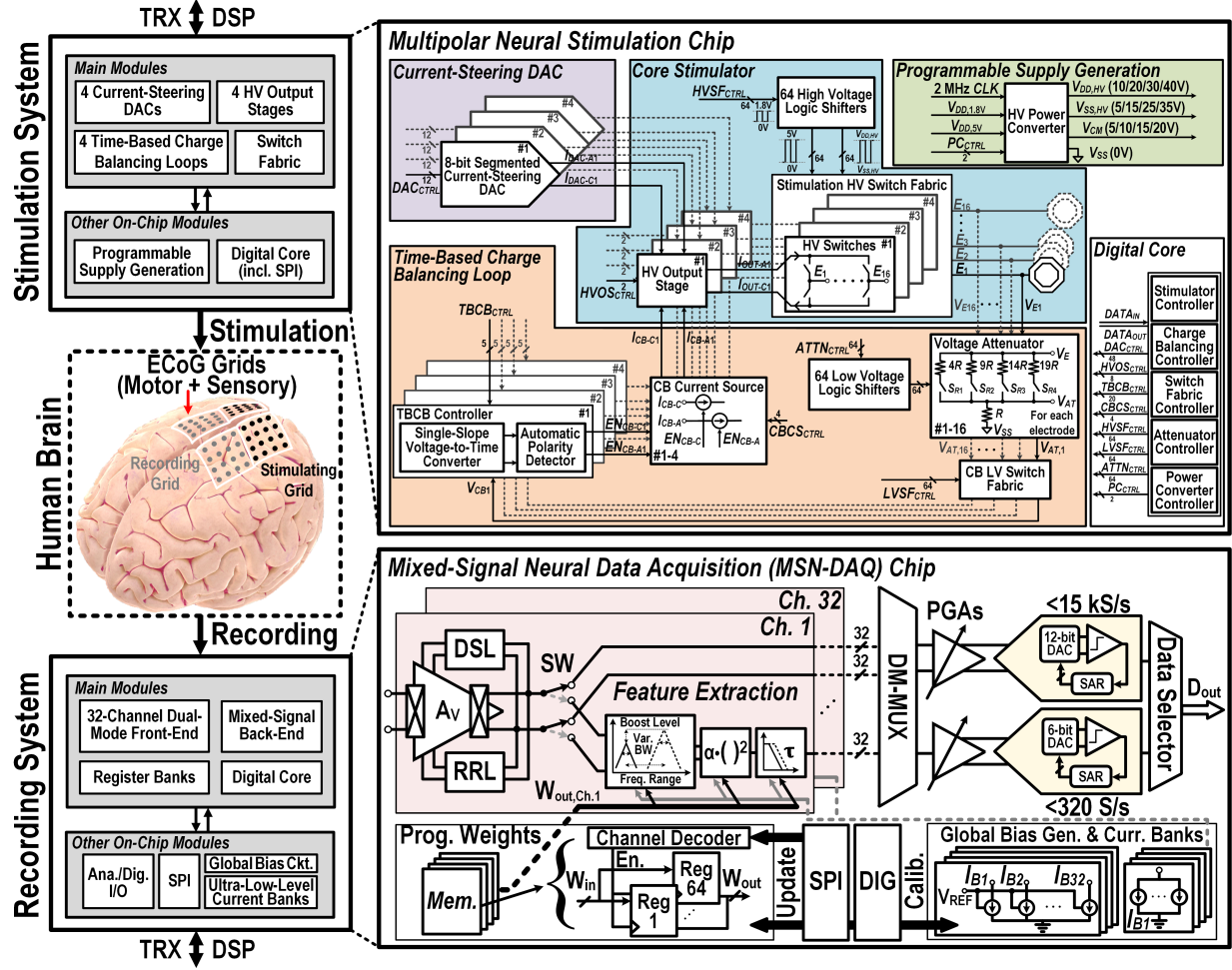


Fig. 2. Architecture of the proposed BD-BCI system.

A. Stimulation System

The proposed stimulation system is shown in Fig. 2, where at its core, four HV current-stimulators are connected to sixteen electrodes through an HV switch fabric. Each stimulator is capable of providing a maximum current of 12.75 mA, which is sufficient for cortical stimulation [2]. This current is generated by an 8-bit segmented current-steering DAC. In addition, a fully-integrated programmable power converter generates the necessary supply voltages to accommodate different bio-impedances.

The TBCB loop is enabled after each stimulation pulse. The loop starts with a voltage attenuator that senses the voltage on each stimulating electrode and lowers it down to 1.8-V low-voltage (LV) regime. Subsequently, an LV switch fabric in the loop feeds this voltage to the corresponding TBCB controller. The TBCB controller - comprising a single-slope voltage-to-time converter (SSVTC) and an automatic polarity detector (APD) - generates a control signal with its duration proportional to the voltage sensed at the TBCB controller input. The TBCB loop function is completed by generating a compensation current pulse whose duration is controlled by the output of the TBCB controller, which is then fed back to the core stimulator to perform charge balancing. The operation details of each building block will be discussed in Section IV.

B. Recording System

Fig. 2 illustrates the top-level system block diagram of the ULP mixed-signal neural data acquisition (MSN-DAQ). The 32-channel dual-mode front-end array is accompanied with register banks to store the channel-specific programmable weights for feature extraction. The mixed-signal back-end and digital core consist of dual-mode multiplexer (DM-MUX), programmable gain amplifiers (PGAs), and ADCs with distinct bit-resolution and bandwidth tailor-made for training (i.e., full-band (FB)) and decoding (i.e., base-band (BB)) modes. Other on-chip blocks include serial peripheral interface (SPI) for communication and configuration, and bias circuits for global current generation which are tuned by external reference voltages (V_{REF} 's) applied to on-chip diode-connected current mirrors, digitally-controlled ultra-low current banks for local bias and analog/digital input-output (I/O) modules. Details of operation will be disclosed in Section V.

III. IMPLANTABLE BD-BCI PREREQUISITES AND PROPOSED DESIGN PHILOSOPHIES

A. Time-Based Charge Balancing Technique

As mentioned in Section I, CPI is one of the most widely used charge balancing methods (Fig. 3). It uses a feedback mechanism to monitor the residual voltage $V_E - V_{CM}$ and

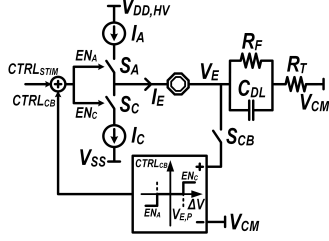
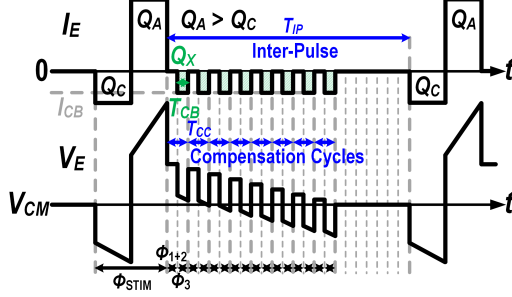


Fig. 3. Conventional CPI loop.

Fig. 4. Typical electrode current I_E and voltage V_E for the conventional CPI technique.

injects charge packs to the electrode-electrolyte interface in the inter-pulse time interval T_{IP} (Fig. 4) to compensate for the remaining charges [7]–[11]. Although this technique minimizes the residual charges on electrode after each stimulation pulse, and further provides a means of controlling both the maximum current and pulse-width to avoid false sensation, it suffers from the trade-off between charge balancing accuracy and compensation time. Through repetitive injections of compensation charge Q_X per cycle, the charge-pack injection loop is designed to converge to a desired residual voltage smaller than or equal to the charge-balancing voltage precision, $V_{E,P}$, after M cycles. This is mathematically expressed, as follows:

$$\frac{1}{C_{DL}} |Q_I - MQ_X| \leq V_{E,P} \quad (1)$$

Note that the gradual dissipation of charge on C_{DL} through a typically very large R_F is omitted. Eq. (1) implies that for a fixed compensation period of T_{CC} and an initial charge imbalance of Q_I ($Q_I = Q_A - Q_C$), $V_{E,P}$ can be reduced by assigning smaller values of Q_X , but at the cost of increasing number of compensation cycles, M (i.e., compensation time). Consequently, if M that satisfies Eq. (1) exceeds the maximum allowable compensation cycles $M_{\max} = \lfloor T_{IP}/T_{CC} \rfloor$, CPI will be incapable of removing all the residual charges prior to the next stimulation pulse, thereby failing to perform effective charge balancing. Although lowering T_{CC} can increase $M_{\max}$, Q_X is reduced accordingly in the CPI scheme where a fixed current I_{CB} - imposed by the patient's sensation threshold - is utilized for charge balancing (Fig. 4). A smaller Q_X , in turn, leads to a larger M despite a shorter T_{CC} (Eq. (1)). Therefore, T_{CC} scaling has a limited impact on the reduction of the total charge balancing time. Additionally, to ensure convergence of the CPI technique, $V_{E,P}$ and Q_X should be chosen such that $V_{E,P} > \frac{Q_X}{2C_{DL}}$. In practice, due to the lack of knowledge about electrode-electrolyte interface (e.g., C_{DL} value), this technique requires a brute-force search to find the largest value of Q_X under a certain $V_{E,P}$ requirement.

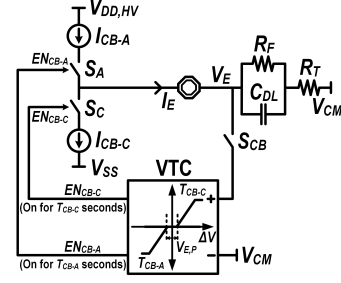


Fig. 5. Proposed TBCB loop.

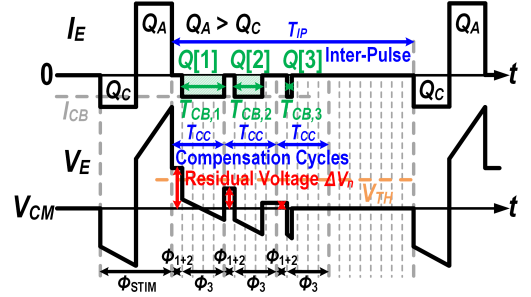
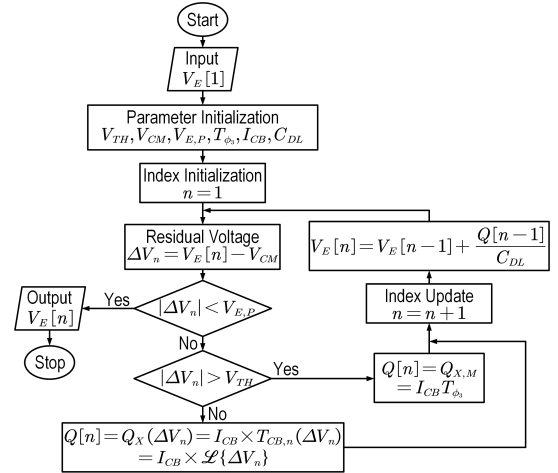
Fig. 6. Typical waveforms of the current through the electrode, I_E and the voltage on electrode, V_E for the proposed TBCB technique.

Fig. 7. Operation of the proposed TBCB loop.

Fig. 5 depicts the proposed TBCB technique. In essence, the TBCB loop consists of a voltage-to-time converter (VTC) and a compensating current source/sink. The TBCB loop operates in three consecutive phases within each compensation period T_{CC} , following the biphasic pulse stimulation, as illustrated in Fig. 6. During ϕ_1 , VTC is reset and auto-zeroing is performed to eliminate the input-referred voltage offset of the amplifier in VTC. In the next phase, ϕ_2 , switch S_{CB} is activated and the residual voltage $\Delta V = V_E - V_{CM}$ is applied to VTC, which conducts sample-and-hold operation on ΔV (Fig. 5). Both ϕ_1 and ϕ_2 are very small in duration, as shown in Fig. 6. Next, in ϕ_3 , the TBCB loop starts compensating for the residual charges. Referring to Fig. 6, the compensation current I_{CB} during ϕ_3 is a fixed amount, whereas the compensation time $T_{CB,n}$ associated with the n^{th} compensation cycle and produced by VTC is a continuously varying quantity proportional to ΔV_n sensed during ϕ_2 . Consequently, $Q[n]$ accepts a value commensurate with ΔV_n .

The detailed operation of VTC itself is, as follows: For

ΔV greater than a circuit-dependent threshold V_{TH} (Fig. 6), $T_{CB,1}$ is ultimately limited by the duration of ϕ_3 , T_{ϕ_3} (i.e., $T_{CB,1} = T_{\phi_3} = T_{CC} - T_{\phi_{1+2}}$). T_{ϕ_3} is obtained based on the patient's sensation threshold during clinical trials so as to avoid false sensation. The maximum allowable compensation charge, $Q_{X,M}$, is created during $T_{CB,1}$ (i.e., $Q[1] = Q_{X,M}$) by I_{CB-A} or I_{CB-C} to obliterate the residual charges over this T_{CC} period (Case 1), as shown in Fig. 6. It is worth mentioning that $Q_{X,M}$ could be much greater than Q_X in the CPI technique. On the other hand, for a residual voltage less than V_{TH} , VTC creates a $T_{CB,n}$ proportional to $V_E - V_{CM}$ and the operation falls into the linear region characterized by $T_{CB,n}(\Delta V_n) = \mathcal{L}\{\Delta V_n\}$, where $\mathcal{L}\{\cdot\}$ represents a linear function. Correspondingly, $T_{CB,n}$ only takes a portion of T_{ϕ_3} (Case 2) (Fig. 6). If $V_E - V_{CM}$ is very small and close to $V_{E,P}$, $Q[n]$ becomes much smaller than Q_X in CPI, thereby significantly increasing charge balancing accuracy. Finally, for residual voltages falling within a small sensitivity zone $\pm V_{E,P}$ (e.g., ± 2 -mV), the charge balancing loop will turn off for all the succeeding compensation cycles to avoid toggling (Case 3). The operation of the proposed TBCB loop is summarized by the flow-chart in Fig. 7 and is formulated, as follows:

$$\Delta V_n = \begin{cases} \Delta V_{n-1} + \frac{I_{CB} T_{\phi_3}}{C_{DL}}, & \text{if } |\Delta V_{n-1}| \geq V_{TH} \\ \Delta V_{n-1} + \frac{I_{CB} \cdot \mathcal{L}\{\Delta V_{n-1}\}}{C_{DL}}, & \text{if } V_{E,P} \leq |\Delta V_{n-1}| \leq V_{TH} \\ \Delta V_{n-1}, & \text{if } |\Delta V_{n-1}| \leq V_{E,P} \end{cases} \quad (2)$$

Although the cycle-by-cycle operation is discrete-time, within each T_{CC} , the TBCB loop essentially performs continuous-time operation. During the compensation cycle in which $V_{E,P} \leq |\Delta V_n| \leq V_{TH}$, the compensation charge $Q[n] = I_{CB} \times \mathcal{L}\{\Delta V_n\}$ is generated by a fixed charge balancing current I_{CB} over a “continuously varying” time interval, $T_{CB,n}$. This continuous-time operation draws a major distinction between TBCB and CPI, in that, the residual charge compensation is performed by quantized charge packs in CPI that inevitably yields a finite quantization error. Consequently, Eq. (1) will no longer hold for TBCB and $V_{E,P}$ value can, in fact, be arbitrarily small without the need for increasing compensation time. Therefore, the proposed TBCB technique mitigates the trade-off between compensation time and accuracy. In addition, as shown in Figs. 5 and 7, when ΔV_n comes very close to $V_{E,P}$, an arbitrarily small $Q[n]$ is generated and the condition of convergence ($V_{E,P} > \frac{Q[n]}{2C_{DL}}$) can be satisfied for an arbitrarily small $V_{E,P}$. Therefore, the charge balancing accuracy $V_{E,P}$ in TBCB is only limited by the imperfections, such as offset voltage created by transistor mismatches and charge injection of switches, and is independent of Q_I , charge balancing time, and the interface characteristics.

Fig. 8 shows three examples that compare the proposed TBCB technique with the conventional CPI method. The comparison is made under the assumptions that both TBCB and CPI use the same clock frequency to synchronize the charge balancing operation, and the detection phases ϕ_{1+2} in Figs. 4 and 6 take one clock period T_{CLK} for both

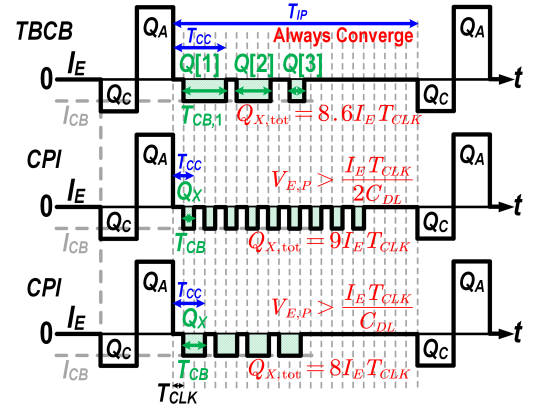


Fig. 8. Comparison of the proposed TBCB and the conventional CPI techniques.

(Fig. 8). In addition, the initial charge imbalance is assumed to be $Q_I = 8.6 I_E T_{CLK}$, which is a non-integer multiple of $I_E T_{CLK}$. For demonstration purpose, in the TBCB example, $T_{CC} = 5 T_{CLK}$, while in the two CPI examples shown in Fig. 8, $T_{CC} = 2 T_{CLK}$ and $3 T_{CLK}$, respectively. It is worth mentioning that the charge pack Q_X used in the two CPI examples are $I_E T_{CLK}$ and $2 I_E T_{CLK}$, respectively (Fig. 8). As mentioned above, the guaranteed convergence of TBCB allows $V_{E,P}$ to be very small such that the total compensation charge $Q_{X,tot} = Q[1] + Q[2] + Q[3] = Q_I$. On the other hand, the condition of convergence in CPI forces $V_{E,P}$ to be larger than the values indicated in Fig. 8. Additionally, the use of quantized charge pack in CPI leads to unmitigated charge errors. Specifically, for $Q_X = I_E T_{CLK}$, $Q_{X,tot} = 9 I_E T_{CLK}$ is close to the nearest integer of Q_I , leaving a charge error of $0.4 I_E T_{CLK}$. Similarly, for $Q_X = 2 I_E T_{CLK}$, a charge error of $0.6 I_E T_{CLK}$ will remain uncompensated, as shown in Fig. 8. Therefore, TBCB can achieve much higher charge balancing accuracy than CPI. It is noteworthy that T_{CC} can be greatly reduced to significantly lower $V_{E,P}$ in the CPI technique, thereby improving charge balancing accuracy. However, this leads to a dramatic increase in the clock frequency.

Unlike CPI that uses only the polarity information of the residual voltage, TBCB employs both the polarity and amplitude of ΔV to determine the polarity of compensating charge and pulse-width of I_{CB} . The amplitude detection and VTC operations in the TBCB technique increase power consumption when compared to CPI. Nevertheless, the major sources of power consumption in both methods stem from circuits responsible for the charge delivery to the tissue, because they operate in HV domain as opposed to the detection circuits operating in LV domain. Therefore, the extra power consumption overhead in TBCB contributes negligibly to the overall power consumption of the charge balancing operation.

B. Stimulation-Side Contour Shaping Artifact Cancellation

In this work, the stimulation-side contour shaping (SSCS) technique is used as the main artifact cancellation method. This technique is based on the electric field potential distributions within the brain tissue. To understand the voltage characteristics caused by the stimulation in the brain tissue under bi-directional multi-site stimulation and recording, the

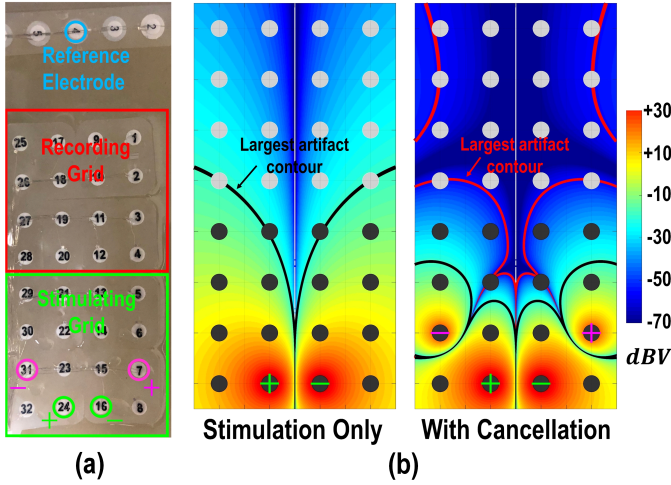


Fig. 9. (a) Physical configuration of the stimulation electrodes, stimulating and recording grids [20]. (b) Voltage spatial distributions under stimulation only and stimulation + cancellation conditions. Grey: recording grid. Black: stimulating grid. Green: primary stimulating source and sink electrodes. Magenta: canceling source and sink electrodes.

monopole model is applied to each current source or sink to calculate the voltages induced at various locations [20], [21]. One example of multipolar, multi-site stimulation involves a primary stimulating dipole and a canceling dipole to form two pairs of current sources and sinks [20]. As shown in Fig. 9, electrode 24 and 16 form a primary stimulating dipole and deliver 10 mA current to the tissue. Concurrently, a canceling dipole (electrode 7 and 31) with reversed polarity is introduced between the primary stimulating dipole and recording side to reshape artifact contours. With rapid attenuation of artifacts through the conductive medium of the brain, the cancellation magnitude can be made smaller than the primary stimulation (e.g., 1.25 mA). Hence, the canceling dipole causes no degradation of the artificial sensation, while significantly suppresses the artifacts on the recording electrodes without incurring any power overhead on the recording system. SSCS essentially reshapes the spatial distribution of artifacts, and as such, its performance is dependent on stimulation location. Nevertheless, since SSCS is on stimulation side, it is complementary to existing recording-side artifact cancellation techniques, such as adaptive filtering [24] and track-and-zoom [31]. Therefore, if used together, they can further suppress stimulation artifacts.

C. Ultralow Power Dual-Mode Neural Data Acquisition

Shown in Fig. 10 is a typical multi-channel neural interface consisting of a data acquisition (DAQ), a DSP, and a TRX. The neural recording architectures employed in DAQ are commonly based on conventional topologies such as capacitively-coupled InAmp+ADC [32], DC-coupled digitally-assisted amplifier [33] and direct conversion (time-based [34], delta-sigma [35], [36]) schemes. These approaches target acquisition and digitization of the brain signals across a wide range of frequencies (near DC up to 1 kHz) that leads to an excess dynamic range and bandwidth, resulting in an unduly high data throughput. Hence, a significant power and computing burden is placed on DSP and TRX, introducing a prominent

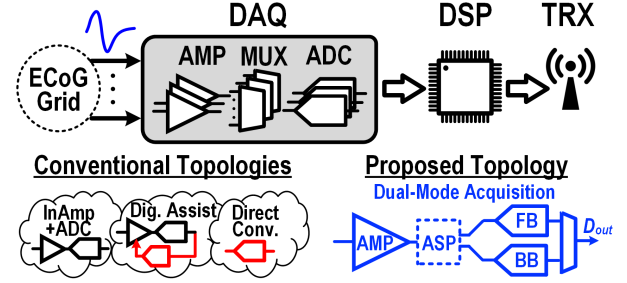


Fig. 10. Conventional and proposed topologies for data acquisition system.

data-processing power bottleneck for massive channel-count systems [37].

Since the most relevant physiological neural information, such as movement intentions, is often found within a fraction of brain signal frequency range (e.g., high- γ band) whose content requires significantly less dynamic range and bandwidth compared to the raw neural signal [29], a cognitive-driven DAQ is highly desired to address this major power bottleneck. Inspired by our work in [30], the proposed MSN-DAQ allows dual-mode acquisition that is capable of extracting useful neural features in the analog domain via a highly reconfigurable analog signal processing (ASP) unit, which significantly relaxes the system-level requirements (e.g., data throughput and power dissipation) to enable prolonged operation time in implantable BD-BCIs.

The power-saving advantage of the dual-mode operation in MSN-DAQ can be quantified by the power ratio, H , defined and expressed as:

$$H \triangleq \frac{P_{FB}}{P_{BB}} \approx \frac{S + 1}{\alpha \cdot S + \eta} \quad (3)$$

Eq. (3) is a compact form of Eq. (1) in [30] for $m=1$. $S = [1 + P_D/(N \times P_U)]^{-1}$, $\eta = (f_{s,FB}/f_{s,BB})^{-1}$ and α is a multiplier factor representing the power overhead introduced by the dual-mode operation in the analog front-end. N , P_D , and P_U represent the number of channels and power consumption of digital processing unit and front-end amplifier, respectively. Additionally, η represents the ratio of sampling rates in BB- and FB-mode operations. To gain better insight into H , each amplifier is assumed to consume no more than $0.8 \mu\text{W}$ per channel with $\alpha = 1.25$ and $\eta = 0.02$, as studied comprehensively in [30]. For a 32-channel neural signal acquisition and processing system, the recently published results from a fabricated 130-nm system-on-chip in [38] are used to estimate the power consumption of the digital back-end. Since a brain-state classifier with similar classification rate (e.g., 4 Hz) as reported in [38] can be employed for decoding movement intentions, its associated power dissipation (i.e., $476 \mu\text{W}$) is used to approximate H . In this case, the dual-mode operation can achieve a 12-fold improvement in the overall power consumption.

IV. STIMULATION CIRCUIT IMPLEMENTATION

A. Time-Based Charge Balancing Controller

A simplified block diagram of the TBCB loop is shown in Fig. 11(a). During the inter-pulse time interval, the attenuated

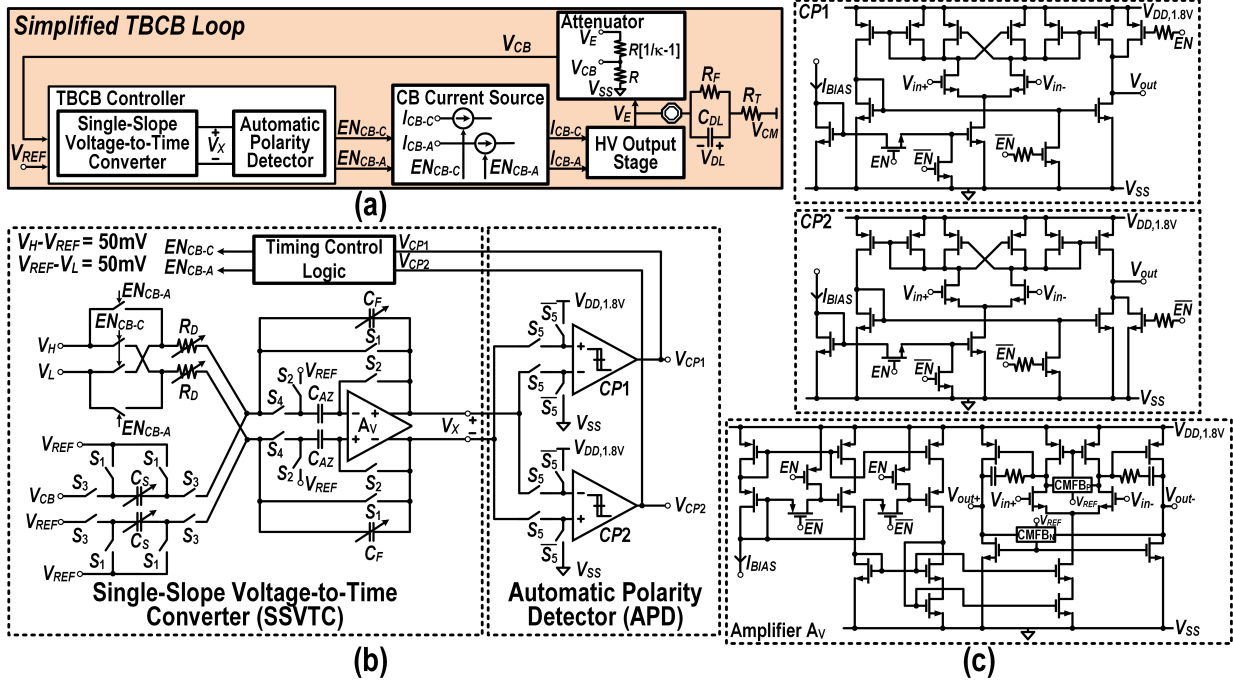


Fig. 11. (a) Simplified time-based charge balancing loop. (b) Circuit implementation of the TBCB controller. (c) Circuit schematics of comparators CP1 and CP2, and amplifier A_v .

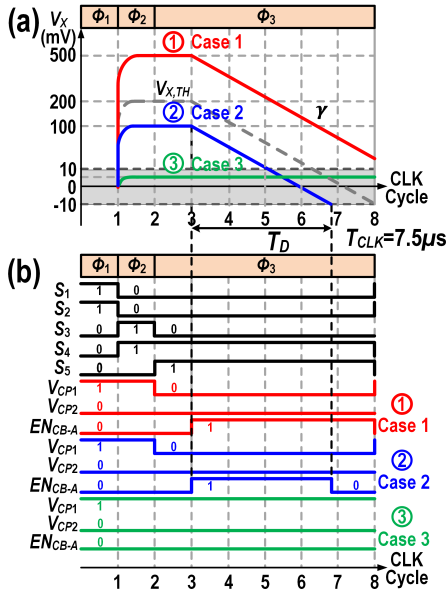


Fig. 12. (a) Single-slope voltage characteristics of V_X at the output of amplifier. (b) Waveforms of the control signals, typical waveforms at the output of two comparators V_{CP1} , V_{CP2} , and charge balancing current control EN_{CB-A} under $V_X > 0$ condition.

version of V_E , V_{CB} , is compared against V_{REF} in low-voltage domain and the voltage difference is processed by the TBCB controller. VTC, described in Section III-A, within the TBCB controller of Fig. 11(a) controls the duration of the charge balancing current, which is injected back to the electrode through HV output stage to perform charge balancing.

As mentioned in Section III-A, VTC entails three phases of operation in each compensation period, ϕ_1 , ϕ_2 , and ϕ_3 with ϕ_1 and ϕ_2 each taking one and ϕ_3 K clock cycles ($K = 6$ in Fig. 12(a)). In addition, depending on the input voltage amplitude, three cases may occur. The details of VTC

operation is shown in Fig. 11(b) and Fig. 12. Referring to Fig. 11(b) and Fig. 12(b), in the first phase of operation (ϕ_1), S_1 turns on and the charges on C_S and C_F are reset to zero. At the same time, S_2 turns on and the input-referred offset voltage of the amplifier A_v is stored on C_{AZ} to perform auto-zero offset cancellation. During this phase, S_5 is off and the output of the upper comparator $CP1$ is '1', while the lower comparator $CP2$ is connected in the opposite fashion and its output is thus '0'. In this phase, $[V_{CP1}, V_{CP2}]$ is logic '10' and the output EN_{CB-A} is off.

During ϕ_2 , S_{1-2} turn off and S_{3-4} turn on. The sampled and amplified version of the input voltage is stored on C_F and appears as V_X at the amplifier's output whose magnitude is proportional to the residual voltage on the electrode ($V_{DL} = -(V_E - V_{CM})$). Similar to operation in ϕ_1 , S_5 is still off, thus $[V_{CP1}, V_{CP2}]$ will keep its '10' state and EN_{CB-A} will remain off.

At the beginning of ϕ_3 , S_3 turns off and S_5 turns on. The two comparators in APD will determine the polarity of subsequent compensation current based on the V_X value attained at the end of ϕ_2 . To be more specific, consider that both comparators are designed to exhibit a hysteresis of $\pm V_{hys}$ ($= \pm 10$ mV). If V_X is larger than V_{hys} , $[V_{CP1}, V_{CP2}]$ will toggle from '10' to '00' in the first clock cycle of ϕ_3 , as shown in Fig. 12(b). Subsequently, in the next clock cycle, EN_{CB-A} will turn on to start injecting anodic compensation current to the electrode. Similarly, if V_X is smaller than $-V_{hys}$, $[V_{CP1}, V_{CP2}]$ will change from '10' to '11' and EN_{CB-C} rather than EN_{CB-A} will turn on (for simplicity, only the operation of $V_X > 0$ is shown in Figs. 12(a)-(b)). Finally, if V_X is within $\pm V_{hys}$, due to comparators hysteresis, $[V_{CP1}, V_{CP2}]$ will keep its logic state of '10', as shown in Fig. 12(b): Case 3, and neither EN_{CB-A} nor EN_{CB-C} will turn on.

Following the study of APD in determining the polarity

of charge balancing during ϕ_3 , the operation principle of the SSVTC in this phase is further illustrated. As shown in Fig. 12(a), at the beginning of the second clock cycle of ϕ_3 , EN_{CB-A} turns on and V_X starts to decrease at a constant rate γ . This rate is determined by the single-slope discharging of C_F through R_D ($\gamma = -\frac{V_H - V_L}{R_D C_F}$), as shown in Fig. 11(b). If $V_X > V_{X,TH} = -\gamma(K-1)T_{CLK} - V_{hys}$ at the end of ϕ_2 (Case 1), the discharging process through an enabled EN_{CB-A} will continue until the end of ϕ_3 (Fig. 12(a)). Otherwise, similar to Case 2, the discharging process will stop when V_X reaches $-V_{hys}$. In this way, the discharging time T_D ($T_D = -\frac{1}{\gamma}(V_X + V_{hys})$) is approximately proportional to V_X held at the end of ϕ_2 , and hence, to the residual voltage sensed by the TBCB loop. As a result, the operation of the TBCB controller follows the time-based charge balancing principle introduced in Section III-A.

The schematics of the two comparators in APD and the amplifier in SSVTC are shown in Fig. 11(c). For the purpose of power saving, an enable signal EN turns off the TBCB circuitry after charge balancing is achieved. Both $CP1$ and $CP2$ are comprised of a first stage with cross-coupled load to provide high-gain amplification and a differential-to-single-ended second stage to increase driving capability. The hysteresis is realized by the internal positive feedback in the first stage and by sizing the cross-coupled PMOS pair slightly larger than the diode-connected pair [39]. When the TBCB loop is disabled, the outputs of $CP1$ and $CP2$ are set to logic '1' and '0', respectively, to avoid false charge compensation. In SSVTC, a two-stage amplifier with wide-swing cascode current mirror as biasing circuit is used to provide high-gain and large dynamic-range amplification. The input-referred-offset of the amplifier is critical in determining the accuracy of the TBCB loop, and therefore, auto-zeroing is employed to eliminate it. On the other hand, the offsets due to the comparators' mismatches are divided by the closed-loop gain (40 dB) of the preceding amplifier when referred to the amplifier's input. Therefore, these offsets cause negligible degradation to the accuracy of TBCB.

The following analysis is conducted to quantify the charge balancing precision of the proposed TBCB technique. The attenuation ratio, κ , in this design can be tuned from 1/5 to 1/20 (Fig. 2). Accordingly, different ratios and their associated mismatches affect the charge balancing precision. Nevertheless, the forthcoming analysis considers the worst-case scenario (i.e., $\kappa = 1/20$). The charge-balancing operation is first examined for an ideal case of no circuit mismatches or other sources of error (e.g., current leakage at the interface). The attenuated residual voltage ($V_{CB} - V_{REF}$) appearing at the input of SSVTC is equal to $\kappa(V_E - V_{CM})$. After amplification (i.e., $A_V = -C_S/C_F$), the sampled and held value of V_X at the end of ϕ_2 is denoted as $V_{X,H}$. Note that the relative magnitude of $V_{X,H}$ and $V_{X,TH}$ ($V_{X,TH} = \kappa A_V V_{TH} = -\gamma(K-1)T_{CLK} - V_{hys}$) determines the operation case, as shown in Fig. 12(a). Once the residual voltage becomes negligible, as depicted in Case 3 of Fig. 12(a), the following condition must be satisfied in order for the charge balancing

operation to be completed:

$$|V_{X,H}| = \left| \kappa \frac{C_S}{C_F} [V_E(0) - V_{CM}] \right| < V_{hys} \quad (4)$$

where $V_E(0)$ is the initial electrode voltage at the beginning of the compensation period. Under the ideal conditions, Eq. (4) indicates that an arbitrarily small V_{hys} yields a small residual voltage V_{DL} on the interface. However, in reality, several sources of inaccuracy prevent us from choosing a very small V_{hys} , which will be further discussed.

During ϕ_1 and ϕ_2 , given that the resistive attenuator is used to convert V_E from HV domain to V_{CB} in LV domain prior to the amplification in SSVTC, the inaccuracies associated with this conversion significantly affect the charge balancing accuracy. To be more specific, two major sources of inaccuracies contribute to the degradation of charge balancing precision. The first one is the circuit mismatches in the resistive attenuator. Accounting for this inaccuracy, the modified attenuation ratio becomes $\kappa/[(1 \pm \epsilon)]$, where ϵ is the passive mismatch (typically 0.1%). Another source of error stems from the current passing through the attenuator. This current causes not only a small voltage drop across R_T which results in a V_{DL} different from $V_{CM} - V_E$ (Fig. 11(a)), but also slowly discharges V_{DL} . Considering these two non-idealities, according to Fig. 11(a), the voltage $V_{DL}(t)$ across the double layer capacitor is calculated as:

$$V_{DL}(t) = \beta V_{CM} \left(1 - e^{-\frac{t}{\beta R_\epsilon C_{DL}}} \right) - [V_E(0) - V_{CM}] e^{-\frac{t}{\beta R_\epsilon C_{DL}}} \quad (5)$$

where the total resistance in series with the electrode-electrolyte interface is $R_\epsilon = \frac{1}{\kappa} R(1 \pm \epsilon) + R_T$ and the coefficient $\beta = 1/(R_\epsilon/R_F + 1)$. The first and second terms denote the zero state and zero input responses, respectively. Considering that the speed of Faradaic reaction is very slow ($R_F \gg R_\epsilon$) [5], the degradation due to finite R_F is neglected ($\beta = 1$). Therefore, $V_{DL}(t)$ at the end of ϕ_2 is expressed as:

$$V_{DL}(t)|_{t=T_{\phi_{1+2}}} = - \left[V_E(0) \exp\left(-\frac{2T_{CLK}}{R_\epsilon C_{DL}}\right) - V_{CM} \right] \quad (6)$$

From Eq. (6), $V_{CB}(t)$ at the end of ϕ_2 is calculated as:

$$V_{CB}(t)|_{t=T_{\phi_{1+2}}} = \frac{R}{R_\epsilon} [V_{CM} - V_{DL}(t)]|_{t=T_{\phi_{1+2}}} = \frac{R}{R_\epsilon} V_E(0) \exp\left(-\frac{2T_{CLK}}{R_\epsilon C_{DL}}\right). \quad (7)$$

Another source of inaccuracy that degrades the charge balancing precision is the input-referred offset of the amplifier (A_V in Fig. 11(a)), which is significantly suppressed by $1/(A+1)$ using auto-zero offset cancellation in phase ϕ_1 (A is the open-loop gain of A_V). Additionally, the mismatches due to the charge injection of switches are resolved by using a fully differential switched-capacitor amplifier, as shown in Fig. 11(b). Thus, the voltage held by SSVTC at the end of ϕ_2 is derived from Eq. (7):

$$|V_{X,H}| = \left| \frac{C_S}{C_F} \left[V_{REF} - V_{CB}(t)|_{t=T_{\phi_{1+2}}} \right] \right| = \left| \frac{C_S}{C_F} \left[V_{REF} - \frac{R}{R_\epsilon} V_E(0) \exp\left(-\frac{2T_{CLK}}{R_\epsilon C_{DL}}\right) \right] \right| \quad (8)$$

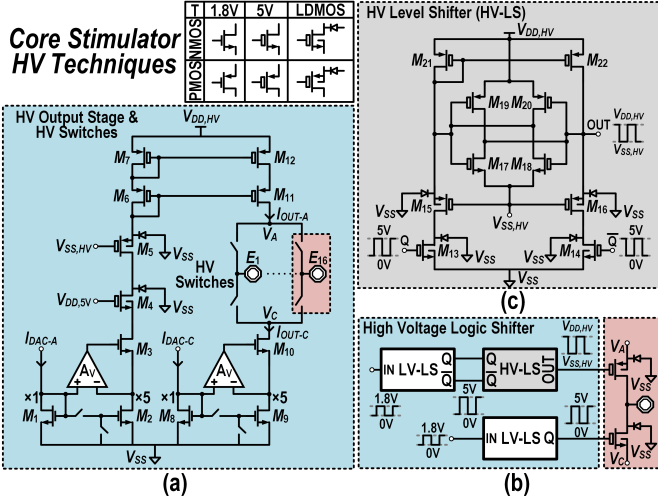


Fig. 13. (a) Schematic of one HV output stage, which is connected to 16 electrodes through 16 HV switch pairs. (b) Schematic of one HV switch and its logic control circuit. (c) Schematic of the HV level shifter (HV-LS).

in which $|A_V| = C_S/C_F$ (e.g., $|A_V| = 100$). As shown in Fig. 12(a): Case 1, if $|V_{X,H}| > V_{X,TH}$, T_D is a constant and equal to $(K-1)T_{CLK}$. If $V_{X,TH} > |V_{X,H}| > V_{hys}$, T_D is variable and the SSVTC employs linear voltage-to-time conversion (Case 2). To ensure convergence in Case 3 (similar to Eq. (4)), we should have $|V_{X,H}| < V_{hys}$. Note that the charge balancing accuracy, $V_{E,P}$, is the range of $V_{DL}(t)|_{t=T_{\phi_{1+2}}}$ (Eq. (6)) such that the condition $|V_{X,H}| < V_{hys}$ is satisfied. Thus, the variation range of $V_{DL}(t)|_{t=T_{\phi_{1+2}}}$ and the corresponding $V_{E,P}$ are expressed as follows:

$$\left(V_{CM} - \frac{R_e}{R} V_{REF}\right) - \frac{R_e}{R} \frac{C_F}{C_S} V_{hys} < V_{DL}(t)|_{t=T_{\phi_{1+2}}} < \left(V_{CM} - \frac{R_e}{R} V_{REF}\right) + \frac{R_e}{R} \frac{C_F}{C_S} V_{hys} \quad (9)$$

$$V_{E,P} = \left(V_{CM} - \frac{R_e}{R} V_{REF}\right) \pm \frac{R_e}{R} \frac{C_F}{C_S} V_{hys}. \quad (10)$$

The second term outside the parenthesis in Eq. (10) determines the charge balancing accuracy, while the term inside exemplifies an offset whose magnitude is purposely varied to be smaller than the one outside such that the second term remains dominant. Considering a passive mismatch of $\epsilon \sim 0.1\%$ [40] and assuming $R_T \ll R$, the second term approximately equals $\pm \frac{1}{\kappa|A_V|} V_{hys}$ ($= \pm 2$ mV). As for the term inside the parenthesis, V_{CM} and V_{REF} are 20 V and 1 V, respectively, with V_{REF} being tunable within ± 1 mV so as to compensate for the attenuator mismatch. The required 100 ppm accuracy (guaranteeing the second term in Eq. (10) to remain dominant) for V_{REF} is achievable both on-chip and using an off-chip voltage reference. Additionally, since R_T varies from several hundreds of Ω to a few k Ω for different stimulation electrodes [4], the effect of R_T cannot merely be compensated by V_{REF} tuning. In this work, $\frac{1}{\kappa}R$ was designed to vary from 0.5- to 3-M Ω , and was thus much larger than R_T .

B. High Voltage Output Stage

One HV output stage of the core stimulator is shown in Fig. 13(a). For cathodic stimulation, the current from the

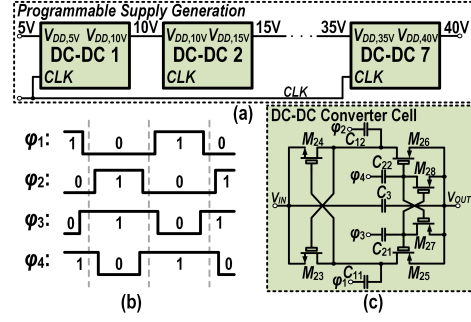


Fig. 14. (a) Programmable supply generation using a seven-stage charge-pump-based DC-DC converter. (b) Timing diagrams for all four phases of the clock. (c) Schematic of one DC-DC converter cell.

DAC I_{DAC-C} is mirrored and amplified 5 times to create the cathodic stimulation current I_{OUT-C} . For anodic stimulation, however, another dual-gate PMOS current mirror ($M_{6,7}$ and $M_{11,12}$), placed in HV deep n-well, is used to convert the current into the anodic stimulation current I_{OUT-A} . Unlike the H-bridge-based stimulator, in the proposed output stage, I_{OUT-C} and I_{OUT-A} are independent, which means, if multiple stimulators are enabled, all accompanying current sources and sinks will be well-controlled. In this way, the proposed system can perform multipolar, multi-site stimulation. The output of the HV output stage is connected to 16 electrodes through 16 HV switch pairs. Each pair is composed of a p-type and an n-type laterally-diffused metal-oxide semiconductor (LDMOS) switch, as shown in Fig. 13(b). Additionally, for the logic control circuit of the p-type LDMOS switch, an HV level shifter (HV-LS) is needed to translate 0- and 5-V to $V_{DD,HV}$ and $V_{SS,HV}$, corresponding to logic '0' and '1', respectively. The proposed HV-LS schematic is shown in Fig. 13(c). When Q is logic high (5-V), M_{13} is on and sinks a small DC current (10 μ A) from the diode-connected transistor M_{21} , lowering the gate voltages of M_{21} and M_{22} . At the same time, since M_{14} is off ($\bar{Q}$ is logic low), M_{22} is forced into the triode region and the output reaches $V_{DD,HV}$. On the other hand, if Q is logic low, M_{13} turns off, bringing the drain voltage of M_{21} up to $V_{DD,HV}$. At the same time, M_{14} is in triode region, lowering the output voltage to $V_{SS,HV}$. M_{15-16} pair limits the output swing and protects 5-V dual-gate transistors, and M_{17-20} form a pair of back-to-back inverters, boosting the speed of the HV-LS.

C. Programmable Supply Generation

To generate all the HV supplies for the HV output stages and switch fabric, a seven-stage charge-pump-based DC-DC converter [41] is designed, as shown in Fig. 14(a). Each stage employs a four-phase voltage doubler [42] in HV deep n-well (Fig. 14(c)), which boosts the supply voltage by 5-V. In steady state, V_{OUT} is charged to 5-V above V_{IN} . Depending on the logic state of CLK , either M_{23} and M_{26} or M_{24} and M_{25} turn on, and a voltage boost of 5-V is thus maintained between V_{IN} and V_{OUT} [43]. In addition, two-phase non-overlapping clock signals ϕ_{1-2} (Fig. 14(b)) are connected to C_{11-12} , while two-phase overlapping clock signals ϕ_{3-4} (Fig. 14(b)) are connected

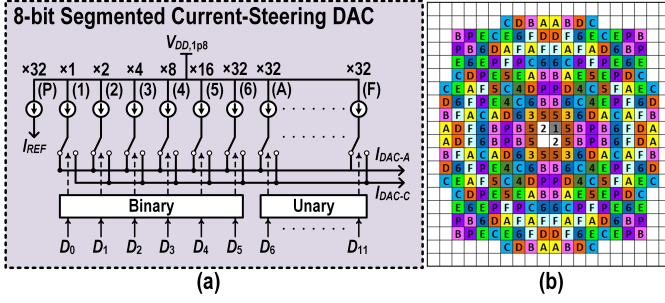


Fig. 15. (a) Schematic of one 8-bit segmented current-steering DAC. (b) Layout of the DAC.

to C_{21-22} to eliminate any possible charge reversal from V_{OUT} to V_{IN} [42].

D. 8-bit Segmented Current-Steering DAC

The 8-bit segmented current-steering DAC is shown in Fig. 15. A combination of unary and binary weighted architecture is adopted to improve DNL. Specifically, as shown in Fig. 15(a), bits 1 to 6 are binary weighted and the most two significant bits 7 and 8 (denoted as A to F), are unary weighted. The current-steering technique is used to increase the DAC speed such that the system can perform arbitrary current-waveform stimulation. Additionally, since for the majority of time, the stimulator and the corresponding current DAC are off, a relatively large reference current I_{REF} (weighted $\times 32$) is used to reduce the start-up time of the current DAC. The DAC layout (Fig. 15(b)) employs common centroid technique to mitigate first-order process variation and, for the most two significant bits, maintain their average distance to the center so as to mitigate the nonideality induced by mismatches.

V. RECORDING CIRCUIT IMPLEMENTATION

A. Dual-Mode Front-End and Analog Interface Circuits

To allow low-noise amplification of the neural signals, a chopper-stabilized amplifier based on folded-cascode structure is employed in the dual-mode front-end [30], as depicted in Fig. 16. Two auxiliary loops are placed between the output and folding nodes in order to minimize the output voltage offset and undesirable ripples. A DC-servo loop [44] facilitates the reduction of the output offset, and provides additional attenuation of low-frequency signals. Moreover, a ripple-reduction loop [44] ameliorates the chopping ripple caused by up-converted voltage offset of the input transistor pair. While chopping technique helps mitigate the flicker noise contribution of transistors, it further alleviates the degrading effect of transistor mismatches on common-mode rejection ratio (CMRR). To attain a higher CMRR, the input capacitors were sized appropriately to minimize their mismatches, and the common-mode feedback (CMFB) circuitry was enhanced by introducing the feedback to the tail current, and thus, achieving a higher loop gain.

Given that the amplified raw signals entail digitization with higher bit-resolution and sampling rate compared to the extracted neural features [30], it follows that channel serialization and post-multiplexing amplification in each acquisition mode

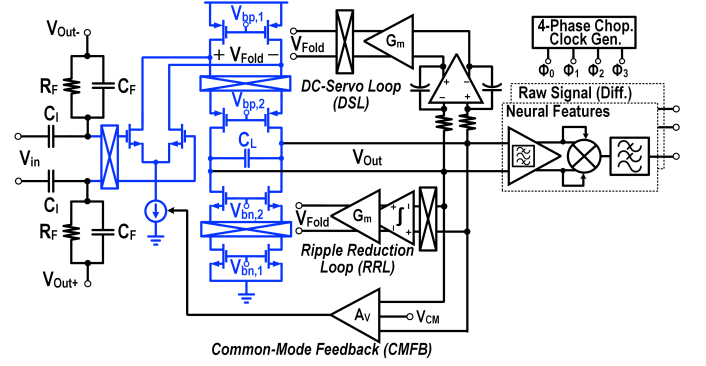


Fig. 16. Schematic of dual-mode front-end module, incorporating DC-servo loop, ripple reduction loop and common-mode feedback.

adhere to a drastically different settling speed requirement. In particular, FB-PGA must undergo less settling time to accommodate proper sampling of the signal by FB-ADC, which implies that a higher unity gain-bandwidth product is needed at the cost of increasing power dissipation. On the other hand, processing of neural features is carried out at much lower bandwidth, and therefore, BB-PGA consumes significantly less power in BB mode.

B. Successive Approximation Register ADCs

To facilitate the ULP operation and achieve the desired accuracy, successive approximation register (SAR)-ADC is adopted in the proposed neural data acquisition system. While both FB- and BB- ADCs follow the same operation principle, the latter has relaxed requirements which translate into fewer circuit design challenges. The differential N -bit (i.e., $N=6$ for BB, $N=12$ for FB) SAR-ADC, as depicted in Fig. 17, employs a V_{CM} -based binary-weighted capacitive DAC, an acquisition-mode-specific comparator and a compact modular non-redundant SAR logic and control with minimum circuit overhead. The unit capacitors (C_0) used in this design for 12- and 6-bit SAR-ADCs are 25 fF and 100 fF, respectively. The V_{CM} -based switching technique provides significant improvement in switching energy efficiency compared to the conventional charge redistribution scheme [45]. Moreover, the comparator in FB mode utilizes a multi-stage pre-amplifier chain with output offset cancellation (OOS) [46] to reduce the input-referred voltage offset and the kickback noise from the regenerative latch. Meanwhile, a conventional dynamic comparator with current source is used in BB mode because of the lower bit-resolution and reduced power dissipation. Additionally, the DAC and comparator are connected using twisted differential signaling [47] which helps mitigate common-mode noise (Fig. 17), an important attribute for FB-ADC.

Shown in Fig. 17, the SAR logic and control needed for V_{CM} -based switching are implemented with minimum combinational and sequential circuits. In specific, digital control circuitry (shaded in light blue) uses one D-flipflop, one inverter and two AND gates for each bit. The details of the circuit operation can be summarized as follows: During sample and hold phase, every D-flipflop in the digital control of SAR is reset by $CK_{S/H}$. This activates all S_3 switches in the capacitive DAC, causing every capacitor's bottom plate to be

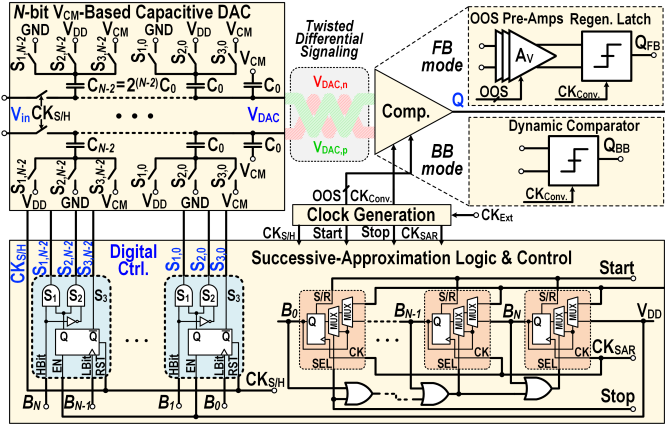


Fig. 17. Schematic of SAR-ADC comprised of V_{CM} -based capacitive DAC, comparator and digital logic & control circuitry.

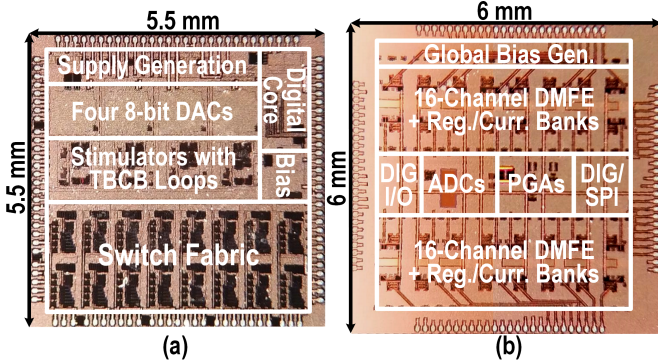


Fig. 18. Chip micrograph of the stimulation system (a) and the recording system (b).

connected to the common-mode voltage (V_{CM}), and makes ready for sampling. To accomplish the binary search algorithm, SAR logic is first initialized and a leftward-propagating pulse is generated in the shift register to mark each sequential step of bit-cycling. During the conversion phase, the comparator's output is captured synchronously with CK_{SAR} and following the relevant bit position, its value is stored in a MUXed D-flipflop (shaded in light brown). In addition, each capture-and-store interval represents a comparison window in which the direction of the binary search is decided, beginning with the most significant bit. The SAR control circuitry detects the onset of transitions in the bit-cycling sequence and generates the control signals for the capacitive DAC based on the stored bit value in a given comparison window. As a result, the corresponding pair of DAC switches (S_1 or S_2) is activated immediately after S_3 is disabled for each bit, performing the necessary charge addition/subtraction. This process continues until all the bits have been resolved for a sampled voltage value, followed by a new sample and hold phase.

VI. EXPERIMENTAL RESULTS

Both the stimulation and recording systems were designed and fabricated in an HV 180-nm CMOS technology occupying $5.5 \times 5.5 \text{ mm}^2$ and $6 \times 6 \text{ mm}^2$ of die areas, respectively (Fig. 18). The functionality of the stimulation system was verified first by electrical measurement and then tested by using *in vitro* phantom measurements. The performance

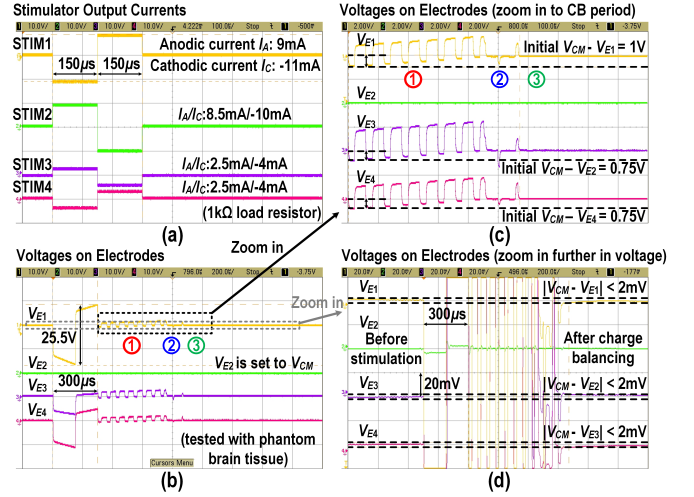


Fig. 19. (a) Stimulator output currents. (b) Voltages on electrodes. (c) Voltages on electrodes (zoom in to CB period). (d) Voltages on electrodes (zoom in further in voltage domain to demonstrate charge balancing precision).

of the recording system was verified by using pre-recorded bio-signals. In addition, the bi-directional measurement was conducted *in vitro* with phantom brain tissue.

The phantom brain tissue was created to mimic the cerebral cortex [20]. Specifically, table salt was added to deionized water, and the mixture was stirred evenly and heated until boiling. Then, agar powder was added into the boiling mixture gradually to create a gel compound. The compound was poured into a Petri dish to form the phantom brain tissue as shown in Fig. 20(a) and the Petri dish was placed in a refrigerator to cool down. The conductivity of phantom brain tissue was controlled by salt concentration [48] and was approximately equal to the conductivity of the human cerebral cortex [49]. Additionally, a thin layer of phosphate-buffered saline (PBS) was added on top of the phantom brain tissue to mimic the cerebrospinal fluid (CSF) [20]. Placed inside PBS, a standard subdural ECoG grid with platinum electrodes (4 mm diameter, 2.3 mm exposed, 10 mm spacing) was used for both recording and stimulation (Fig. 20(a)). The values of C_{DL} and R_F in the electrical model (Fig. 1(a)) were estimated by first measuring the impedance of the electrode-electrolyte interface across frequency and then applying curve-fitting to the impedance frequency response based on the electrical model. C_{DL} and R_F were approximately equal to 880 nF and 2 M Ω , respectively.

A. Stimulation System Measurement Results

The measurement setup of the stimulation system is shown in Fig. 20(a). A microcontroller (MCU) was used to control the stimulation system and the outputs of the stimulation system were connected to either a test board or phantom brain tissue through an ECoG grid (Fig. 9(a)). The test-board electrical test and the *in vitro* phantom measurement were used to characterize output currents and evaluate the performance of TBCB, respectively. For the test board measurement, the output of each stimulation channel was loaded with a 1 k Ω resistor and the output current was characterized by measuring the voltage across this resistor.

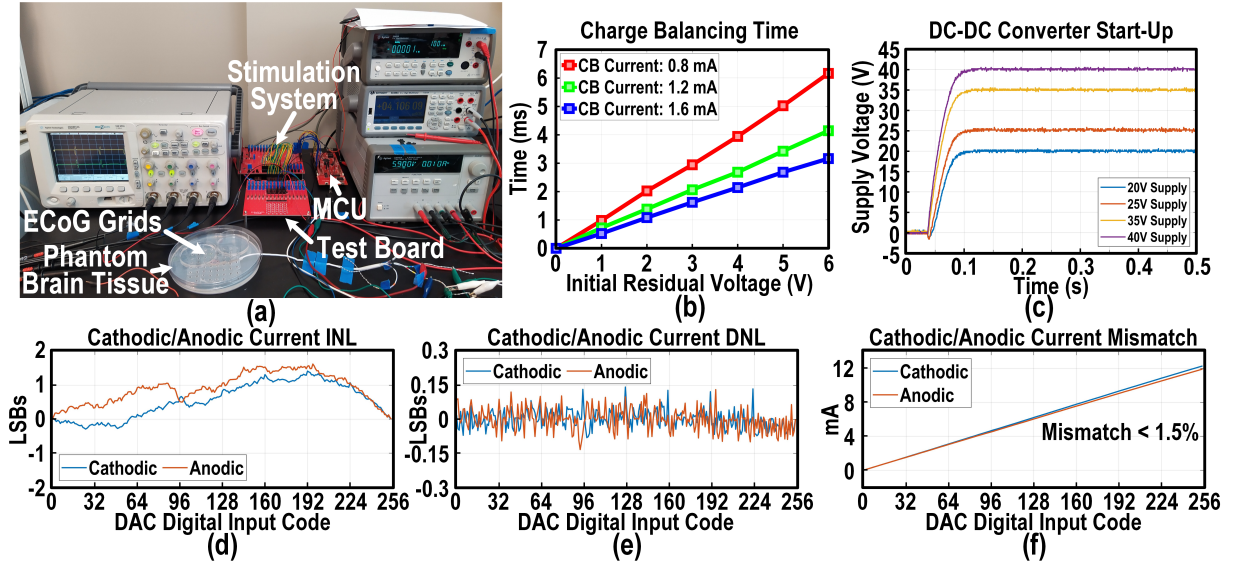


Fig. 20. (a) Stimulation system *in vitro* measurement setup. (b) Total charge balancing time for various compensation currents and initial residual voltages. (c) DC-DC converter start-up. (d) INL of the stimulator output current. (e) DNL of the stimulator output current. (f) Cathodic and anodic currents mismatch.

The measured characteristics of the stimulator output current is shown in Fig. 19(a) and Figs. 20(d)-(f). The measured static behavior shows that the DAC INL, DNL, and cathodic/anodic current mismatch are less than 1.4 LSB, 0.14 LSB, and 1.5%, respectively. To demonstrate the performance of multipolar, multi-site stimulation, all four stimulators were turned on concurrently, as shown in Fig. 19(a). For demonstration purposes, each stimulator independently delivered an unbalanced biphasic square pulse with 150 μ s pulse-width for each phase of the current injection. The measurement results for multipolar stimulation incorporating TBCB technique are shown in Figs. 19(b)-(d). As discussed in Section III-B, stimulators 1-2 (STIM1-STIM2) and 3-4 (STIM3-STIM4) were connected to electrode pair 24-16 and 31-7 to perform primary stimulation and cancellation, respectively (Fig. 9(a)). Given the fact that grid placement on the brain is governed by functional mapping to establish motor and sensory areas of interest, this typically allows physical separation between the stimulation and recording sites. In this demonstration, electrode pair 24-16 was chosen as the primary stimulation dipole to allow maximum distance between the stimulation and recording electrodes using a single grid. Electrode pair 31-7 was determined by the optimization algorithm [20] as the optimal location to achieve the maximum artifact cancellation. In real tissue, the monopole-model-based optimization algorithm [20] may not yield a globally optimum cancellation due to the complicated boundary conditions of the brain and unsatisfiable condition of infinitely far reference. However, the optimization algorithm is still effective and can provide better accuracy if an improved mathematical model is used to describe the electrical field distribution in the brain. Such study is beyond the scope of this work. In addition, one of the primary stimulation electrodes (i.e., electrode 16 corresponding to V_{E2} in Fig. 19(b)) is connected to V_{CM} as the reference electrode to collect the return stimulation current. The voltage on each electrode was measured, as shown in Fig. 19(b). Note that the stimulation current flowing through the reference electrode (corresponding

to V_{E2} in Fig. 19(b)) will charge and discharge the double-layer capacitor of the reference electrode, as well (Fig. 1). Therefore, the measured voltages V_{E1} , V_{E3} and V_{E4} , as shown in Fig. 19(b), are the summation of the residual voltages of the reference electrode and the corresponding stimulating electrodes. To better illustrate the transient waveforms during the TBCB operation, Fig. 19(c) shows a zoomed-in version of Fig. 19(b). In the absence of charge balancing mechanism, the initial residual voltage ($V_{CM} - V_E$) on electrode was 1 V for STIM1 and 0.75 V for STIM3 and STIM4. With TBCB technique being activated, the TBCB loop switches from Case 1 to Case 2, and finally to Case 3, and halts all subsequent charge balancing cycles (Fig. 19(c)). The charge balancing precision is demonstrated in Fig. 19(d), where the residual voltages on all electrodes are brought down to within ± 2 mV of the common-mode voltage.

Fig. 20(b) demonstrates the charge balancing time for various compensation currents and initial residual voltages under the condition of a fixed compensation period. As expected, the charge balancing time increases linearly with the initial residual voltage and decreases with an increase in the compensation current. As described in Section III-A, in practice, clinicians should determine the maximum compensation current in conjunction with the duration of ϕ_3 such that the charge delivered in each period T_{CC} causes no false sensation. The start-up waveforms of four selected output supply voltages of the DC-DC converter are depicted in Fig. 20(c). It takes less than 0.1 s for supply voltages to reach their nominal values.

B. Recording System Measurement Results

Operating at 1-V supply voltage, the MSN-DAQ chip achieves a minimum closed-loop gain of 42.5-dB, an input-referred noise of 1.03 μ V_{rms} across 2-200 Hz with an equivalent noise and power efficiency factors (NEF/PEF) of 2.37/5.62, and 88-dB average CMRR for 10 mVpp interference within 50-160 Hz range. Furthermore, the measured frequency response of MSN-DAQ in different gain modes

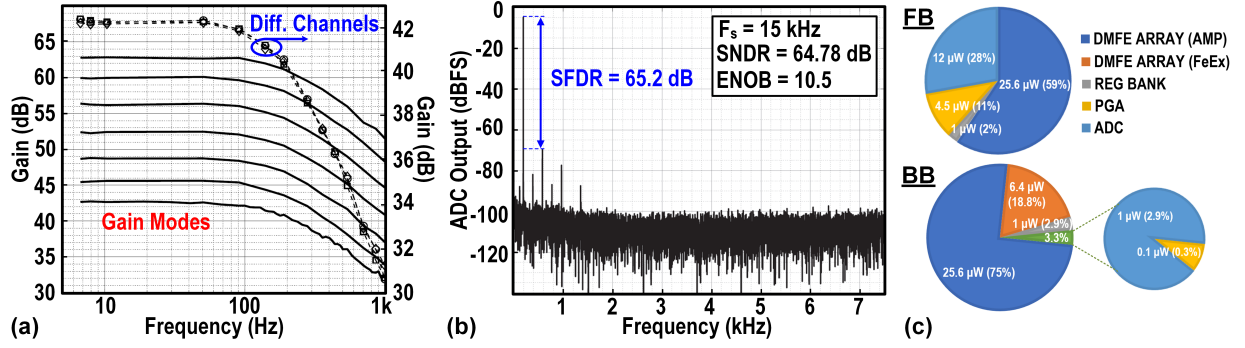


Fig. 21. (a) MSN-DAQ measured frequency response, (b) ADC measured output power spectrum and (c) power dissipation breakdown.

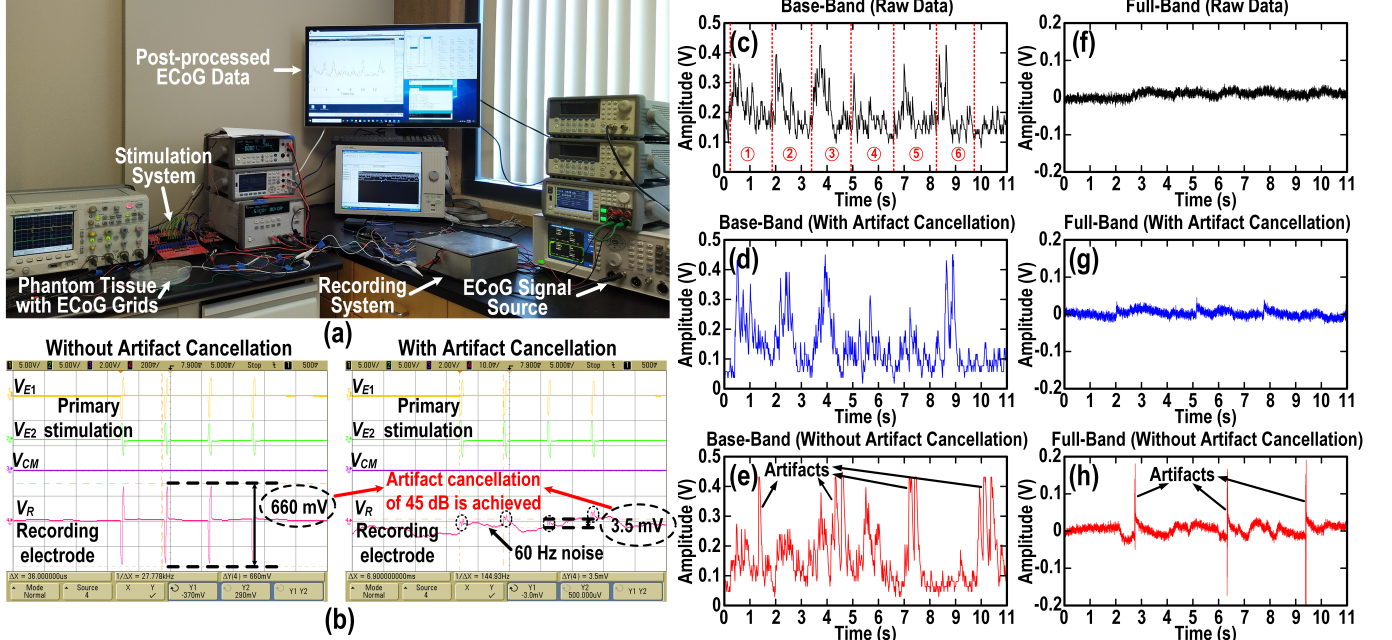


Fig. 22. (a) Bi-directional *in vitro* measurement setup. (b) Artifact V_R shows up on the recording electrode without/with stimulation side contour shaping artifact cancellation. (c) Post-processed base-band ECoG data without stimulation. (d) Base-band data with both stimulation and artifact cancellation. (e) Base-band data with stimulation but without artifact cancellation. (f) Full-band data without stimulation. (g) Full-band data with both stimulation and artifact cancellation. (h) Full-band data with stimulation but without artifact cancellation.

of one channel as well as across 3 neighboring channels is depicted in Fig. 21(a). The measured FFT from the 12-bit SAR-ADC output for a 193.17-Hz tone (i.e., upper edge of the frequency band) at maximum sampling rate of 15 kHz, as shown in Fig. 21(b), exhibits a signal to noise-and-distortion ratio (SNDR) of 64.78 dB, a spurious-free dynamic range (SFDR) of 65.2 dB, and an effective number of bits (ENOB) equal to 10.5. The power dissipation of each operating mode is further quantified in Fig. 21(c), exhibiting significantly reduced power consumption for PGA and ADC in BB-mode as compared to FB-mode operation.

C. In-Vitro Phantom Bi-Directional Measurement Results

The measurement setup and results for bi-directional *in vitro* phantom brain tissue experiment are shown in Fig. 22. Referring to Fig. 22(a), pre-recorded ECoG data was reproduced by a high-resolution signal generator and delivered to electrode 26 (Fig. 9(a)) to mimic neural signals. Concurrently, four channels of the stimulation system turned on. The primary

stimulation current (10 mA) was delivered through electrode pair 24-16 and the cancellation (1.25 mA) was delivered through 7-31 (Fig. 9(a)). This setup was employed based on the primary dipole stimulation and the optimal cancellation described in Section III-B and Section VI-A. Electrode 18 was chosen as the recording channel and was connected to both the recording system and one channel of the oscilloscope (denoted as V_R in Fig. 22(b)).

Fig. 22(b) demonstrates how the artifact, V_R , shows up on recording electrode with/without artifact cancellation. After applying cancellation, the artifact dropped from 660 mV to 3.5 mV with a suppression ratio of 45 dB. These measured artifacts contain both common and differential components, but only the differential component (which is a small portion) is sensed by the recording system. Therefore, the proposed SSCS technique is capable of suppressing stimulation artifacts effectively before reaching the recording system and thus, preventing the AFEs from saturation. Figs. 22(c)-(h) shows the post-processed data from the recording system. In particular, the extracted high- γ features from BB mode are

TABLE I
STIMULATION SYSTEM PERFORMANCE COMPARISON

Reference	TBioCAS 2016 [13]	BioCAS 2018 [15]	JSSC 2018 [6]	JSSC 2020 [24]	JSSC 2020 [31]	ISSCC 2020 [7]	JSSC 2021 [50]	ISSCC 2021 [51]	This Work
Number of Channels / Stimulators	1/1	6/6	1/1	4/4	32/32	8/8	16/16	1/1	16/4
I_{MAX} (mA)	3	10	5.12	2	1.5	0.775	1.35	0.2	12.75
Resolution (bits)	4	9	9	8	8	5	8	-	8
Charge Balancing Method	DCM+ Passive	OR	IPCC+OR	No	Passive	CPI	No	No	TBCB
Charge Balancing Precision	$\pm 13.2\text{mV}^a$ 6.6nA@3mA	$\pm 20\text{mV}$	$\pm 20\text{mV}$	-	-	$\pm 50\text{mV}$	-	-	$\pm 2\text{mV}$ 1nA@10mA ^a
Voltage Compliance (V)	12	49	22	22	3.3	4	3.3	1	40
Multipolar Stimulation	No	No	No	No	No	No	No	No	Yes

^aCalculated based on $2M\Omega R_F$.

TABLE II
RECORDING SYSTEM PERFORMANCE COMPARISON

Reference	TBioCAS 2017 [52]	JSSC 2017 [36]	JSSC 2018 [35]	JSSC 2019 [34]	TBioCAS 2020 [53]	JSSC 2021 [50]	ISSCC 2021 [51]	ISSCC 2021 [54]	This Work
Number of Channels	16	64	16	4	64	16	64	8-24	32
Supply Voltage (V)	1.8	1.2/2.5	0.8	1.2	0.5/2.5	0.6/1.2/3.3	0.5-1.6	1.8	1
Power/Channel (μW)	15	0.63	0.8	3.9	2.98	0.99	0.14	14.94/13.94	1.07(BB)/ 1.32(FB)
Artifact Cancellation	Mono/Bipolar Pole-Shifting	Passive	Fast Recovery	Artifact Tolerant	Template Subtraction	Artifact Tolerant	Artifact Tolerant	No	SSCS
Bandwidth (Hz)	0.3-7k	0.01-500	500	200	1-1k	1-500	10k	0.5-1k	2-200
CMRR (dB)	81	88	81	>75	76	>78	-	-	88
NEF/PEF	4.77/41.1	2.86 ^b /-	1.81/2.6	4.9/28.81	2.21/-	3.5/15.2	4.7/13.2	-/-	2.37/5.62
ENOB (bit)	7.9 ^a	11.7 ^a	10.7	13.2	15.7	9.7	8	11 ^e	10.5
IRN (μV_{rms})	4.57	1.13	0.99	1.3	1.66	2.6	-	2.72/2.31	1.03
Input Impedance ($M\Omega$)	-	0.99-1.02	>26	160	92	>1000	40 ^c /100 ^d	-	>44

^aCalculated. ^bAmplifier+ADC. ^cFor 25 kHz chopping frequency. ^dFor 10 kHz chopping frequency. ^eADC resolution.

shown in Fig. 22(c), exhibiting power modulations during six consecutive elbow flexion and extension periods as annotated. For base-band operation, Figs. 22(c)-(d) demonstrate the envelopes of the pre-recorded ECoG signals under no stimulation and stimulation with cancellation conditions, respectively. As expected, these two envelopes closely follow one another. However, in the absence of cancellation (Fig. 22(e)), the power envelope is severely contaminated by the stimulation artifacts. Similar results for full-band operations are shown in Figs. 22(f)-(g).

Tables I and II show performance summary and comparison between the proposed stimulation and recording systems and the prior art. The stimulation system incorporating TBCB technique achieves 12.75-mA maximum current, 40-V voltage compliance and 2-mV charge balancing precision, considered to be the lowest value on the record to date. Furthermore, the recording system achieves excellent performance that includes 88 dB CMRR, 10.5 ENOB and NEF/PEF of 2.37/5.62. The power consumption per channel is $1.07\mu\text{W}$ and $1.32\mu\text{W}$ for BB- and FB-mode operation, respectively.

VII. CONCLUSION

A companion chipset incorporating both stimulation and recording systems for fully-implantable BD-BCI applications was presented. The detailed operation of the high voltage compliance multipolar stimulation system together with the conceptual and analytical formulation of the proposed TBCB technique was provided. The neural stimulator achieves a record-breaking charge balancing precision of 2-mV and a maximum stimulation current capability of 12.75-mA. In addition, for the recording system, a fully-integrated $1\mu\text{W}/\text{channel}$

dual-mode neural data acquisition was demonstrated. Enabled by the multipolar operation, the SSCS artifact cancellation technique was adopted to significantly suppress the stimulation artifacts. Measurement results for the fabricated prototype in an HV 180-nm CMOS process further validated the performance of the proposed chipset.

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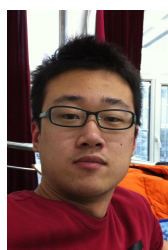
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