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Localized Self-Assembly of InAs Nanowire Arrays on Reusable Si Substrates for Substrate-Free Optoelectronics

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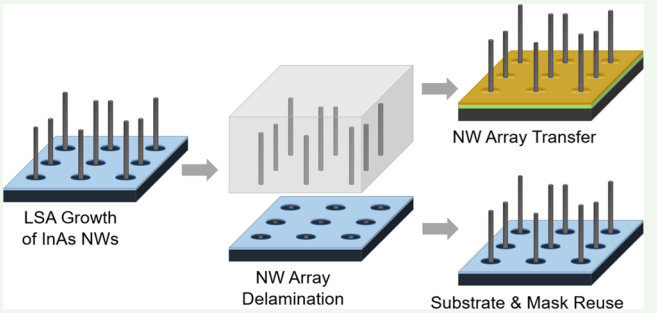
ABSTRACT: We present a low-cost and scalable approach for the synthesis of wafer-scale InAs nanowire (NW) arrays on photolithographically patterned, reusable Si wafers using a localized self-assembly (LSA) epitaxial growth technique. Conventional *i*-line lithography is used to define arrays of 500 nm diameter pores through 50 nm thick SiO_2 layers, which serve as the LSA mask. A two-step, flowrate-modulated growth sequence is implemented to optimize selective-area self-assembly of NW arrays with over 80% yield and excellent control over the placement of one NW, with a mean diameter of 130 nm, inside each 500 nm pore. As-grown NW arrays are delaminated from the growth substrate, enabling fabrication of flexible membrane devices as well as reuse of Si wafers and growth masks while preserving the template pattern fidelity. Reuse of Si substrates for III−V epitaxy is demonstrated with and without pre-growth substrate restoration treatments. In both cases, the yield of NWs on reused wafers is comparable to that achieved in the original growth run. Without substrate restoration procedures, the remnant base segments of NWs on parent wafers act as preferential sites for regrowth of vertical NWs. Transmission electron microscopy analysis reveals that the InAs lattice is coherently extended from the remnant NW base segments during regrowth. The delaminated InAs NW arrays are transferred to carrier wafers for the fabrication of substrate-free photodetectors through the use of an anchoring procedure, which preserves the original NW position and orientation. Under broadband illumination, the NW array-based photodetectors produce a photo-to-dark current ratio of 10^2, demonstrating the utility of the fabrication procedure employed. This work establishes a low-cost route toward III−V semiconductor-based flexible optoelectronics via LSA epitaxial growth of NW arrays on reusable Si wafers.



KEYWORDS: *InAs nanowires, localized self-assembly, regrowth, substrate reuse, photodetectors*

INTRODUCTION

Semiconductor nanowires (NWs) have received great interest for optoelectronic applications due to their unique properties, as well as their controllable epitaxial growth and *in situ* doping.[1−3] In contrast to conventional thin-film geometries, a broad range of material compositions can be grown heteroepitaxially in the NW form due to efficient strain relaxation.[4−6] In particular, III−V semiconductor NWs are promising for photodetector applications. Using periodic arrays of coaxial NWs, the traditional tradeoff between external quantum efficiency and response speed can be overcome due to orthogonalization of the directions of photon absorption and carrier collection.[7] Photodetectors that utilize NW array device geometries also benefit from highly selective resonant absorption and tunable spectral range of operation.[8−10]

Growth of periodically arranged III−V NW arrays can be realized through various template-assisted epitaxial methods. One of the most common NW growth techniques is the Au-assisted vapor−liquid−solid (VLS) approach.[11] High growth rates, wide variability in dopant concentrations, and excellent control over the NW crystal structure can be achieved using this growth mode.[12−15] However, the VLS approach faces several challenges, including (a) compositional phase segregation effects, particularly during growth of ternary alloys;[16] (b) undesired incorporation of Au atoms from the catalyst;[17,18] and (c) formation of graded junctions and compositionally smeared heterointerfaces due to the catalyst droplet reservoir effect.[19,20] Moreover, in some cases, Au nanoparticles must be selectively etched in order to better accommodate the growth of coaxial NW architectures or to mitigate optical reflection losses.[21,22] This introduces additional synthesis and processing complexity.

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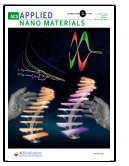
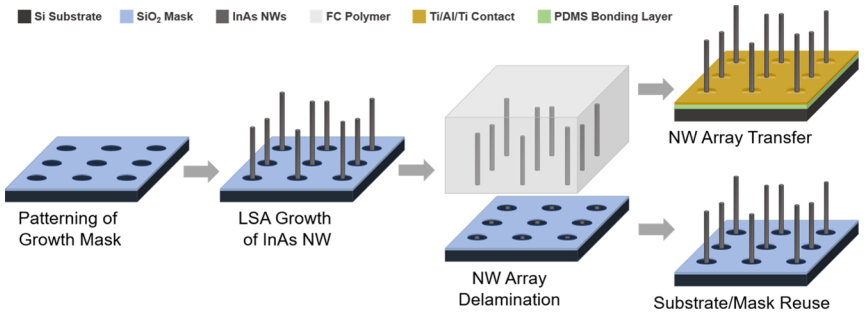


Scheme 1. Schematic Representation of LSA Growth of an InAs NW Array on a Photolithography-Patterned Si Substrate Followed by NW Array Delamination and Transfer for Subsequent Device Fabrication and Substrate Reuse



The above challenges can be either reduced or, at best, entirely overcome through the growth of NWs via selective-area epitaxy (SAE). The SAE growth mode enables several key advantages, including the ability to (a) grow complex core−shell heterostructures; (b) realize abrupt junctions and heterointerfaces; and (c) avoid the need for Au nanoparticle deposition and selective etching steps.[23]

Regardless of the growth mode, one of the main challenges for large-scale production of epitaxial III−V NW arrays is their synthesis cost.[24,25] Some synthesis costs are inevitable; these include, for example, the costs of instrumentation, operation, and precursor sources. However, other major cost contributions, such as those associated with the growth substrate, are largely reducible and can be separated into two categories (1) the cost of III−V wafers as the NW growth platform and (2) the lesser cost of pre-epitaxial processing of masking templates used for position-controlled synthesis of periodic NW arrays. Novel nanofabrication procedures that can overcome both cost streams are desired for large-scale implementation of III−V NW-based technologies.

Key substrate requirements for most applications include epitaxial guidance for the growth of vertically oriented NWs and the ability to serve as a robust carrier platform for handling during device fabrication. Low-cost foreign substrates such as Si(111) wafers fulfil both of these requirements, and they have been routinely used instead of bulk III−V wafers in order to considerably curtail the manufacturing costs.[26−28] However, site-specific NW synthesis still requires the patterning of masking templates on starting wafers, which presents an additional cost barrier. A possible strategy for simultaneously reducing pre-growth processing costs and complexity is to reuse Si substrates with existing predefined growth masks for site-selective and seed-free growth of III−V NW arrays. Such a process requires delamination of as-grown NWs from the "parent" Si substrate and transfer to alternative handling platforms for further device processing in order to accommodate substrate reuse and preservation of the original masking template. Moreover, Si substrates would need to be reused fewer times than III−V substrates for recovery of wafer costs.

For conventional SAE growth, masking templates are used to define the number density, position, and periodic arrangement of the NWs.[23] Growth templates are typically defined by first depositing a thin SiO_x or SiN_x layer on the substrate and subsequently patterning arrays of nanopores, which expose the substrate through the masking layer and serve as sites for preferential nucleation and NW crystal growth. The nanopore arrays can be defined using various lithography techniques, such as electron-beam lithography (EBL), nanoimprint lithography (NIL), or nanosphere lithography (NSL), followed by either wet-etching or reactive-ion etching for substrate exposure inside the nanopores. Each of these lithographic approaches have their own limitations. For example, EBL is a costly and low-throughput approach, while NIL suffers from reproducibility challenges, and NSL faces limitations with respect to the formation of patterns with long-range periodic order.[29,30] Comparatively, conventional photolithographic patterning for the fabrication of nanoporous masking templates is preferred with respect to cost, reproducibility, throughput, long-range order, wafer-scale manufacturing, and compatibility with existing foundry processing lines. However, conventional photolithography is commonly prohibited for the synthesis of NWs due to the resolution limit.

Using a combination of the above strategies, in this paper, we establish a procedure for the low-cost and wafer-scale, selective-area self-assembly of III−V NWs with sub-lithographic dimensions on photolithographically patterned and reusable Si substrates. We present an optimized growth parameter space with respect to the yield and aspect ratio of InAs NWs synthesized under a seed-free growth mode, whereby the NWs self-assemble inside predefined nanopores without occupying the full extent of each growth site. We chose InAs as a model material system for demonstration of this approach for two main reasons. First, InAs serves as the binary basis for the growth of ternary III−V NW systems that enable tunability across a wide spectral range from short-wavelength infrared (using ternary $In_xGa_{1-x}As$) to long-wavelength infrared (using ternary $InAs_ySb_{1-y}$) for applications in photodetection. Second, the lattice mismatch between InAs and the underlying Si substrate is sufficiently high to accommodate localized NW growth under a strain-limited, self-assembly regime (additional details regarding the growth mechanism are discussed further below).[31−36] We provide a procedure for the delamination of as-grown NW arrays, which allows for Si substrates to be reused without additional patterning of masking templates between subsequent regrowth steps. We demonstrate the growth of NW arrays on recycled substrates with comparable aspect ratio and yield upon regrowth. We provide two approaches for substrate reuse, including with and without the introduction of intermediate substrate restoration procedures, and we discuss the merits of both approaches. In the absence of an intermediate restoration procedure, remnant NW base segments left below the delamination fracture plane serve as preferential growth sites in subsequent growth runs. We show that the vertically oriented InAs NW lattice is coherently extended along the axial growth direction during regrowth cycles. Lastly, we demonstrate a unique process flow for the fabrication of substrate-free

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Table 1. Summary of Relevant Growth Conditions and NW Details for all Samples

sample	pre-growth processing	substrate reuse	growth sequence	growth time (s)	TMIn (μmol/min)	V/III	NW aspect ratio	single NW occupation yield (%)
A	solvent cleaning, 5 s BOE	no	growth step	1500	1	365	100 ± 12	31
B	solvent cleaning, 5 s BOE	no	nucleation step	60	16	22.8	11 ± 5	68
			growth step	1500	1	365		
C	solvent cleaning, 5 s BOE	no	nucleation step	30	16	22.8	34 ± 9	81
			growth step	1500	1	365		
D	citric acid etch solvent cleaning, 5 s BOE	yes	nucleation step	30	16	22.8	38 ± 10	75
			growth step	1500	1	365		
E	solvent cleaning	yes	growth step	1500	1	365	61 ± 11	80

NW-based infrared (IR) photodetectors that allows delaminated arrays to be transferred to foreign platforms while preserving the original position and orientation of the as-grown NWs. Scheme 1 shows the overall process flow for NW array growth, delamination, and transfer as well as substrate reuse. The main focus of this work is the locally confined self-assembly of InAs NWs with sub-lithographic dimensions on photolithographically patterned Si wafers and the reuse of the parent wafers for subsequent III−V crystal growth runs without the need for intermediate processing steps prior to substrate reuse. This work enables the reduction of manufacturing cost of optoelectronic devices through selective-area self-assembly growth of III−V nanostructures on reusable Si substrates.

EXPERIMENTAL DETAILS

Substrate Pattering and NW Growth. Si(111) wafers were used as the substrates for all crystal growth experiments. Masking templates were prepared by coating 150 mm "parent" Si wafers with 50 nm thick SiO_2 films via plasma-enhanced chemical vapor deposition, followed by conventional *i*-line lithography using a ASML PAS 5500/200 stepper and reactive ion etching (RIE) using a AME P5000 instrument to obtain wafer-scale arrays of hexagonally arranged nanopores with 500 nm diameter and 1000 nm pitch. Next, vertically oriented InAs NW arrays were grown using a 3 × 2″ close-couple showerhead AIXTRON metalorganic chemical vapor deposition (MOCVD) reactor. Three distinct sets of growth conditions were investigated (henceforth, referred to as Samples A, B, and C) under different group-III precursor flowrates in order to optimize the NW yield and single NW per pore placement. Prior to loading in the MOCVD reactor, samples were rinsed with standard solvents and the native oxide of the Si substrate exposed through each pore was etched during a 5 s buffered-oxide etching (BOE) treatment. Trimethylindium [TMIn; $In(CH_3)_3$] and arsine (AsH_3) were used as gas-phase precursors for the supply of In and As growth species, respectively. All samples were first subjected to a 5 min annealing treatment at 850 °C under AsH_3 flow in order to improve the growth yield, similar to what was reported to favor NW growth along the vertical ⟨111⟩ direction over other equivalent ⟨111⟩ directions.[37,38] Next, the reactor was cooled to a growth temperature of 700 °C. All temperature values reported here refer to the thermocouple-controlled reactor set-point value. The AsH_3 flowrate and the chamber pressure were maintained at 365 μmol/min and 100 mbar, respectively, for all growths. Table 1 summarizes the key growth conditions for the various samples investigated in this study. Sample A growth was performed using a TMIn flowrate of 1 μmol/min over a 25 min growth duration. A two-step, flowrate-modulated growth sequence was introduced for Samples B and C to increase the NW yield. In order to increase the number of nucleation sites, during the first growth step (i.e., the nucleation step), the substrate surface was flooded with a high TMIn flowrate of 16 μmol/min for a period of 60 and 30 s for Samples B and C, respectively. During the second step (i.e., the growth step), the TMIn flowrate was reduced to 1 μmol/min for a period of 25 min.

Delamination Procedure, Substrate Restoration, and Reuse. For delamination of InAs NW arrays, the Colorless First Contact (CFC) polymer was applied to as-grown samples by drop-casting small volumes of the polymer solution. After drying under ambient conditions for ∼24 h, the NW array-embedded membranes were mechanically delaminated from their native growth substrates through shear-induced fracture. After delamination, all substrates were treated with the First Contact Thinner solution to ensure the dissolution of residual CFC polymers on the surface. Then, two different methods were investigated for substrate reuse. In the first method, substrate restoration to the pre-growth state was investigated. In this case, substrates were treated with either a citric acid solution ($C_6H_8O_7/H_2O_2$, 20:1) solution or a piranha solution (C_2SO_4/H_2O_2, 3:1) for 5 min in order to selectively etch the InAs NW base segments that remained attached to the substrate in each pore (i.e., below the NW fracture plane). After rinsing with standard solvents and a pre-growth BOE treatment, the restored substrates (i.e., Sample D) were loaded in the MOCVD reactor for reuse and growth of second generation InAs NW arrays using a two-step growth sequence (i.e., same growth sequence as Sample C). In the second substrate reuse method, post-delamination wafers (i.e., Sample E) were simply rinsed with standard solvents and then directly reloaded in the MOCVD reactor for growth of second generation InAs NW arrays without intermediate substrate restoration steps to etch the remnant NW base segments formed during the initial growth cycle. Sample E NWs were grown under otherwise identical growth conditions as Sample A NWs.

Transfer of NW Arrays and Device Fabrication. To transfer the delaminated NW arrays for subsequent device fabrication, the backside surfaces of the exfoliated polymer membranes were subjected to an RIE process to expose ∼150 nm along the base segments of the embedded NWs. Next, a trilayer stack of Ti/Al/Ti (25 nm/300 nm/25 nm) was sputtered on the backside of the membranes to serve as a backside contact and supportive medium to preserve the as-grown vertical orientation and original position of the NWs in the delaminated arrays. The membranes were then bonded to corona-treated Si carrier wafers using uncured PDMS as the bonding matrix, followed by a 3 h baking step at 60 °C. Next, the bonded membranes were submerged in the First Contact Thinner solution for 12 h to dissolve the delamination matrix. For device fabrication, a S1813 photoresist layer was spin-coated to encapsulate the transferred NW arrays and then thinned using an RIE treatment to expose the tip segments of the NWs. The samples were then submerged in a citric acid solution ($C_6H_8O_7/H_2O_2$, 20:1) for 30 s to selectively etch the exposed NW tip segments in order to generate a more homogeneous height profile for all NWs in the large-area arrays. The photoresist layer was again subjected to a short RIE step to expose the NW tip segments prior to sputter deposition of a 300 nm indium−tin-oxide (ITO) layer as a transparent conductive topside contact. Lastly, samples were annealed at 250 °C for 1 h.

Materials Characterization and Device Measurements. A Hitachi S-4000 scanning electron microscope (SEM) was used to image the morphology of as-grown NWs. A Bruker DI-3000 atomic

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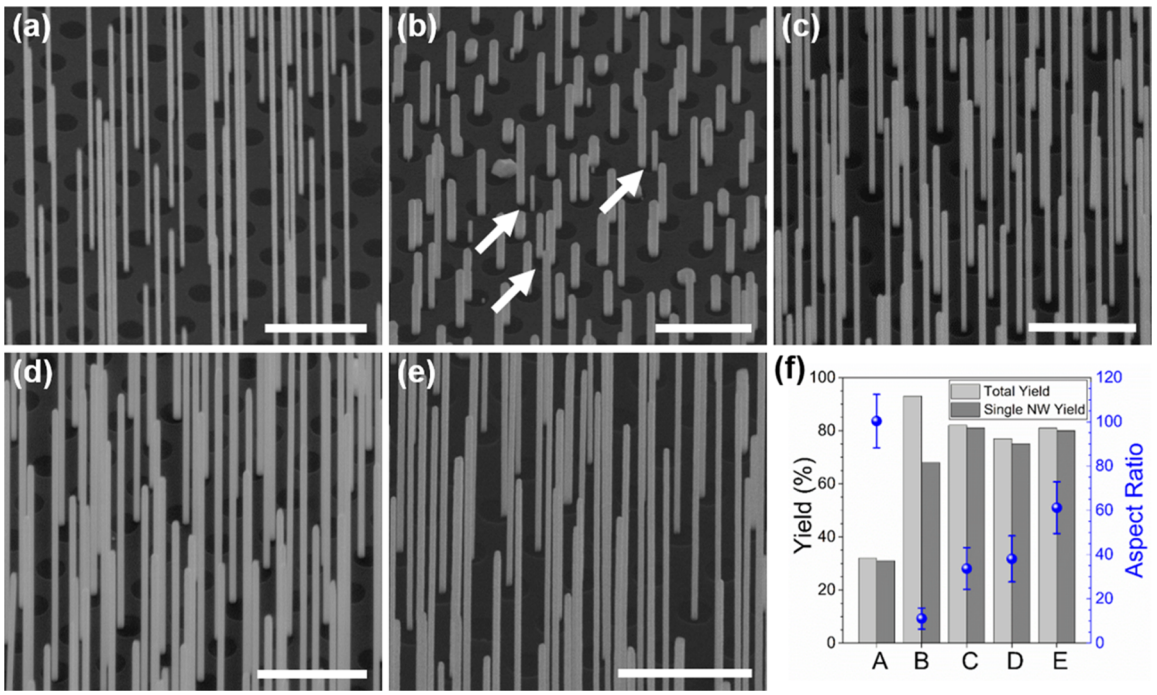

Figure 1. (a–e) 45° tilted-view SEM images of LSA-grown InAs NWs corresponding to Samples A–E presented in this work. (a) Sample A, grown in a one-step process without a separate nucleation step. (b) Sample B, grown using the two-step, flowrate-modulated sequence with a 60 s nucleation step. Arrows point to three examples of nanopores in which more than one NW are formed. (c) Sample C, grown using the two-step sequence with a 30 s nucleation step. (d) Sample D, grown on a reused Si substrate following a citric acid restoration procedure and BOE treatment. (e) Sample E, grown directly on a reused substrate after delamination of the parent NW array without an intermediate restoration procedure or BOE treatment (only solvent cleaning). All scale bars represent 2 μm. (f) Measured values for total yield (light gray bars) and single NW occupation yield (dark gray bars), as well as the mean NW aspect ratio (blue data points; error bars represent ± one standard deviation from the mean) for Samples A–E.

force microscope (AFM) was used in the intermittent contact mode for imaging and NW base segment height profilometry. A FEI Strata 400 STEM focused ion beam (FIB) was used for the preparation of lamellae for analytical transmission electron microscopy (TEM) experiments. The crystal structure of re-grown NWs was characterized using a FEI F20 high-resolution transmission electron microscope (HR-TEM). Energy-dispersive X-ray spectrometry (EDXS), acquisition of elemental maps and linescans, and collection of selected-area electron diffraction (SAED) patterns were performed using the same instrument. Electrical measurements were performed by probing the top and backside device contacts using a Keithley 2400 SourceMeter Unit (SMU). All electrical measurements were conducted at room temperature under dark and illuminated conditions. Broadband illumination (i.e., 350 to 2500 nm) was provided by a tungsten halogen source with power density of 57 mW/cm^2.

RESULTS AND DISCUSSION

Epitaxial growth of III–V NW arrays under the SAE regime is commonly carried out using oxide masking templates that are defined by EBL.[39−41] This technique provides excellent control over the position, growth rate, and, consequently, dimensions of the SAE NWs. However, EBL is also associated with high costs and prohibitively long processing times for wafer-scale template fabrication. To overcome these limitations, standard *i*-line photolithography is employed here to prepare oxide masking templates on 150 mm-diameter Si wafers.

The first objective of this work is to tune the MOCVD growth parameters in order to realize a high total yield of NWs with only single NW occupation per nanopore. Three different sets of growth conditions are investigated toward optimization of yield and aspect ratio of InAs NWs. The samples grown under these three sets of conditions are referred to as Samples A, B, and C, as summarized in Table 1, and are described in the Experimental Details.

Figure 1 shows representative tilted-view SEM images obtained from as-grown Samples A–E. For each sample set, dimensional analysis is performed by measuring more than 100 NWs from different sample locations, while yield analysis is conducted based on the occupancy of more than 400 nanopores across four regions on each sample. Based on these measurements, the calculated mean NW aspect ratio (blue data points) and NW yield (gray bars) values for each of the three samples are presented in Figure 1f. The yield measurements are sub-categorized as the total yield, which is defined as the percentage of nanopores occupied by at least one vertical InAs NW (light gray bar), and as single NW occupation yield, which is defined as the percentage of nanopores occupied by exactly one vertical InAs NW (dark gray bar). For Sample A NWs, which are grown without a high flowrate nucleation step, a mean length of 11320 ± 1250 nm and mean diameter of 113 ± 9 nm is measured (errors represent one standard deviation from the mean). We note from Figure 1 that most NWs are grown near the peripheral pore regions. While the exact basis of this effect is currently unclear, we speculate that it may be related to the higher capture probability of stable nuclei, which preferentially form at the edge of the pores due to a greater supply of diffusive adatoms from the neighboring oxide field. Yield analysis reveals that 32% of all patterned nanopores are occupied by NWs, while only a negligible fraction of nanopores are occupied by two or more NWs, resulting in a measured single NW occupation yield of 31%.

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To increase the number of occupied pores, a two-step sequence is introduced during the growth of Sample B NWs. First, the substrate is flooded with a high TMIn flowrate of 16 μmol/min for 60 s in order to promote NW nucleation inside the exposed pores. Next, the TMIn flow is reduced to 1 μmol/min for a period of 25 min in order to promote adatom surface migration, leading to axial extension of the InAs lattice at each nucleation site. Sample B NWs, shown in Figure 1b, exhibit a mean length of 2216 ± 548 nm and a mean diameter of 176 ± 21 nm. Use of the two-step growth sequence results in a total yield of 93%. However, a higher fraction of pores are occupied by more than one NW. The white arrows in Figure 1b point to the three examples of nanopores in which two NWs are formed. This effect results in a single NW occupation yield of only 68% in Sample B.

The undesired multiple NW occupancy effect is resolved in Sample C, simply by reducing the duration of the initial high-flowrate nucleation step from 60 to 30 s. A reduction in the number of nucleation sites and distribution of growth species amongst correspondingly fewer NWs lead to the formation of higher aspect ratio structures in comparison to Sample B. This is quantified by a mean length of 4377 ± 878 nm and a mean diameter of 132 ± 17 nm for Sample C NWs. Figure 1c shows an image of Sample C NWs, which exhibit a total yield of 82% and a single NW occupation yield of 81%, indicating that only a negligible fraction of the nanopores contain multiple NWs. The growth conditions of Sample C provide a suitable basis, with respect to the NW yield and aspect ratio, for additional Si wafer reuse and substrate-free device fabrication experiments. For all three samples, no parasitic crystal growth is observed on the oxide mask, which is one indication that growth may proceed under a selective-area regime.

During SAE growth, island nucleation occurs preferentially inside the patterned nanopores due to the large sticking coefficient differential between the masking layer (i.e., SiO_2) and the exposed substrate (i.e., Si). In the current work, the large lattice mismatch between InAs and Si (i.e., ∼11.6%) and the corresponding lattice strain lead to a high interfacial surface energy, which limits lateral expansion of nuclei inside the template pores. Thus, direct InAs island nucleation from the vapor phase becomes energetically favorable without wetting layer formation according the Volmer−Weber growth mode, which can proceed in the absence of metallic seeding agents.[33,34] Since the InAs islands are epitaxially registered to an atomically flat Si substrate with (111) surface orientation, crystal growth proceeds preferentially along the vertical ⟨111⟩ direction of the InAs lattice.[35] Thus, vertical and free-standing NWs can be formed under a pseudo-Volmer−Weber regime.[33,34]

Due to the large pore size of 500 nm used here, strain-limited self-assembly results in NWs that do not fully occupy the exposed substrate area inside each pore.[41] This allows only coarse control over the exact position of NWs inside the template pores of relatively larger diameter and, under certain conditions, can lead to the formation of multiple NWs in a single pore. This is in contrast to the case of a more closely lattice-matched system, such as GaAsP on Si, for which the SAE-grown nanocrystals extend across the full area of the template nanopores under otherwise comparable SAE conditions (refer to Figure S1 of the Supporting Information document). For growth of InAs on Si, the fact that NW diameter is not strictly dictated by the template nanopore diameter also results in the formation of NWs with a range of heights. The large standard deviation values associated with the aspect ratio data shown in Figure 1f illustrate this point.

These features distinguish the current approach from the conventional NW SAE growth mode, where NW diameters are commonly equal to or exceed the nanopore dimensions. We emphasize this distinction by referring to our growth mode as "localized self-assembly" (LSA). A similar description was recently adopted by Dubrovskii et al. for Ga-droplet assisted epitaxy of GaAs NWs on Si substrates through microscale pores of oxide masking layers.[42] We also note that Gao et al. have reported a dual growth regime wherein InP NW epitaxy can simultaneously proceed via both SAE and VLS regimes under the same growth conditions depending on NW diameter.[43] To investigate the possibility of In-droplet-mediated NW synthesis in the current work, we have carried out an additional growth under Sample C conditions, but in the absence of AsH_3 flow during the cooling stage. Thus, NW growth was terminated by simultaneously stopping both group-III and group-V precursor flows. Here, no isolated In phase (i.e., seeding droplet) was observed at the NW tip, as determined by TEM and EDXS analysis (Figure S2). This is in contrast to the observation of In droplets at the tip of thinner InP NWs grown under otherwise SAE conditions reported by Gao and colleagues.[43] Given that our growth process precludes a group-III species pre-deposition step and that In droplets were not observed at the NW tip under AsH_3-free cooling conditions, we believe that the current LSA growth mode is more comparable to the seed-free SAE mechanism than localized VLS growth.

Before investigating the reuse of Si substrates for multiple III−V crystal growth runs, Sample C NW arrays are delaminated from the parent wafer. Figure 2a shows a representative image of the Sample C Si substrate and an oxide masking template immediately after the delamination step. After NW array peel-off, the oxide masking layer remains fully intact. However, short NW base segments are observed inside the pores, which reveal the fracture plane. Three examples of clearly identifiable remnant NW base segments are indicated by white arrows in Figure 2a.

The fracture surface profile and average height of the remnant base segments are measured using AFM. Figure 2b shows an AFM image of a representative nanopore in which a NW base segment is visible after the delamination step. The height profile of this base structure is shown in Figure 2c, which corresponds to the line segment spanning points A to B marked in Figure 2b. A graded fracture profile is observed and a base segment height of ∼16 nm is measured at its apex (i.e., maximum height relative to substrate surface baseline). Based on similar analysis of over 30 pores, a mean apex height of 20.6 ± 5.1 nm is measured for the NW base segments after peel-off.

For Si substrate reuse investigations, two different strategies are employed. In the first approach, after NW array delamination, the substrates are restored to their pre-growth condition using a simple citric acid treatment to preferentially etch the InAs segments inside the template nanopores. For comparison, Figure S3a of the Supporting Information shows the surface of the parent Si wafer immediately after NW array delamination. As shown in Figure S3b, the citric acid treatment fully restores the Si substrate to its initial pre-growth state without damaging or unintentionally inducing porosity in the oxide masking template. An alternative substrate restoration procedure utilizing a piranha solution treatment is also described in the Supporting Information (Figure S3c).

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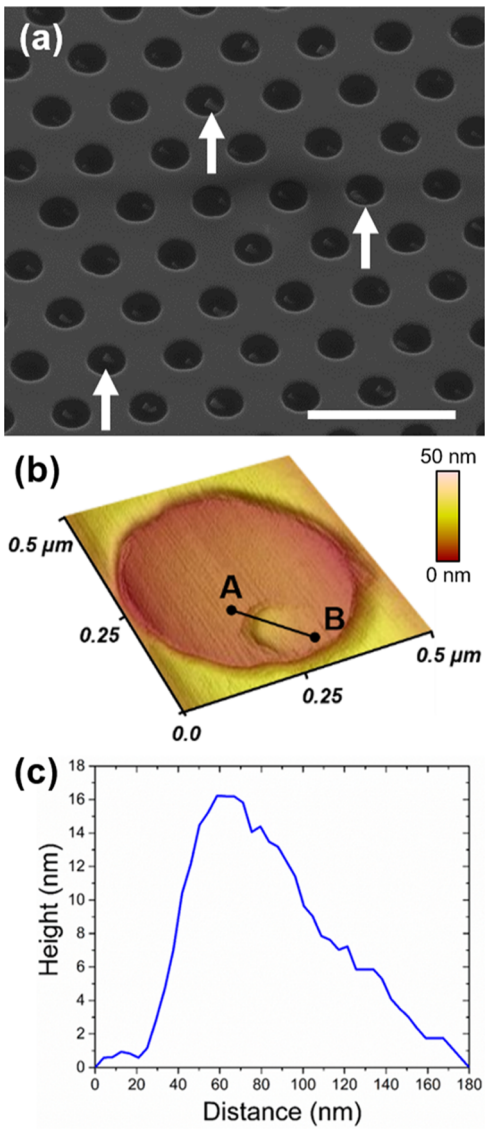

Figure 2. (a) 45° tilted-view SEM images of the parent, SiO_2-templated growth substrate immediately after NW array delamination. The white arrows point to three examples of pores in which remnant NW base segments can be seen. Scale bar represents 2 μm. (b) AFM image collected in the tapping mode along a masking template nanopore after NW array peel-off, revealing a NW base segment inside the pore that was left behind below the NW's fracture plane. The hexagonal cross-section profile of the NW can be seen toward the left-hand side of the base segment. The color scale legend is normalized to the Si substrate surface baseline. (c) Corresponding AFM height profile measured across points A to B in (b).

In order to verify the feasibility of the restoration process as an intermediate step toward reuse of Si substrates with masking templates, the flowrate-modulated LSA sequence (i.e., under Sample C growth conditions) is performed on parent Si wafers after InAs NW array delamination and citric acid treatment. Figure 1d shows a representative SEM image of as-grown NWs on a restored and reused Si substrate, henceforth, referred to as Sample D. A mean length of 5065 ± 1244 nm and a mean diameter of 133 ± 16 nm are measured in the case of Sample D NWs. Total yield and single NW occupation yield values are measured to be 77 and 75%, respectively, on the reused substrates after the restoration treatment. Thus, similar NW dimensions and yield values are realized in the preliminary growth run on parent substrates (Sample C) and in the secondary growth run on reused substrates (Sample D). Compared to the conventional substrate reuse methods for thin films that are intended to mitigate the high cost of III−V wafers, such as the epitaxial liftoff (ELO) technique,[44] the NW array delamination and wet chemical etching approach reported here offers the following advantages: (a) liberation of active device structures without the need for either growth or subsequent chemical etching of sacrificial release layers; (b) elimination of the additional processing steps, dedicated instrumentation, and high costs associated with chemo-mechanical polishing (CMP) procedures (we note that prior demonstration of an ELO procedure without use of CMP has also been presented by Cheng et al.[45]); and (c) replacement of starting III−V wafers with reusable Si substrates.

However, the substrate reuse approach described for Sample D has a critical drawback. Due to the formation of a native oxide layer inside the nanopores of the LSA making template after substrate restoration, a pre-growth BOE treatment is needed prior to loading the reused substrates in the growth reactor. This imposes a limit on the number of times each oxide-templated substrate can be reused due to continual dissolution of the masking layer, which has an etch rate of ∼80 nm/min in the BOE solution employed here.[46] We were able to reuse the patterned Si substrate three times when employing the intermediate citric acid treatment and BOE procedure before the SiO_2 template was dissolved as a result of the pre-growth oxide etching step. One approach for extending the longevity of the masking layer is to use a silicon nitride template,[47] which allows a high etch rate selectivity of the native oxide over the LSA mask.[48] However, an even simpler alternative is adopted here. This alternative approach involves elimination of the substrate restoration procedure and pre-growth BOE step, such that parent Si wafers with masking templates and remnant NW base segments are reused after NW array delamination. Here, the remnant NW base segment inside each pore serves as a preferred growth site for direct extension of the InAs lattice along the substrate normal direction (i.e., axial NW growth direction). This approach potentially allows a greater number of substrate reuse cycles to be realized compared to a procedure that requires pre-growth wet etching of the substrate native oxide.

To investigate the potential for direct re-growth, Sample E substrates are loaded in the MOCVD reactor following the NW array delamination procedure and a solvent rinsing step. Since the template pores are occupied by remnant NW base segments that serve as preferential growth initiation sites, the nucleation step, which is necessary in the case of Samples B−D, is eliminated from the Sample E growth sequence. Figure 1e shows a representative tilted-view SEM image of as-grown Sample E NWs after growth on reused substrates with no restoration procedure. Vertical extension of the remnant base segments is realized, leading to the growth of NWs with a mean length of 6285 ± 1474 nm and a mean diameter of 99 ± 11 nm. Total NW yield and single NW occupation yield values of 81 and 80% are measured for Sample E, respectively, which match well with the yield values of the initial LSA growth run on parent substrates (i.e., Sample C). A comparison of the NW aspect ratio and yield data for Sample D (substrate reuse after citric acid restoration) and Sample E (substrate reuse without restoration) is shown in Figure 1f. In both substrate reuse approaches, the original pattern fidelity and NW verticality is preserved.

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Next, the crystal structure of Sample E NWs that are extended from the remnant base segments on reused Si wafers is investigated using TEM. Emphasis is placed on inspecting the crystal structure along the NW base region about the anticipated delamination fracture plane. As noted above from AFM analysis, this region of interest is located ~20.6 ± 5.1 nm from the InAs/Si interface and serves as the location of InAs lattice extension during the regrowth sequence. Figure 3a

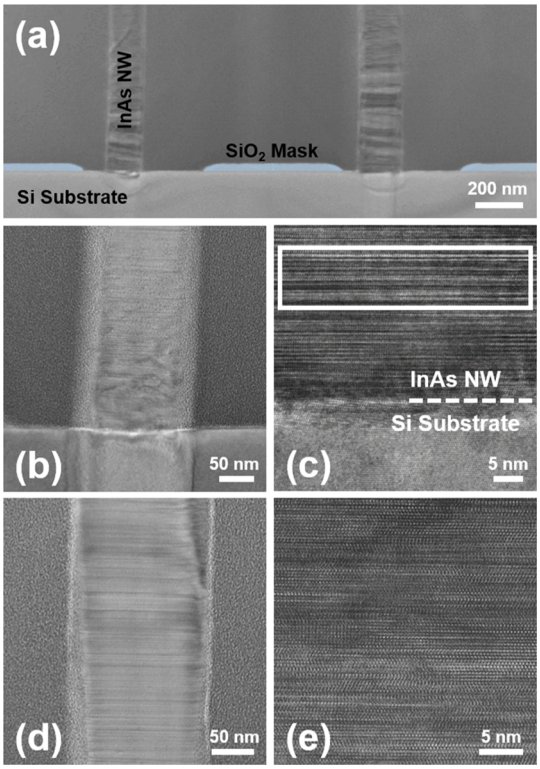

Figure 3. Bright-field TEM images of InAs NWs grown from remnant base segments on parent Si substrates, which were reused without restoration procedures. (a) Low-magnification bright-field image of two adjacent NWs. The oxide masking layer between NWs is false-colored in blue. (b) Bright-field TEM and (c) HR-TEM images collected at the InAs NW/Si substrate interface. The white box in (c) indicates the anticipated region of InAs lattice extension during the regrowth sequence. (d) Bright-field TEM and (e) HR-TEM images collected along a region approximately 500 nm above the NW/substrate interface.

shows a low-magnification, bright-field TEM image of two neighboring vertical InAs NWs on the reused substrate, where the SiO_2 masking template is false-colored in blue. Figure 3b,c shows higher-magnification bright-field and HR-TEM images, respectively, collected along the reused substrate/InAs interface of the NW seen on the left-hand side of panel (a). In Figure 3c, the substrate interface is marked by a white dashed line, while the region corresponding to the anticipated delamination fracture plane (i.e., regrowth initiation region) is marked by a white border. Figure 3d,e shows bright-field and HR-TEM images, respectively, collected along a segment of the same NW that is located approximately 500 nm from the Si/InAs interface. Along the entire length of the NW, including the regions corresponding to the remnant base segment of the parent NW and the regions above the regrowth initiation plane, a mixed crystal structure consisting of a combination of zinc-blende and wurtzite phases is observed. Fast Fourier transform (FFT) patterns generated from the lattice-resolved HR-TEM images are shown in Figure S4 of the Supporting Information. The coincident symmetries of the FFT patterns and comparable streaking along the growth direction confirm the mixed phase lattice arrangement that is common to both remnant base and regrowth segments. This polytypic crystal structure is characteristic of InAs NWs grown under both SAE[49,50] and self-assembly[33,51] growth modes on various substrates. Considering that the polytype crystal structure is commonly observed under the growth condition used in this work,[37,51,52] no additional lattice discontinuities, variations in the crystal structure, or extended defect phases are introduced as a result of the regrowth procedure. A higher magnification image and corresponding SAED pattern obtained at the interface between the regrown NW and reused substrate, along with elemental linescans and maps obtained using EDXS, are provided in Figure S4 of the Supporting Information.

The NW array delamination and substrate reuse procedure is intended to enable the fabrication of substrate-free, III−V membranes for optoelectronic device applications, such as broadband photodetectors. Figure 4 shows the process flow utilized in the current work for NW array transfer and device fabrication, as described in the Experimental Details. The black and yellow arrows in Steps 2 to 5 represent the NW array when positioned in the upright (i.e., as-grown) and inverted orientations, respectively. In contrast to alternative fabrication approaches for NW-embedded flexible membrane devices that require device processing on the growth substrate,[53] the current approach allows the direct transfer of NW arrays to any foreign platform (e.g., carrier wafer, contact layer, etc.) while preserving the orientation and position of as-grown NWs during subsequent processing steps.

Figure 5a shows a photograph of a delaminated membrane containing a NW array that is embedded in the CFC polymer layer and held by a pair of tweezers. A tilted-view SEM image of the membrane's backside surface is shown in Figure 5b. The bases of the delaminated NWs are visible through the encapsulating polymer layer after an RIE step to expose NWs for contact deposition. In Figure 5c, the same backside surface is shown after deposition of a Ti/Al/Ti trilayer stack, which simultaneously serves as a reflective rear contact layer and a mechanical anchor. This anchoring medium preserves the original NW array spacing and orientation upon transfer to foreign carriers, and it ensures reliable fidelity of the original array geometry during subsequent processing steps. In Figure 5c, the contact points of the anchoring contact layer to individual NWs appear as hemispherical protrusion beyond the surface of the enclosing polymer matrix.

Since important optical properties of NW arrays, such as spectral range and wavelength-selective resonant absorption, can be engineered as a function of NW orientation, diameter, and pitch values,[54−56] maintaining NW verticality and array geometry during fabrication is critical. An image of an upright NW array, anchored by the backside contact stack, after dissolution of the encapsulating CFC membrane, is shown in Figure 5d; this corresponds to Step 6 of the process flow in Figure 4. As seen in the micrograph, successful transfer of the NW array is realized with a near-unity yield. After dissolution of the delamination polymer, the original orientation and relative position of each NW in the array is preserved. Alignment angle measurements collected after the CFC dissolution step show that approximately 90% of all transferred NWs are positioned within ±1° of the vertical orientation,

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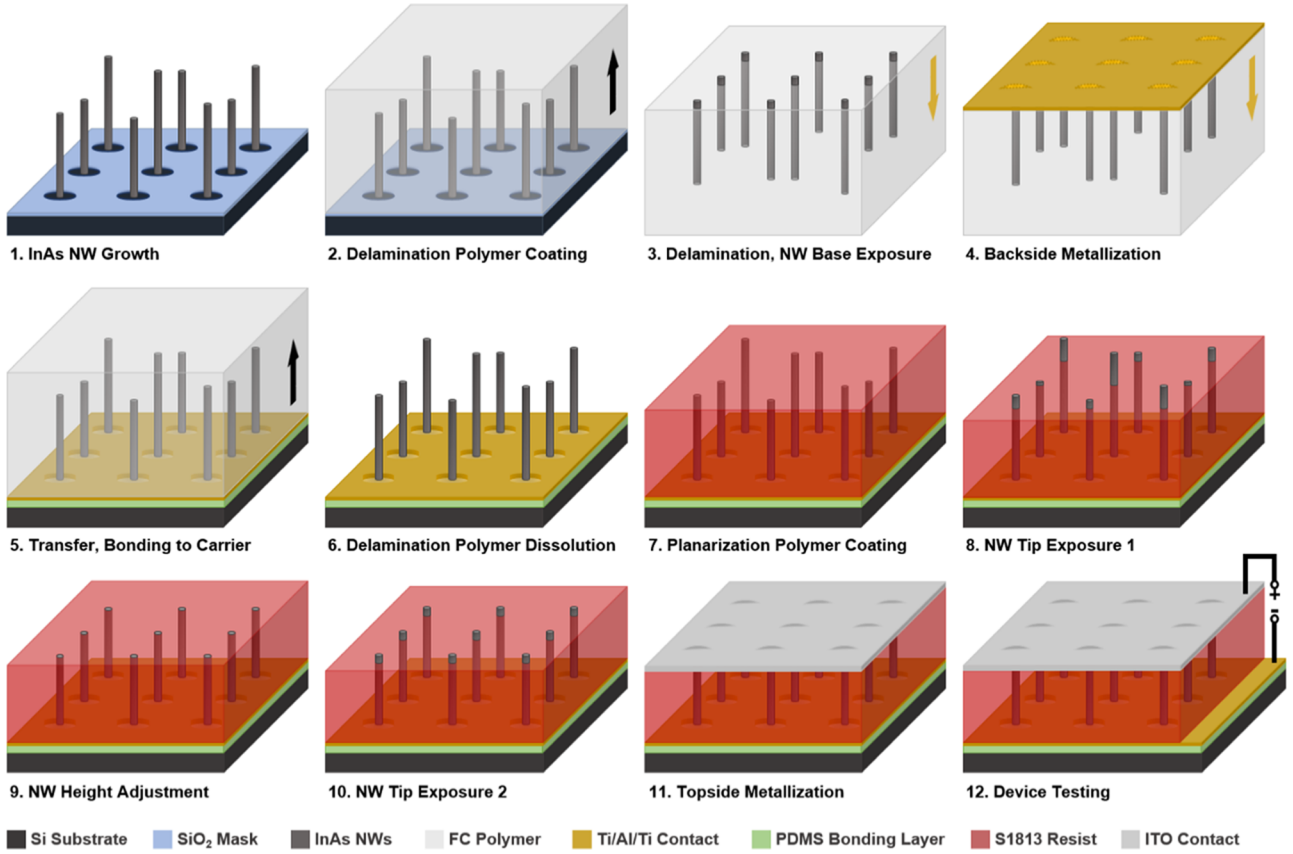

Figure 4. Schematic diagram of NW array transfer and the device fabrication process: (1) LSA growth of NW arrays via MOCVD; (2) CFC polymer deposition (black arrow shows the as-grown, upright array orientation); (3) delamination of the NW-embedded polymer, followed by membrane inversion and RIE treatment to expose NW base segments (yellow arrow shows the inverted array orientation); (4) deposition of anchoring backside contact; (5) PDMS bonding of the NW-embedded membrane to carrier wafer for further device fabrication; (6) dissolution of the CFC polymer membrane, which results in NWs being transferred from their native growth substrate to a new carrier wafer with preserved position and vertical orientation; (7) coating and planarization of the S1813 resist layer; (8) RIE treatment to expose the NW tip segments to a common height of ~1.75 μm; (9) wet-etching of exposed NW tips using citric acid solution for height adjustment; (10) RIE treatment to expose NW tip segments for top contacting; (11) ITO top contact deposition followed by annealing treatment; and (12) the final device structure and probing configuration.

while the remaining 10% of NWs are aligned within ±2° of the vertical angle. Distributions of the angles of orientation of as-grown and transferred NWs are provided in the Supporting Information (Figure S5).

Several alternative NW array peel-off and substrate reuse approaches have been presented to date. Spurgeon et al. first demonstrated the delamination of Si NW arrays and reuse of a parent Si(111) substrate along with the porous oxide masking layer in 2008.[46] After mechanical separation, the authors selectively etched the remnant NW base segments inside the template nanopores prior to electrodeposition of Au inside the pores, which served as catalysts for Si NW regrowth via the VLS mechanism. Similarly, Cavalli et al. showed reuse of NIL-patterned InP(111) substrates through delamination of InP NW arrays using PDMS membranes. For substrate cleaning, diluted tetra-butyl-ammonium fluoride solution was used to remove the residual polymer followed by a dilute HCL treatment to remove the base part of the InP NWs.[57] More recently, Zhang et al. published an elegant approach for NW array peel-off. This involved spin-coating bilayers of S1818 and SU-8 polymers separated by Pd/Pt alloy films and double-exposure to selectively remove the S1818 layer at the base of the NWs, while leaving the remainder of the NWs embedded in the SU-8 layer.[58] The authors noted that these approaches enabled array delamination due to the built-in stress within the SU-8 layer and reduced potential inhomogeneity at the NW facture plane. Jafari Jam et al. recently presented another practical method, which involved VLS growth of GaAs/AlAs/GaAs NWs through a patterned SiN_x porous template.[59] After growth, the NWs were embedded in a PDMS layer and mechanically fractured across the AlAs segment, which was subsequently selectively etched. Thus, the AlAs segment served as a sacrificial layer and generated a homogeneous surface for the underlying GaAs segment inside the pores of the masking template for selective re-electrodeposition of Au catalysts, enabling regrowth of NWs on the parent GaAs substrate. The NW array transfer and substrate reuse methods presented in the current work combines some of the strategic advantages of the recently demonstrated approaches, including (a) use of high-throughput and reproducible *i*-line photolithography to pattern oxide masking templates on 150 mm wafers; (b) absence of foreign seeding agents in exchange for a simplified LSA growth mechanism; (c) use of the CFC polymer as a delamination medium, which enables process simplicity by eliminating the need for polymer bilayer deposition and double-exposure; and (d) ease of dissolving the CFC polymer membrane while preserving the vertical NW orientation, which enables potential use in biomedical applications.[60] A

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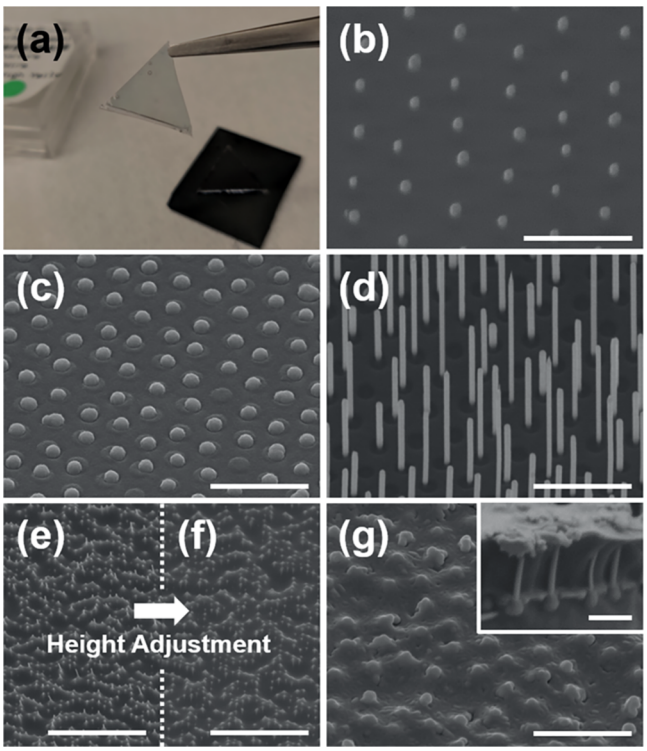

Figure 5. (a) Photograph of the InAs NW array membrane held with tweezers. 45° tilted-view SEM images obtained at various stages of the device fabrication process: (b) backside of the delaminated membrane after the RIE step to expose the NW base segments; (c) backside of the delaminated membrane after Ti/Al/Ti trilayer stack deposition (hemispherical features represent the location of NW base segments); (d) transferred, free-standing NW array on carrier wafer after backside PDMS bonding and CFC dissolution, showing that the original vertical orientation and positions of NWs are preserved; (e) S1813 polymer layer coating and planarization before height adjustment and (f) after citric acid treatment for height adjustment; and (g) topside of the NW membrane device after ITO top contact deposition. Inset shows a cross-sectional view of the fabricated device with 4 visible vertical NWs anchored in place by the backside contact (anchoring bulbs visible under each NW). Scale bars in (b–g) represent 3 μm. Scale bar in the inset of (g) represents 1 μm.

distinguishing aspect of the current work is that remnant NW base segments are exploited as preferential sites for NW re-growth on parent substrates, which avoids growth and selective etching of sacrificial NW segments as well as additional substrate restoration steps.

In comparison to the above approaches, however, the LSA growth mode utilized here has a notable disadvantage: The inhomogeneity in the length distribution of as-grown NWs presents a challenge for planarization and subsequent top contact deposition. During conventional SAE NW growth, the high degree of lateral confinement provided by the narrow-diameter template pores enables growth of NWs with uniform diameters and, therefore, more homogeneous length distributions. In contrast, during LSA of InAs on Si, the diameter of NWs is not strictly defined by the size of the larger template pores. Rather, the NW diameter and axial-to-radial growth rate ratio depend upon other parameters. These parametes include the lattice-mismatch between InAs and Si, the number of nearest neighbor NWs, the spacing of nanopores, and the epitaxial growth conditions. The wider distribution of NW diameters resulting from LSA synthesis introduces NW length non-uniformities in the case of large-area arrays.

To normalize the NW height distribution and mitigate top contact deposition challenges, two planarization steps are introduced. After re-encapsulating the transferred NW array in a S1813 photoresist planarization medium (Figure 4, Step 7), an RIE procedure is used to expose ~90% of all NWs in the array, as shown in Figure 5e (corresponding to Figure 4, Step 8). At this stage, the embedded NWs are buried in the S1813 polymer to a common height of ~1.75 μm. Next, a citric acid treatment is used to etch the excess length of the NWs exposed beyond the surface of the encapsulation medium (Figure 4, Step 9). This process effectively corrects NW length disparities over large areas and generates a more homogeneous array height. Lastly, a short RIE treatment is used to uniformly expose the top 150 nm of the NWs for ITO deposition, as shown in Figure 5f (corresponding to Figure 4, Step 10). Figure 5g shows the planarized top surface of the NW array after top contact deposition (corresponding to Figure 4, Step 11). The locations of individual NWs are visible through the ITO film. The inset of Figure 5g shows a cross-sectional view of the fabricated device, where four vertical NWs are seen that are partially embedded in the planarization medium and anchored in place by the backside trilayer contact. Each anchoring point can be seen as a bulb-like protrusion in the underlying PDMS bonding layer. Samples are subjected to a thermal annealing treatment prior to device testing to form Ohmic contacts, as well as to improve the transparency of the ITO film and reduce its sheet resistance.

The photoresponse of the substrate-free, vertical InAs NW array-based metal–semiconductor–metal (MSM) photoconductors is measured at room-temperature by probing the top and backside contacts, as depicted in Step 12 in Figure 4.[35,36,61] A tungsten halogen lamp is used as the broadband source, which provides illumination over the 350 to 2000 nm wavelength range, with an incident power density of 57 mW/cm^2. Figure 6 shows the semi-log current–voltage (I–V) characteristics of a representative NW array device under dark (black curve) and illuminated (red curve) conditions over the −1 to +1 V bias range. A reverse dark current of ~3 μA is measured at −1 V. Upon illumination, the production of photogenerated carriers results in a clear current enhancement, characterized by a photocurrent of roughly 0.3 mA at −1 V.

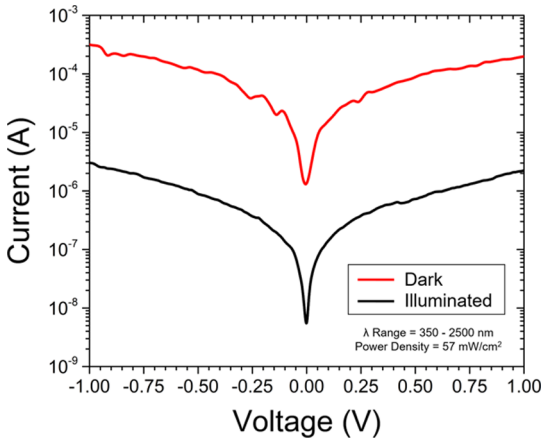

Figure 6. Output characteristics of the substrate-free InAs NW array-based MSM photodetector under dark (black curve) and illuminated (red curve) conditions.

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Thus, a room-temperature on/off current ratio (I_{ON}/I_{OFF}) of approximately 10^2 is measured. The detected photoresponse validates the feasibility of the fabrication process described above. It also demonstrates that the delaminated NWs that are regrown on reused Si substrates are optically active and remain structurally stable during the transfer process. Using the substrate reuse and processing protocols established here, the performance and functionality of NW-based photodetectors can be improved in future works through implementation of several proven strategies, such as introduction of p−i−n junctions and heterojunctions during NW growth,[62] as well as modulation of NW diameter and array geometry for enhanced selective resonant absorption.[10,63]

While the LSA growth technique offers a series of practical advantages, it also has some notable limitations. The main drawbacks of the LSA method include (a) inherent inhomogeneity in diameter and length of as-grown NWs and sample-to-sample variability in NW dimensions; (b) limited control over the exact position of NWs inside wider nanopores, which leads to array aperiodicity; (c) strain-limited self-assembly requires a high degree of lattice mismatch between the substrate and epi-layer, which limits the number of materials combinations that can be synthesized under this growth mode; and (d) challenges associated with the growth of axial and coaxial NW heterostructures with equivalent geometries. However, the LSA growth mode enables heterogeneous epitaxy of vertical and high aspect ratio InAs NWs and micropillars with a wide range of tunable dimensions including diameters ranging from 100 nm to 1 μm and lengths tunable from 0.1 μm to greater than 10 μm, using template pores varying from 0.5 to 4 μm in diameter and array pitch values in the 1 to 10 μm range (not shown here; to be reported in a separate publication).

CONCLUSIONS

The LSA growth mode by MOCVD provides a low-cost path toward III−V NW array growth on large-area Si substrates. Scalable photolithography is employed for patterning of selective-area masking templates. The growth sequence uses flowrate modulation, which provides global NW yields exceeding 80% and allows control over the arrangement of only a single NW per template nanopore. As-grown InAs NW arrays are embedded in a polymer encapsulation medium, mechanically delaminated from the growth surface, and anchored by a metallic trilayer stack. The latter serves as a backside device contact layer and ensures that the original position and vertical orientation of the free-standing NWs are preserved upon transfer to foreign carrier wafers for device processing. Parent Si wafers and their masking templates are reused for subsequent LSA growth runs using two separated regrowth approaches. In the first approach, a citric acid (or a piranha solution) treatment is used to restore the parent substrates and nanoporous oxide masking layers to their pre-growth state. In an alternative approach, the original substrates, which contain short NW base segments that remain inside the template pores after delamination, are directly reused without introduction of intermediate substrate restoration steps. In this case, the remnant NW base segments act as preferential sites for the extension of the InAs lattice in the vertical direction. In both approaches, the original LSA masking template pattern fidelity is preserved upon substrate reuse and no parasitic nucleation is observed on the mask, consistent with crystal growth under a selective-area self-assembly regime. The transferred InAs NW arrays are processed for proof-of-concept demonstration of substrate-free MSM photodetectors with I_{ON}/I_{OFF} ratios of 10^2 under broadband illumination. Future extensions of the current work include detailed characterization of the optical properties of delaminated InAs NW arrays of various dimensions in dissimilar encapsulating polymer media, analysis of the influence of anchoring backside contact layers on their optical properties, and detailed performance analysis of substrate-free membrane photodetectors fabricated using type-II heterojunction NWs. This work establishes the LSA growth mode as a feasible approach for the heteroepitaxial synthesis of large-area III−V NW arrays on oxide-templated Si wafers that can be reused without dedicated restoration between regrowth cycles for applications in substrate-free and flexible optoelectronic membrane devices.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsanm.1c03557.

Comparison of InAs LSA and GaAsP SAE on Si; analysis of the NW tip structure and composition; description of citric acid and piranha surface treatment for substrate and masking template restoration; analytical TEM results of InAs NW growth on the reused Si substrate; and statistical analysis of the alignment angle of delaminated NWs (PDF)

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Author Contributions

A.A. and P.K.M. conceived the research project and designed the experiments. A.A. and M.A.B. conducted sample preparation and epitaxial growth experiments. S.J.P. and E.-M.S. supported and assisted with growth experiments. A.A. carried out SEM imaging, sample processing, device fabrication, device testing, and related data analysis. A.F. performed AFM measurements. A.A. conducted analysis of AFM and analytical-TEM results. S.M.H. and P.K.M. supervised the research. All the authors discussed the results. A.A. and P.K.M. wrote the manuscript with the assistance of all the authors.

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Notes

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