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Trapping processes and band discontinuities in Ga_2O_3 FinFETs investigated by dynamic characterization and optically-assisted measurements

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ABSTRACT

In this paper, we analyze the threshold voltage stability of beta-Ga_2O_3 FinFETs for power applications using Al_2O_3 as gate insulator. In dynamic characterization measurements, when the filling bias condition is moved from off-state to on-state a positive threshold voltage shift is induced, caused by the trapping of electrons in the insulator or at the insulator interface with the semiconductor.

The threshold voltage variation was found to be stable in rest condition, but illumination by 280 nm UV light was able to slowly recover the threshold voltage even below its value before the filling condition was applied, suggesting the presence of natively trapped charge into the oxide even in the as-grown device. In order to obtain more information on the role of the external illumination, monochromatic excitation in the range from 1.5 eV to 5 eV was applied to the device before a transfer characteristic measurement. Results show that photon energies lower than 2.2 eV cause a positive threshold voltage shift, caused by charge trapping during the measurement phase and not related to illumination. Photon energies between 2.2 eV and 3.5 eV promote electron detrapping, leading to a partial recovery in the threshold voltage. Finally, energies above 3.5 eV cause an additional charge trapping process.

The physical origin of the photon energy difference was investigated by monochromatic light-induced current transients, and a suitable model considering the conduction band discontinuities between the gate metal and the oxide and between the oxide and the semiconductor was developed to explain the experimental data.

Keywords: Gallium oxide, FinFET, threshold voltage instability, charge trapping, band discontinuity

1. INTRODUCTION

Gallium oxide in the beta crystal structure is a promising material for next generation power electronics, thanks to its high bandgap, critical electric field and mobility, and only a minor loss in thermal conductivity compared to other wide bandgap semiconductors [1]–[3]. Both diodes and transistors based on beta-Ga_2O_3 with excellent performance are already demonstrated, relying on various device structures [4]–[8]. The current trend in power electronics is to move to vertical device topologies, which result in higher breakdown voltage and higher current density for the same area use of a lateral device [9]–[11]. The use of gate insulators in devices at a low technology readiness level still poses problems of performance and reliability that have to be addressed [12], [13].

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2. EXPERIMENTAL DETAILS

The devices under test are based on the FinFET architecture. The structure is fully vertical, so the Ti/Au drain contact is placed directly below the substrate. The drift region is a 10 µm thick n^--Ga_2O_3 layer grown by hydride vapor phase epitaxy (HVPE) on top of a n-doped (001) Ga_2O_3 substrate. The 1.39 µm fins are obtained by dry etching of the drift layer. The gate insulator is Al_2O_3, deposited by atomic layer deposition (ALD) and 35 nm thick, and the gate metal is a 50 nm Cr layer. In order to improve the source contacts, the Ti/Al/Pt stack is deposited on top of a 400 nm n^+-Ga_2O_3 layer, obtained by ion implantation of silicon atoms. Al_2O_3 is used also as the spacer between the gate and source metals, which are also used to form field-plate structures. The sketch of the structure is shown in Figure 1, and more details can be found in [14]. The behavior of the sample was investigated by means of pulsed I_D-V_G measurements, I_D-V_G sampling and photoassisted I_D-V_G and I_{DG} measurements.

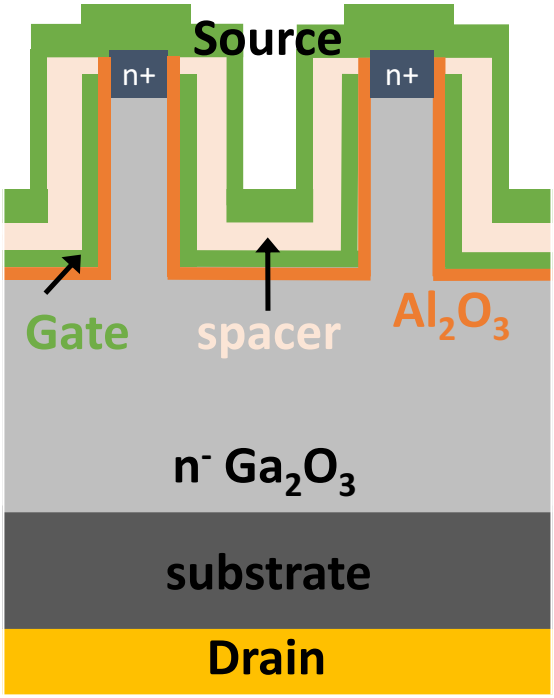

Figure 1. Schematic structure of the FinFETs under test.

3. THRESHOLD VOLTAGE INSTABILITY

A common occurrence in insulated gate devices is the presence of electron trapping at high positive gate bias, due to the injection of the channel electrons into the gate dielectric. This effect is present in the devices under test, as shown in Figure 2 (a): when the filling gate bias is higher than the OFF-state voltage a rigid positive shift in the I_D-V_G is visible, caused by the electrostatic repulsion between the electrons trapped in the gate oxide and the electrons of the channel. The amount of threshold voltage variation and the filling gate voltage leading to it is shown in Figure 2 (b). The electrons are supposed to be trapped in interface or border traps [15].

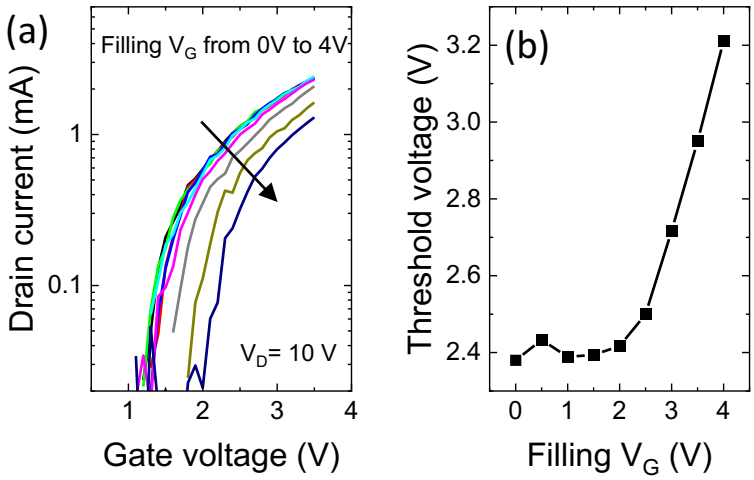

Figure 2. (a) positive shift in the I_D-V_G curve and (b) dependence on the filling gate voltage during pulsed I_D-V_G measurements at increasing positive gate filling bias..

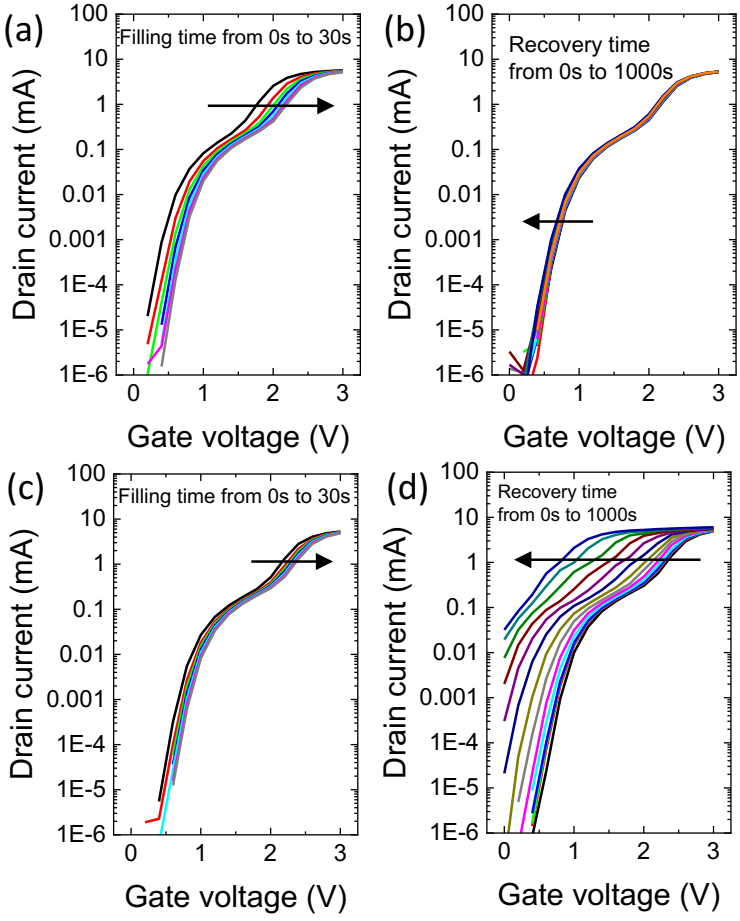

Figure 3. Repeated I_D-V_G measurements during (a, c) filling at V_G = 4V and V_D = 0V, and (b, d) and recovery time. The recovery is carried out at room temperature in (b) dark condition and (d) under 288 nm UV light.

The detected variation in threshold voltage can, in principle, be caused also by a permanent degradation of the device. In order to understand if the charge trapping hypothesis is correct, we monitored the shift in the I_D-V_G curves during filling and recovery time, as shown in Figure 3 (a-b). The detected shift, plotted in Figure 4 (a-b) is only partially recoverable at room temperature, a finding compatible with emission of trapped electrons but not excluding possible degradation effects.

For this reason, the same experiment was carried out by shining UV light with a 288 nm LED. As shown in Figure 3 (c, d), the photons are able to promote the de-trapping of electrons, suggesting that no permanent degradation takes place in the filling phase.

Moreover, the threshold voltage recovers to a value even lower than the initial one (see Figure 4 (c, d)), suggesting that in the initial state of the sample some electrons are natively trapped in the oxide, possibly deeper in energy or position than the ones filled in the filling phase, which can be removed by the high-energy photons.

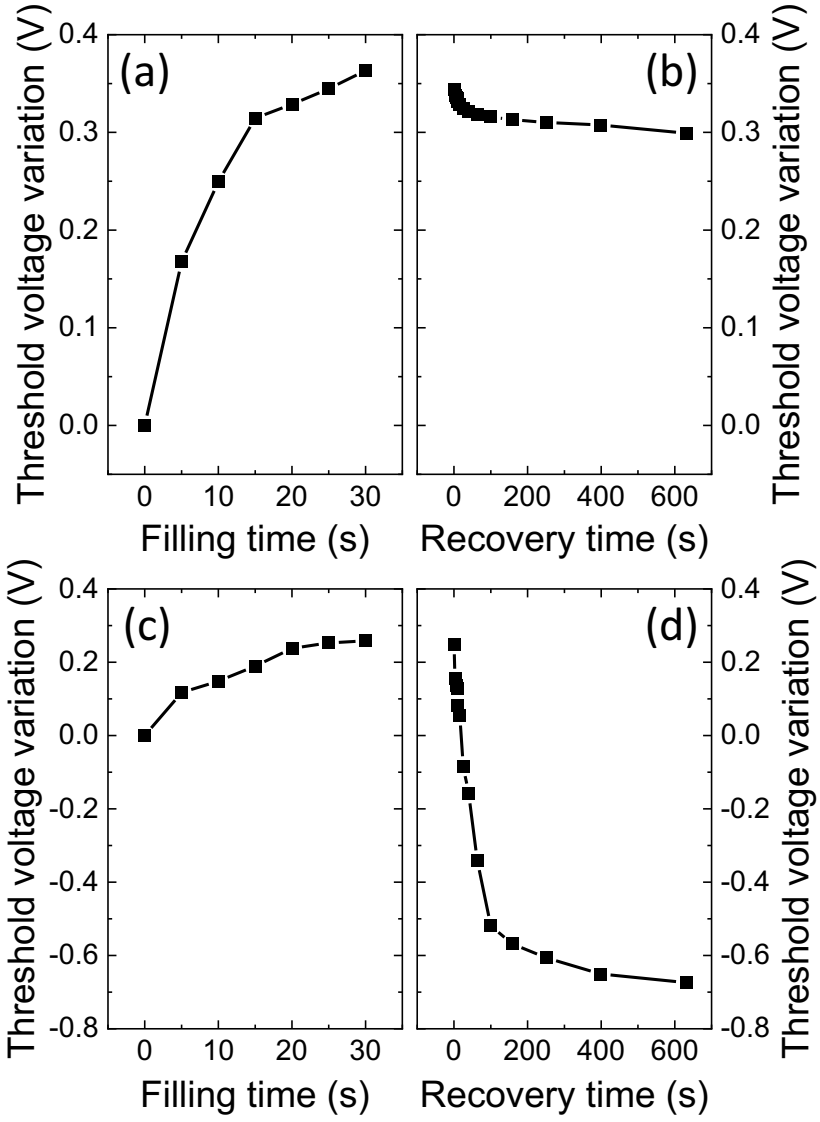

Figure 4. Shift in threshold voltage extrapolated from the I_D-V_G measurements in Figure 3.

4. EFFECT OF MONOCHROMATIC LIGHT

The finding that light is able to penetrate the structure and lead to a change in trap charge state is relevant, since it allows for characterization of the related deep levels by means of monochromatic photoassisted measurements. The devices are measured in dark condition, after five minutes of illumination in rest bias condition.

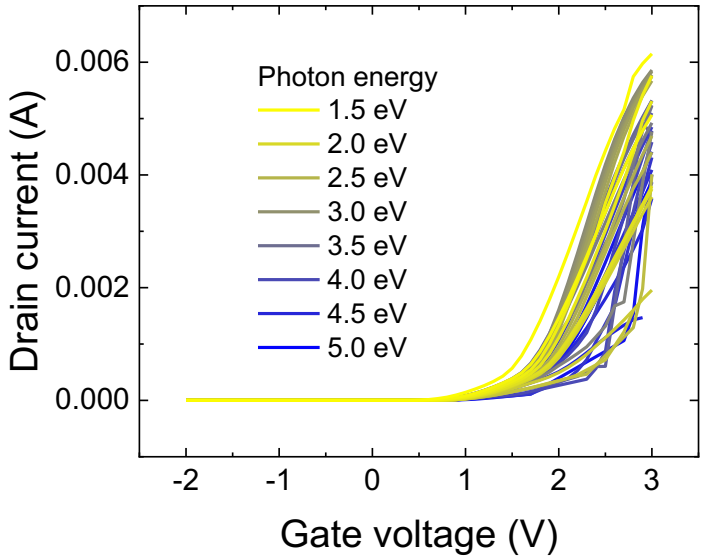

Figure 5. Variation in I_D-V_G measurements under excitation with monochromatic light with different photon energy.

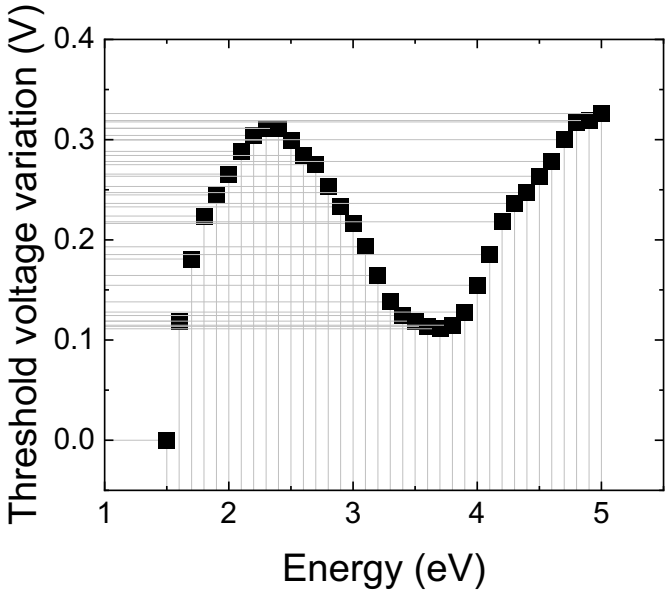

Figure 6. Variation in threshold voltage extrapolated from the measurements in Figure 5. Gray lines are guides for the eye.

The results of the I_D-V_G measurements, shown in Figure 5, highlight a complex interplay between the photons and the behavior of the device. Analysis of the threshold voltage variation, reported in Figure 6, shows a positive shift up to 2.2 eV, followed by a negative shift up to 3.5 eV and by a subsequent additional increase.

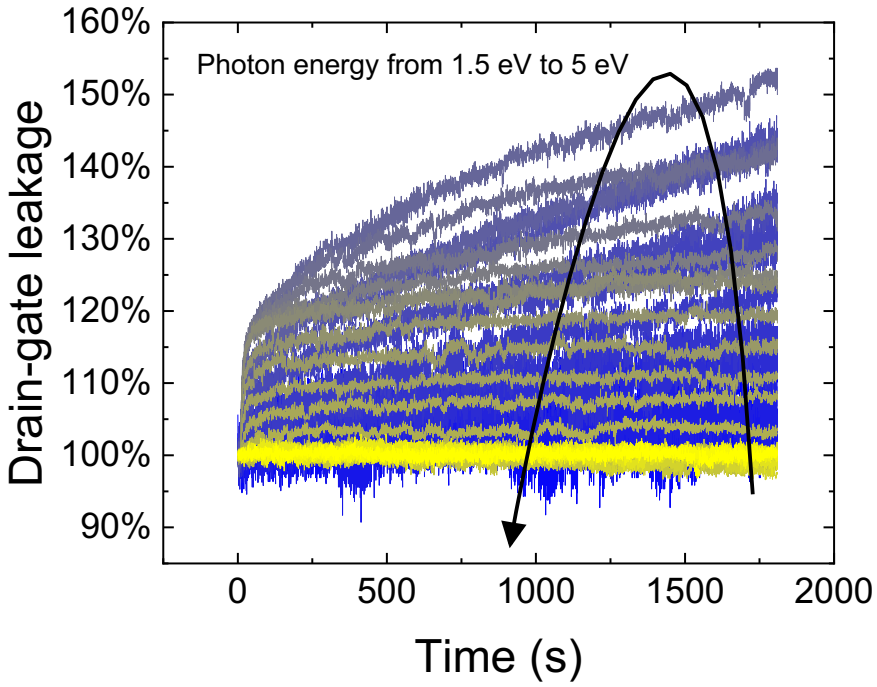

Figure 7. Variation over time in drain-gate leakage induced by illumination with photon energies from 1.5 eV to 5 eV, step 0.1 eV. A non-monotonic trend is detected.

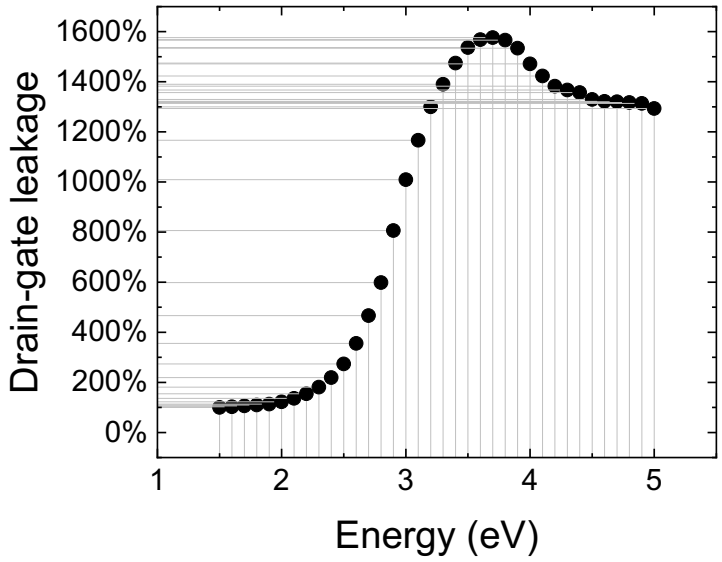

Figure 8. Variation in drain-gate leakage extrapolated from the measurements in Figure 7. Gray lines are guides for the eye.

The interpretation on the physical meaning of this result relies on additional photoassisted current transient measurements, in a configuration similar to the one of internal photoemission spectroscopy measurements (IPS). The measurement of the drain-gate leakage at VG = 0 V and VD = 2 V under monochromatic light is shown in Figure 7, and the corresponding end value of the current transient is plotted in Figure 8 as a function of the photon energy.

Below 2.2 eV the drain-gate current does not change, since the energy is not high enough to remove the trapped electrons or to transfer electrons across the gate dielectric. Therefore, the detected increase in threshold voltage is ascribed to the effect of the cumulative I_D-V_G measurements, where the gate is brought up to 3 V, enough to induce some charge trapping as shown in Figure 2. Between 2.2 eV and 3.5 eV, the photon energy is high enough to promote detrapping. The detrapped electrons drift towards the drain increasing the measured leakage, and the lower electrostatic repulsion causes the recovery in the threshold voltage. Above 3.5 eV, electrons from the metal are injected in the insulator, leading to additional electron trapping. This electron trapping produces the increase in threshold voltage, due to the increase in electrostatic repulsion, and the decrease in leakage current, since they oppose the injection of additional electrons from the metal towards the oxide. A 3.5 eV barrier in the conduction band between Cr and Al_2O_3 is confirmed by some reports in the literature [16], [17].

5. CONCLUSIONS

In summary, we analyze the threshold voltage stability of beta-Ga2O3 FinFETs for power applications using Al_2O_3 as gate insulator. After a filling bias condition a threshold voltage shift is induced, recoverable by illumination with UV light. Illumination with different photon energies causes positive or negative threshold voltage shifts, depending on the specific wavelength used. By means of monochromatic light-induced current transients a suitable model considering the conduction band discontinuities between the gate metal and the oxide and between the oxide and the semiconductor was developed to explain the experimental data.

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