A 3.1-51GHz, Sub-8mW, Single-Core LC VCO Based on a Novel Compact Tunable Transmission Line (CTTL) Resonator in 28nm FDSOI CMOS

Thomas Tapen[#1], Andreia Cathelin[$2], Alyssa Apsel[#]
[#]Cornell University, USA
[$]STMicroelectronics, France
[1]tpt26@cornell.edu, [2]andreia.cathelin@st.com

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***Abstract*— The adoption of 5G standards requires new wireless devices to support not only traditional RF bands, but also mmW frequencies up to and beyond 40GHz. Such mmW hardware typically requires narrowband LC resonant circuits for efficient, low-noise operation. For widely-tuned software-defined systems, multi-octave LC tuning is not achievable due to the lack of a practical, solid-state tunable inductive element, limiting the mmW performance of software-defined radios. In this paper, we present a novel, compact, lumped/distributed LC-equivalent resonator capable of continuous tuning over more than four octaves in frequency while maintaining a practical quality factor in an unmodified 28nm FDSOI CMOS for the first time. This resonator is used to implement a cross-coupled LC VCO tunable from 3.1 to beyond 51GHz requiring less than 0.208mm^2 of area, less than 8mW of power, and achieving a state of the art peak FOM$_T$ for multi-octave tunable mmW VCOs of -198.2dBc/Hz.**

***Keywords*— tunable circuits, digital-controlled oscillators, voltage-controlled oscillators, millimeter wave, wideband, tunable filter, 5G, FMCW radar**

I. Introduction

With the advent of 5G and millimeter wave (mmW) wireless standards, RF hardware designs must achieve high performance from sub-GHz frequencies to 40 GHz and beyond. For multi-standard and software-defined radios, this requires an LO tunable across multiple octaves from low RF to mmW frequencies. Typically, ultra-widely tunable frequency synthesizers use a narrowly tuned VCO in conjunction with dividers and/or multipliers to achieve multi-octave tuning (e.g. [1]). However, divider-based VCOs do not scale well compared to standalone LC VCOs at mmW frequencies as the VCO must always operate at or above the highest desired frequency of operation. Frequency multipliers can be used to extend the tuning range upward, but active multipliers will also consume additional power and degrade phase noise performance ([2]). Finally, multiple narrowly tuned VCOs can be switched between for wide tuning, but this approach scales very poorly in required area ([3], [4]).

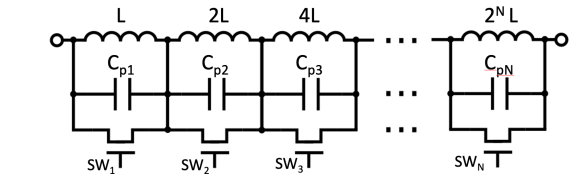
Ideally, a conventional LC VCO could simply be tuned across a wide range of frequencies, however this generally requires a form of tunable inductance in order for the resonant circuit to maintain a constant impedance at resonance across a wide tuning range. Existing integrated tunable inductor designs suffer from one or more of the following: very low quality factor (Q), narrow tuning range ([5]), additional power consumption and reduced linearity ([6]), or require exotic devices/processing such as MEMS approaches ([7]), making multi-octave inductively-tuned LC circuits impractical.

In this paper, a compact, lumped/distributed resonant LC structure is presented capable of over four octaves of tuning range with moderate Q, suitable for use as a standalone shunt resonator or a variable inductor in an LC tank circuit. To demonstrate the performance of the structure, a single core LC VCO is designed with greater than four octaves of tuning range. This ultra-wide single VCO tuning avoids the area costs associated with array-based VCOs, and the power costs associated with mmW divider/multiplier-based VCOs. The result, to the authors' best knowledge, is the first practical, integrated, multi-octave tunable LC resonator in an unmodified CMOS technology and the highest peak FOM$_T$ of a multi-octave tunable mmW VCO presented to date. The paper is organized as follows: Section II describes the novel LC resonator's design and behavior as a compact, tunable transmission line (CTTL) resonator. Section III discusses the design of the CTTL-based low-power VCO in the 28nm FDSOI process. Section IV presents the measured performance of the CTTL-based VCO and a comparison to existing widely tunable VCOs.

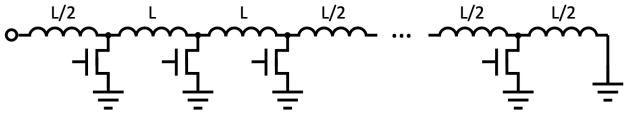
II. Compact, Tunable Transmission Line (CTTL) Design

Conventional tunable inductors based on CMOS switches are limited in Q due to the combination of non-negligible on-resistance and off-capacitance of CMOS switches. The performance of an RF CMOS switch in this regard can be described in terms of a theoretical cutoff frequency $F_{CO} = 1/(2\pi R_{ON} C_{OFF})$. Assuming a constant transistor length, F_{CO} will be approximately constant across switch width in a given technology. For a simple switched inductor (Figure 1a), the total C_{OFF} must not lower the inductor's self-resonant frequency (SRF) too close to the highest desired frequency of operation. Because F_{CO} is constant, requiring low C_{OFF} inevitably implies a large R_{ON}. Therefore, tunable inductors typically have large resistive losses and very low Q, a narrow tuning range, or both.

In order to break this trade-off, the tunable transmission line structure shown in Figure 1b is proposed. Here, when all the NFET switches are off, each tap along a series inductance sees the parasitic shunt capacitance of each switch



(a)



(b)

Fig. 1. Two tunable inductors. (a) A basic switched inductor, where the parasitic switch capacitance C_p must be kept small for the overall circuit to act as an inductor across a wide frequency range. (b) The proposed compact, tunable transmission line structure (CTTL) implemented as a shunt inductor/resonator, where switch capacitance is absorbed to create an artificial transmission line to allow larger, lower loss switches.

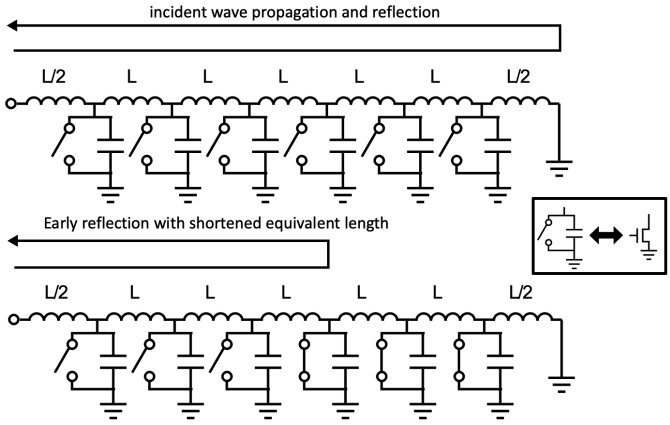


Fig. 2. The constant Z_0, ultra-wide tuning of the CTTL structure. As switches are sequentially closed from the shorted end of the line, the effective line length is shortened, and therefore the resonant frequency increases. The resonant frequency $f_0 \propto$ (number of non-shorted taps)$^{-1}$.

(C_{OFF}), presenting an artificial transmission line structure with characteristic impedance $Z_0 \approx \sqrt{L/C_{OFF}}$ and electrical delay $\tau \approx N\sqrt{L \cdot C_{OFF}}$ where N is the total number of taps. To implement a resonator, this transmission line is shorted at one end, presenting a $\lambda/4$ transmission line stub. Unlike conventional tuned inductor designs, here the parasitic switch capacitance is absorbed to create the desired transmission line structure, and so a much higher C_{OFF} can be tolerated, implying a much lower R_{ON} and therefore a much higher overall Q. The NFET switch width can be calculated to present the desired C_{OFF} from the desired Z_0 and τ of the transmission line stub resonator.

With these appropriately sized NFET switches in place, the switches can be turned on one-by-one to short sections of the line to ground, effectively shortening the length of the line with a constant Z_0 and increasing the resonant frequency (Figure 2). Thus wide frequency tuning with fixed Z_0 is achieved. Assuming equal inductance between switches, the transmission line structure can be tuned over a range $f_{max}/f_{min} \leq N$.

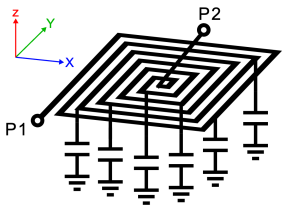


Fig. 3. The proposed 3D layout of the CTTL. The capacitive NFET switches are integrated in the substrate below the 2D spiral on a top metal layer. Taps are placed as necessary to achieve equal inductance between switches.

A. *Area-Efficient Layout*

To implement a compact, tunable transmission line (CTTL) stub as described above, we observe that the multiple series inductors in Figure 1b can be implemented by a single, fixed inductor with many taps. Because the NFET switches are designed to present C_{OFF} to ground at each tap, they can be located underneath the spiral inductor to eliminate tap routing parasitics and further reduce the required area (Figure 3). Thus, the tunable structure occupies only the area necessary for the total required inductance at the lowest frequency of operation.

In this layout, the many inductor segments are multiple turns around a common center, resulting in mutual inductive coupling between each segment. In order to implement the desired transmission line-like behavior, this mutual coupling must be kept low, and so a wide turn spacing is desired in the indctive spiral. The effect of moderate mutual coupling is observed as a degradation of the artificial transmission line's Bragg frequency and an increase in τ in E/M simulation. As more taps are shorted to ground, more of the mutual coupling will be to the shorted section of line and the Bragg frequency degradation is reduced. Therefore, as long as the degraded Bragg frequency remains significantly higher than the $\lambda/4$ frequency of the line at all settings, proper operation is ensured, albeit with a frequency shift due to the variation in τ. The limited impact to Bragg frequency in the proposed spiral layout is confirmed by measurement in Figure 6.

III. Ultra-widely Tunable VCO Design using CTTLs

To demonstrate the extreme tuning range and acceptable Q of the CTTL structure, a simple cross-coupled LC oscillator design is adapted to use a symmetric, dual-CTTL load in place of a center-tapped LC tank (Figure 4). Because tuning range and/or tuning resolution of the CTTL increases with more taps, a very large number of taps (29) is chosen to achieve tuning greater than four octaves with as much tuning resolution as possible. To provide continuous tuning between CTTL bit settings, small varactors are added to the oscillator.

The 28nm FDSOI technology provides $F_{CO} \approx$ 500GHz at 1V V_{GS} including the forward body biasing technique ([8]), which is a significantly higher F_{CO} than regular bulk CMOS technologies. The CTTL switches and cross-coupled NFETs use LVT devices with a forward body bias equal to their DC gate bias. For the cross-coupled NFETs, this increases g_m and so reduces phase noise. The cross-coupled NFETs

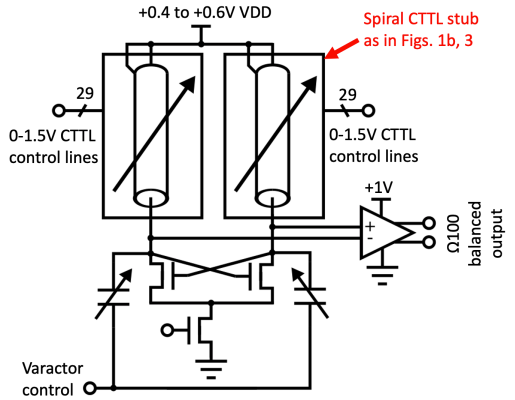


Fig. 4. The VCO schematic. Two CTTLs each with 29 taps provide the LC resonant structure, which is driven by a pair of cross-coupled NFETs. Fine, continuous tuning is provided by small MOS varactors. Output buffer power is not included in reported power consumption. Not shown are peak detectors used to verify the internal oscillator amplitude.

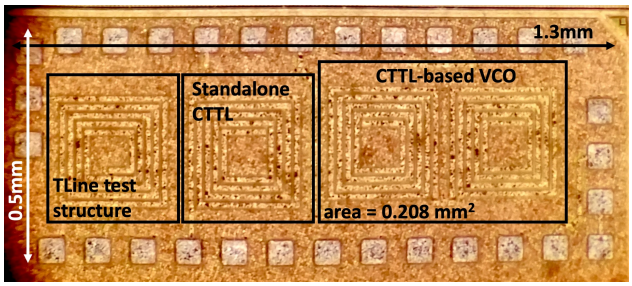


Fig. 5. The manufactured die including the VCO and test structures.

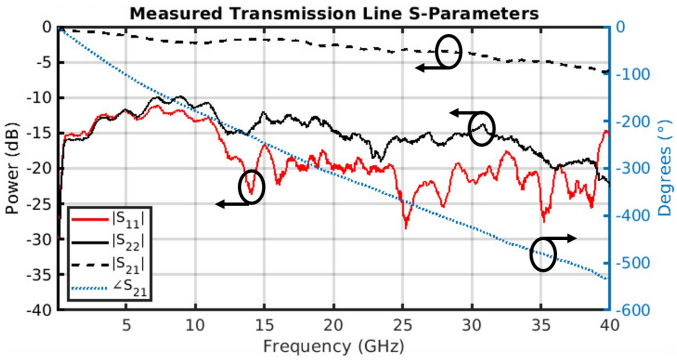


Fig. 6. Measured s-parameters of the non-tunable spiral artificial transmission line test structure showing good wideband performance despite the effects of non-uniformity and mutual inductance given the compact spiral layout.

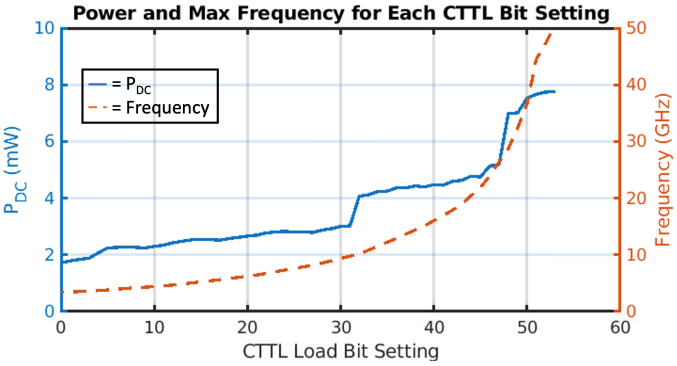


Fig. 7. Measured maximum VCO frequency and power consumption across CTTL bit settings. Because each CTTL has 29-taps, the two combined provide the 58 unique bit settings. Settings 55-58 may operate beyond the measurement limit of 51GHz, but this cannot be confirmed and they are omitted in this plot.

are minimum length to minimize their parasitic capacitance, however due to the FDSOI process they exhibit high 1/f noise, resulting in a 1/f corner frequency of ∼5MHz in simulation. In the CTTL NFETs, forward body bias provides higher R_{ON} vs V_{DS} linearity, and can be leveraged to either increase the Q or increase the allowed number of taps and therefore the tuning range. In order to maximize RF switch performance, the CTTL tap NFET gates are driven from 0 to 1.5V. For VCO node swings between 0 and 1V, this satisfies the maximum $|V_{GS}| \leq 1$V when a switch is off. When a switch is on, its drain is shorted to $V_{DD} = 0.5V$, and no significant swing is present on the source or drain, allowing a safe gate drive of 1V + V_{DD} =1.5V.

IV. Measured Performance and Comparison to Existing VCOs

The manufactured die is shown in Figure 5. The oscillator itself occupies less than 580x353 um, while the remaining area is consumed by two test structures. One is a capacitively-loaded spiral without switches to demonstrate the wideband transmission line performance despite mutual inductance effects, and the other is a passive, standalone CTTL resonator.

First considering the transmission line test structure, 2-port s-parameter measurements are shown in Figure 6. The Bragg frequency for a 12-tap, $Z_0 = 50\Omega$ line is clearly in excess of the measurement limit of 40GHz of the Agilent 8722ES VNA used for measurement. This shows f_{Bragg} is more than 10x the $\lambda/4$ frequency of 4.3GHz.

The VCO core itself has a continuous tuning range of 3.1GHz to beyond the Agilent 4448A's measurement limit of 51GHz. The VCO consumes a maximum of 7.7mW at 51GHz down to a minimum of 1.9mW at 3.23GHz as shown in Figure 7. Operated on a 0.4V supply, the VCO can be run as low as 1mW at 3.2GHz. The phase noise at 40MHz offset and FOM_T are shown across VCO frequency in Figure 8. A 40MHz offset is chosen due to the wide expected 1/f noise corner as discussed in Section III which is confirmed in Figure 8. Peak FOM_T is calculated using the offset where the phase noise skirt meets the measurement noise floor. Some discrepancy can be observed between the 40MHz phase noise plot (left side of Figure 8) and the representative phase noise curves (right side of Figure 8) as the latter were taken with an Agilent 8563EC with significantly lower input sensitivity and therefore a poorer ability to resolve phase noise at wide offsets for higher carrier frequencies with lower output amplitudes. The 4448A measurements (left of Figure 8) are therefore more accurate where there are any discrepancies.

Table 1 compares the presented VCO to other widely tunable VCOs. We present unmatched tuning range for a single VCO core, which improves our area compared with multi-core

Table 1. Comparison with State of the Art Widely Tunable VCOs

	[3]	[4]	[1]	[9]	[10]	[11]	**This Work**
Technology	0.35μm SiGe HBT	0.35μm SiGe HBT	90 nm CMOS	65 nm CMOS	90 nm CMOS	65 nm CMOS	28nm FDSOI CMOS
Frequency (GHz)	3 - 23	8 - 32	0.01 - 7	25 - 38	9.9 - 20.3	1 - 12[1]	**3.1 - 51**
Power (mW)	200 - 400	452	9.6 - 15.6	17.5 - 21.6	5.2 - 7.1	0.8 - 7.2[1]	1.9 - 7.7
# of VCOs	3 + div. by 2^n	3 + div. by 2^n	1 + fractional ILD	1	1	1	1
Phase Noise (dBc/Hz)	-108 to -125 @1MHz	-82.5 to -110 @1MHz	-111.4 to -123.1 @1MHz	-112 to -121 @3MHz	-84 to -103 @1MHz	-119.2 @10MHz	-101.3 to -131 @40MHz
Area (mm^2)	1.8	<3.18	0.05	0.08	0.0029	0.03[1,3]	0.208
FOM$_T$ (dBc/Hz)[2]	-191	-177	-204	-199	-186[3]	-184[3]	-198

[1] VCO only [2] $\text{FOM}_\text{T} = L(\Delta f) - 20\log(\frac{f_0}{\Delta f} \cdot 10FTR) + 10\log(\frac{P_{DC}}{1\text{mW}})$, $FTR = \frac{2(f_{max}-f_{min})}{f_{max}+f_{min}}$ [3] Estimated from plots

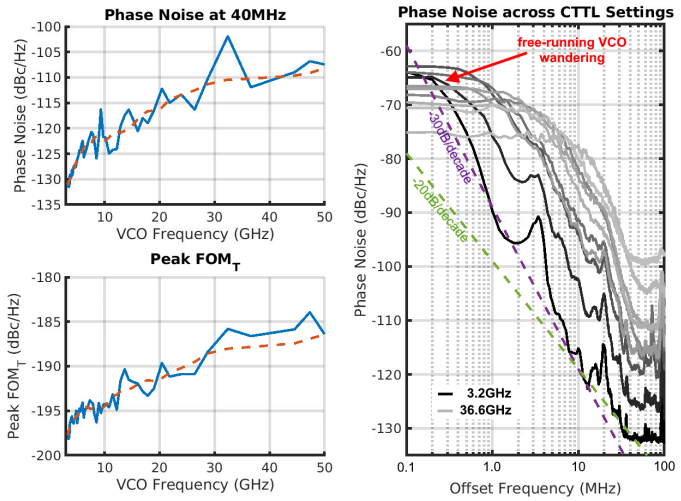


Fig. 8. The measured free-running VCO phase noise at a 40MHz offset from the carrier across frequency, peak FOM$_T$ across frequency, and representative phase noise plots from 3.2 to 36.6GHz. Flat phase noise at small offsets is due to the free-running VCO wandering most significant at higher frequencies.

designs, and our FOM$_T$ compared with other mmW VCOs. [1] presents a higher FOM$_T$, however this is only achieved up to 7GHz by dividing a 7.8-10.5GHz VCO. Techniques similar to the approach in [1] generally provides the highest FOM$_T$ in the literature below 10GHz, but they do not scale to mmW frequencies without a FOM$_T$ penalty as VCO FOM degrades and frequency divider power consumption increases at higher frequencies. [9] also shows marginally better FOM$_T$, but achieves less than one octave of tuning range. Therefore, the benefit of CTTL-tuned VCOs is the combination of ultra-wide tuning, compact area, and high power efficiency (i.e. high FOM) beyond 10GHz—a combination which cannot otherwise be found in the literature to this extent.

V. Conclusion

In this paper a novel design for a compact, tunable transmission line (CTTL) resonator with practical Q over more than four octaves of tuning range is presented. To demonstrate the resonator's practicality, a four-octave continuously tunable LC VCO is designed with compact area and high FOM$_T$ compared with state of the art multi-octave tunable VCOs in the same frequency range. This VCO and the concept of CTTL-resonant circuits in general presents a new opportunity for compact, low-power, software-defined mmW hardware.

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