A Novel, Software-Defined Control Method Using Sparsely Activated Microcontroller for Low-Power, Multiple-Input, Single-Inductor, Multiple-Output DC–DC Converters to Increase Efficiency

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***Abstract*—This paper proposes a novel control for the multiple-input, single-inductor, multiple-output (MISIMO) dc–dc converters. It is digitally and discretely implemented, which can have an outstanding performance in low-power applications so that at the power of 10 mW, it has an efficiency of 92.5%. Conventionally, in this power range, an attempt is made to take advantage of an analog design that is flexible. Thus, a fully programmable (software designed) converter with digital design using a microcontroller is in great demand. This converter design basis is to deploy the microcontroller's central processing unit (CPU) as little as possible. Also, it only turns on the CPU when necessary to be employed in low-power, portable systems, e.g., energy-harvesting technologies. Therefore, construction costs are significantly reduced. Depending on the energy level of the inputs, they can simultaneously be utilized to charge the outputs. This paper uses stability analysis, time-multiplexing control method, and variable-frequency pulse-width modulation in the proposed control design. Each output can be charged with different frequencies according to its load, and the maximum switching frequency is equal to 10 kHz. Also, the proposed technique for zero-current switching has been digitally implemented; it can be utilized to determine the optimal value of the inductor discharge duty cycle based on the inductor's left-side voltage. Comparative simulations and experimental results reveal the superiority and practicality of the proposed approach.**

***Index Terms*—Multiple input single inductor multiple outputs (MISIMO) dc–dc converter, time-multiplexing control, variable-frequency pulse-width modulation (PWM), zero-current switching (ZCS).**

I. Introduction

MANY power consumers, such as portable electronic equipment, telecommunication circuits, data transmission, etc., require several independent supply voltages [1]–[10]. Especially in the last decade, there has been an across-the-board need for portable electronic equipment. Such electronic equipment usually has an electronic power management system (EPMS) to deliver regulated and stable supply voltages to various consuming parts, including processors, Bluetooth and Wi-Fi modules, radio frequency power amplifiers, and LCD modules [1]–[5]. With more applications and integration of these circuits and modules onto smaller motherboards and using system-on-chips, more stringent performance metrics for systems in terms of the need for smaller footprints, lower cost, and higher efficiency are faced.

In EPMSs, a dc–dc converter controller can be either analog or digital. In the past, analog implementations have mostly been preferred—see [1], [11]—while newer implementations use digital and discrete design more and more. Digital implementation requires many digital gates (e.g., see [12]), which are very suitable for the integrated design, but not so ideal for discrete design. The same digital design can also be done using a microcontroller. Since most systems have a processor available, control of the dc–dc converter can be delegated to the same processor. This idea already exists [13].

Utilizing a microcontroller has several significant challenges. First, turning on and off the switches with software commands, on the one hand, dramatically increases the power consumption of the microcontroller because the microcontroller must always be on to control the converter. This matter can be a problem in wireless systems or cases where the system is low-power, and the microcontroller is not always on [14], [15]. On the other hand, implementing accurate timing by microcontroller commands is not an easy task [16], [17]. For example, if the microcontroller receives an interruption, the timings will be disrupted. This article proposes an alternative solution to use microcontroller timers/counters that generate timings by hardware—making power consumption much lower and accuracy much higher.

The microcontroller will only be turned on in order to reset the timing in the timer/counter. In this way, the intervals that the microcontroller turns on reach 1% or even less, which practically reduces or eliminates the effect of the microcontroller power consumption on the power converter efficiency. Therefore, in contrast to integrated design—which is inherently adaptable—our discrete design is flexible with the

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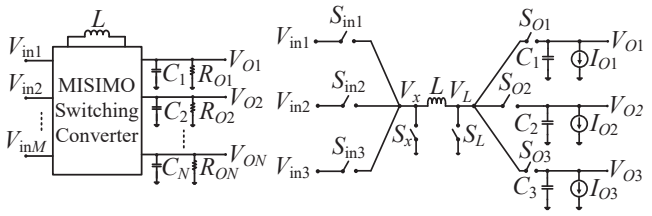

Fig. 1. Power management system: (a) MISIMO switching converter and (b) the three-input, three-output MISIMO converter in this paper.

help of software to achieve a fully programmable (software designed) converter. As a result, a significant reduction in construction costs is seen [15], [18].

EPMSs consisting of several dc–dc switching converters are employed to achieve greater efficiency—thereby receiving their required power from a battery or other energy resources. These switching converters must work independently and have no interference and cross-regulation on each other. The multiple-input, single-inductor, multiple-output (MISIMO) dc–dc switching converter [see Fig. 1(a)] is a low-cost and suitable alternative to the conventional multiple switching converter structures [17], [19]–[25]. The multiple supply voltages affect a switching node in an MISIMO dc–dc converter, cross-regulation occurs between the outputs, significantly affecting the voltage regulation performance in steady-state and dynamic operation, and even in some situations, may lead to system instability. This effect of cross-regulation has been studied in several references (e.g., [1]–[10], [17], [23]), and various control methods have been introduced to improve it. For ease of reference, the "MISIMO dc–dc converter" is referred to as the "MISIMO converter" hereinafter.

In an MISIMO converter, due to the multi-input of this converter, it is possible to use a rechargeable lithium battery, photovoltaic (PV) cells, and thermoelectric generator or any other source that can produce energy. This type of converter should be possible to use several sources to charge the outputs simultaneously. These sources can also be employed to charge the lithium battery when the sources' energy level is high. Such converters can be deployed where battery life is critical, such as energy-harvesting (EH) systems [19]–[22].

This paper aims to discretely design and implement a converter that uses only one microcontroller. Besides, it seeks to use a digital controller, which can be employed in low-power applications; in those applications, the power consumption of the microcontroller becomes essential and must be reduced in some way. In this regard, this paper proposes reducing the power consumption of the microcontroller by making use of the timer/counter hardware of the microcontroller and by time limiting the CPU turning on [12], [14], [15], [18].

Benefiting from multiple inputs also matters. In this regard, having an algorithm to obtain the optimal duty cycle for the input and output switches so that the cross-regulation problem no longer exists is essential in low-power applications. The maximum switching frequency is 10 kHz, which is a relatively low frequency. In low-power applications, when the load value at the output is low, the switching frequency should also be reduced [19], [21]. Furthermore, the controller's power consumption appears substantial—especially at low loads. Thus, it significantly affects the efficiency and hence should be

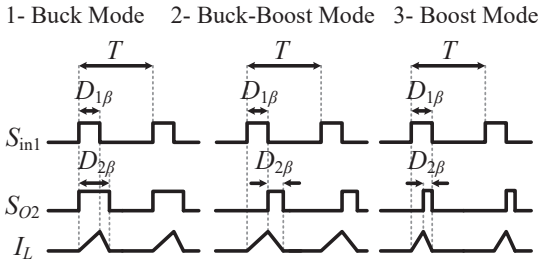

Fig. 2. Converter with the TMC control scheme in three different conversion methods—$D_{1\beta}$ and $D_{2\beta}$ correspond to the inductor's charging and discharging duty cycles assigned to the second output by a single input, respectively.

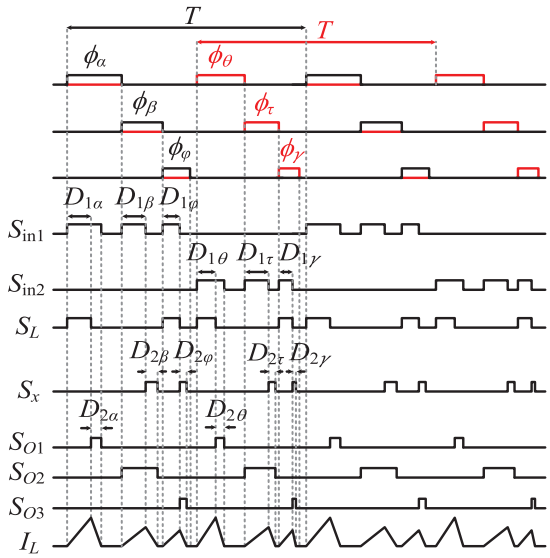

Fig. 3. Timing diagram of the MISIMO converter in the DCM operation.

reduced. For that reason, the controller's CPU should be prevented from being turned on too much in such a case in order to minimize its power consumption. Other applications include medical and portable devices. In those instruments—in order to have long battery life and the best performance for power consumption—the controller's CPU may be turned off for a long time, or EPMS may even require the system to go into standby (or shutdown) when no power is drawn from the output [14], [15].

Some specific MISIMO converters have been considered for EH systems [19]–[22]. Most of these converters have focused on improving efficiency due to the low power at their inputs. These converters work in discontinuous conduction mode (DCM). However, the corresponding control schemes vary with the types and features of the input sources.

The solar EH systems also utilize MISIMO converters with two inputs and two outputs [20]. The first and second inputs are connected to PV cells and a rechargeable battery, respectively. The battery is charged when the PV's energy level is high. The double-conversion rejection technique is introduced in [19]. It transfers power from the three input sources if the energy level of each has reached its maximum. Also, if the output load requires power, the power from the source with a high energy level is transferred to it. Otherwise, the energy of these sources is transferred to the battery. Implementing these systems to harvest energy requires a specific control scheme. Since the energy level at the inputs is inherently low in these MISIMO

converters, the converter must be implemented via integrated designs—which require higher costs [19]–[22]. However, the design of MISIMO converters presented in [17], [23]–[25] is discrete, which indeed demands lower implementation costs. The amount of output and input power and voltage compared to MISIMO converters in [19]–[22] is high, so using such a design for low-power applications makes many challenges.

A deadbeat-based method has been proposed in order to improve the tuning performance in [23], regulating the input current and the output voltage. However, these methods require a slightly more complex algorithm. Most of these converters use the time-multiplexing control method, thus limiting the combination of the desired number of input sources. Since these converters have an inductor, the problem of cross-regulation cannot be ignored. Diminishing it has been addressed in [25].

The reasons detailed above have made the control method more complicated in MISIMO converters. In order to address this challenging complexity, this paper proposes a novel and simple yet control. Without loss of generality, it is designed for a three-input, three-output MISIMO converter connected to a battery; see Fig. 1(b). Depending on the mode, certain switches are turned on/off. Fig. 2 shows the inductor current waveforms (I_L for three different modes) and the signals applied to the first input switch and the second output switch of the circuit in Fig. 1(b) when the second output is charged by the first input in three different modes. Fig. 3 shows its typical timing diagram.

Compared to state of the art elaborated in the literature reviewed earlier, this paper's contributions are as follows.

1) Multiple inputs are simultaneously employed, the algorithm control is digitally and discretely implemented. Also, the controller's central processing unit (CPU) is turned on at a minimum. The proposed algorithm is such that the battery is deployed as little as possible.
2) Due to the low-power design of the converter introduced in this article, it is able to perform in a good power range with relatively high efficiency. This converter works in buck, buck-boost, and boost modes.
3) The maximum switching frequency is relatively low—i.e., 10 kHz. The capability of adjusting the frequency of the pulse-width modulation (PWM) makes it feasible to control the ripple of the supply voltages for different loads and achieve maximum efficiency.
4) The proposed technique for zero-current switching (ZCS) is also digitally and discretely implemented; it is employed to determine the optimal value of the inductor discharge duty cycle according to the inductor's left-side voltage.
5) The use of the timer/counter, as well as minimal CPU usage, has caused the power consumption of this converter's controller to be reduced as much as possible—thus making it an excellent alternative to the whole integrated design.

The rest of this paper is organized as follows. Section II describes the circuit implementation. Section III explains the control algorithm, and Section IV presents the MATLAB simulation results. Section V exhibits experimental results. Finally, Section VI draws this article's conclusions.

II. Proposed DC–DC Converter's Structure

A. MISIMO Converter Topology

The detail of the dc–dc converter circuit design is shown in Fig. 4. The third input is connected to the battery, and the third

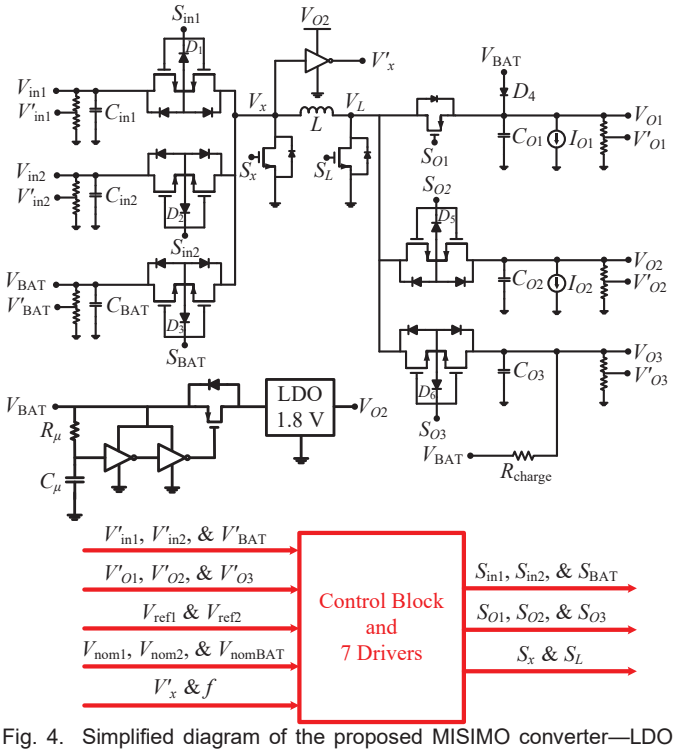

Fig. 4. Simplified diagram of the proposed MISIMO converter—LDO stands for low-dropout regulator.

output is employed to charge the battery. For the first output, which should have the highest voltage, a p-type switch (S_{O1}) has been employed to be turned on simply by reducing its gate voltage. A higher voltage than the output voltage is required to turn on n-type switches, for which the first output voltage is deployed. In such a dc–dc converter system, one of the outputs can supply the microcontroller itself. For this purpose, the second output is assumed to be equal to 1.8 V. When the circuit starts working, the second output is zero and requires a start-up circuit. Therefore, in order to turn on the microcontroller at the system start-up, a low-dropout (also known as LDO) regulator connected to the battery (V_{BAT}) can be used, as shown in Fig. 4.

B. ZCS

The output switches must be turned off when the inductor current reaches zero. If the output switches are switched off too early (i.e., when the inductor current is positive), passing this current through the S_x switch body's diode, the voltage of the node V_x will be equal to $-V_{on}$ of the diode. As a result, some of the energy remaining in the inductor will pass through the p-type switch's diode of the first output. This matter will cause a considerable loss and an unwanted slight increase in the first output voltage. In the opposite case, when the switches are turned off too late and when the inductor current is negative, the current is drawn from the output, thereby reducing efficiency. This current passes through the input switch's diode and causes the voltage V_x to be equal to $V_{in} + V_{on}$ (V_{in} means the desired input). Thus, the zeroing moment of the inductor current should be detected as correctly as possible.

C. Design of the Driver for Power Switches

First, the typical structure with a capacitive load equal to the input capacitor of the power switches connected to the output is simulated in order to design the desired driver; see Fig. 5(a). Considering the drivers' transistors, the driver's current consumption, in this case, is about 120 μA for an 8-V power supply and the 5-kHz switching frequency.

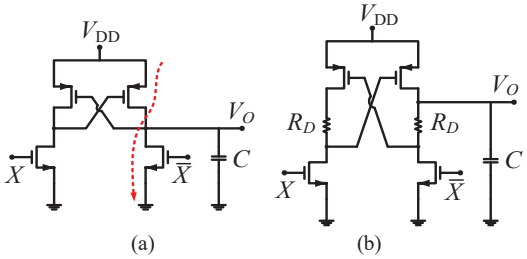

Fig. 5. Power switch's driver: (a) a typical schematic of the level shifter and (b) the proposed driver.

The reason for this relatively high current is due to the rise time and fall time of the microcontroller signal; the one side's switches [see Fig. 5(a)] stay "ON" for a short time, which creates a path from the driver's supply to the ground. Fig. 5(b) shows how a 100-Ω R_D reduces this so-called short circuit current, so the driver's current consumption reaches 40 μA.

III. Control Algorithm

This paper proposes and discusses several algorithms implemented in order to control this converter. Fig. 6 shows an overview of these algorithms detailed below.

A. First Algorithm

The first algorithm is named "*fixed time step - fixed frequency*" and is initially discussed—where the CPU turns on and begins adjusting the duty cycle within a fixed time interval, i.e., t_1 called "*time step*" hereinafter. Also, in this algorithm, the frequency is constant. As shown in Fig. 6, the red and blue blocks are inactive in this algorithm. Analog-to-digital converters (ADCs) sample the output and input voltages without the CPU turning on and stored in memory.

1) Charging Duty Cycle Calculation: When the CPU gets turned on, the error value is first obtained by using the last value of the sampled output voltage. Also, the inductor charging duty cycle [i.e., $D_{1\alpha}$, $D_{1\theta}$, $D_{1\beta}$, $D_{1\tau}$, $D_{1\varphi}$, and $D_{1\gamma}$ denoted by $D_{1\alpha,\,\theta,\,\beta,\,\tau,\,\varphi,\,\&\,\gamma}$] is determined by using the error value described via (1). The inductor charging and discharging duty cycles for each output's inductor of the first part of the paper is also shown in Fig. 3.

$$error = V_{\text{ref}} - V'_{\text{OS}}, \quad \text{and} \quad D_1 = K_p \times error + \sum K_i \times error. \tag{1}$$

The coefficients K_p and K_i are determined by the percentage of error considered for the output voltages. If any of these outputs are inside or outside the range $(1 \pm x\%) \times V_{\text{ref}}$, the coefficients of K_p and K_i will be different based on their mode (buck, boost, buck-boost). In this article, 3% error is taken into account. Due to the high energy level in the inputs intended for battery charging, and since the third output is regarded as a battery charger, the switching frequency of the third output is constant and equal to the maximum circuit frequency (10 kHz). Additionally, because the load equivalent to the battery charger does not change rapidly, the corresponding K_p and K_i coefficients only change based on the third output mode (buck, boost, buck-boost).

2) Desire Input Selection: Every Z minute, the input voltages are compared to their nominal values (V_{nom}). The considered algorithm avoids using the battery as much as possible. Thus, when the values of the first and second input voltages (V_{in1} and V_{in2}) are larger than their minimum value, they can charge the first and second outputs. When each of the first, second, or even both inputs is simultaneously employed to charge the outputs, the battery is no longer used in order to charge the outputs. Also, when the values of the first and second input voltages are larger than their maximum value, they have a high energy level. In addition to charging the first and second outputs, they can also be utilized to charge the battery by the third output. The maximum and minimum values are regarded as the percentages of the nominal voltage.

3) Battery Charging Method Determination: Charging the battery is done with constant current (CC) and constant voltage (CV) methods. The constant current method is applied when the battery voltage is less than 80% of the nominal battery voltage (V_{nomBAT}), determined by the battery datasheet. Otherwise, the battery charging method would be constant voltage. The third output is selected to charge the battery; therefore, the third output reference voltage (V_{ref3}) in the CC method is greater than the battery voltage as much as C, which is a constant value. The third output voltage in the CV method is constant and equal to V_{nomBAT}.

4) Converter Mode and Signal Generator: In order to determine the dc–dc converter mode (buck, boost, or buck-boost) according to the status of the input switches and the third output switch, the reference voltages of each output compare with the active input voltages. The converter mode is specified for each output relative to the input that charges it.

The switching frequency of the third output is constant and equal to 10 kHz and may be different from the switching frequency of the other two outputs. Therefore, dead time must be considered intelligently; for example, suppose the first and second inputs are active, three outputs are being charged simultaneously, and the switching frequency of the first and second outputs is 5 kHz. Fig. 7(a) has shown the considered dead time that the inductor's total charge and discharge time for the first and second outputs is about 15 μs and for the third output is about 20 μs, which in practice is less than this considered time.

For the case where the power of the first and second outputs is lower than the previous case, the switching frequency considered for them is equal to 1 kHz, and the dead times are taken into account, as shown in Fig. 7(b). When the outputs have equal switching frequency, the phase shift value can be determined in terms of the power drawn from each of them.

5) ZCS: Since there is a maximum of 6 charge and discharge phases, 6 ZCSs are considered. Each of these ZCSs works so that it reads and samples the value of V'_x (shown in Fig. 4) in the corresponding phase and stores them in six memory cells. The corresponding phase relates to the falling edge of signals whose falling edge is far from that of the signals given to the output switches as much as t_3. Fig. 8 illustratively explains the ZCS employed in the control algorithm—in which D_{2pw} is the initial value of the discharge duty cycle. D_{2pw} is deployed to enforce V'_x to get close enough to the area in which the current is zero, as indicated in Fig. 8.

For example, $PWM\text{-}S_{\text{O1}\alpha}$ is a signal that is only active in the α phase, and its falling edge is far from the falling edge of the $PWM\text{-}S_{\text{O1}}$ signal in the same phase as much as t_3, where t_3 is considered to be about 100 ns. As it turns out, the output logic level of the inverter is one or zero. When the CPU is on, the last value read by each of these ZCSs is checked. As detailed in

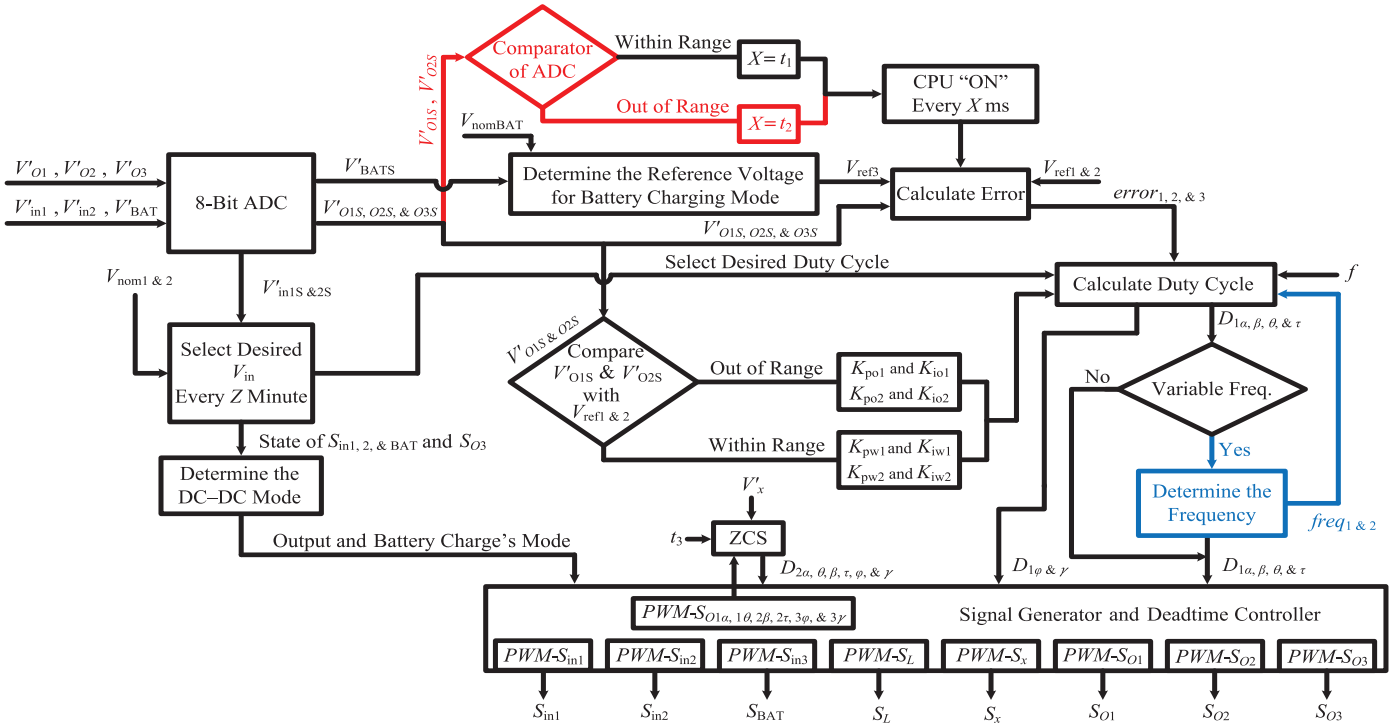

Fig. 6. Proposed control algorithm.

Subsection II-B, if its logic level was zero, i.e., the output switch is turned off late, in this case, the discharge duty cycle is reduced. Additionally, if the logic level was one, it means that the output switch is turned on early, in which case the discharge duty cycle increases.

B. *Second Algorithm*

The second algorithm is named "*variable time step - constant frequency*." Only the blue block in Fig. 6 is inactive in this algorithm. The controller's comparator contrived for the ADC considers a high limit and a low limit for the output voltages. Considering the time step value, switching frequency, and output voltage mode, the K_p and K_i values should be determined in order to ensure the closed-loop system's stability, which is discussed in the next section.

The reason for using this algorithm is that voltage changes in the small range caused by sudden current changes are essential for this category of applications. t_1 is equal to 10 ms, and t_2 is equivalent to 1 ms. When each output voltage is out of range, the CPU starts adjusting the duty cycle for 100 ms with a time step of 1 ms. In other words, it acts as hysteresis. Additionally, if the voltages are within the allowable range, the CPU starts again with the same time step of 10 ms, which can be changed, depending on the application. Even in low-power applications, the CPU can be turned off and only be turned on with a specified time step in the short interval when the voltage of each output is out of range.

C. *Third Algorithm*

The third algorithm is named "*constant time step - variable frequency*." The time step is fixed, but the frequency is variable. The switching frequency value is determined based on the amount of current drawn from the output impacted by the inductor charge time. The red block in Fig. 6 is disabled, and the blue block is active in this algorithm.

The logic level of the pin denoted by the symbol *f* in the algorithm shown in Fig. 6 determines whether or not the system operates at a variable frequency; see Figs. 4 and 6. Initially,

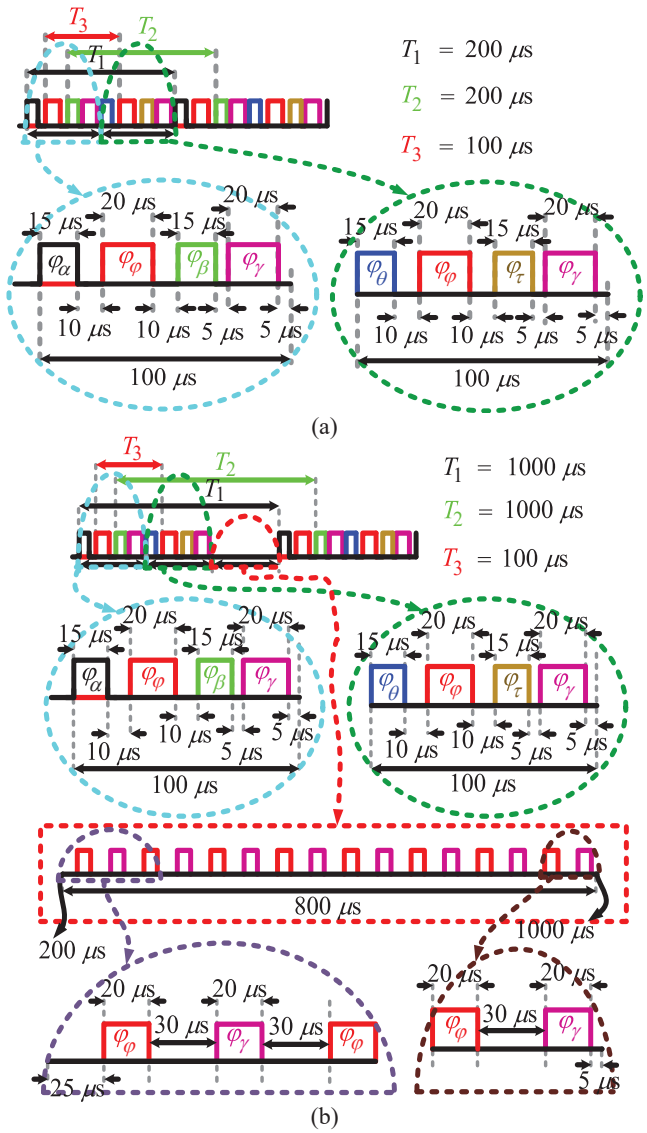

Fig. 7. Various dead time considered.

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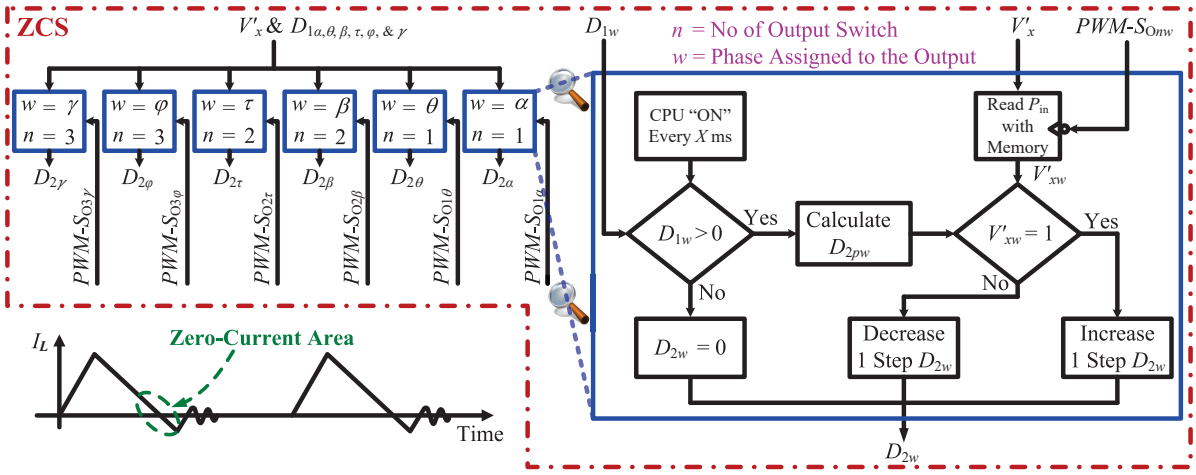

Fig. 8. ZSC employed in the algorithm—in which D_{2pw} is the initial value of the discharge duty cycle.

according to the present frequency of the circuit in each phase, the maximum and minimum values of the inductor charge duty cycles are determined by the maximum and minimum ripple values, respectively. By changing the circuit's frequency, it is necessary to update the maximum and minimum values of the duty cycles. In single input mode, after calculating the inductor charge duty cycle in each phase, its value is compared with the maximum and minimum values of the duty cycle. If it is less than the minimum duty cycle, the frequency decreases, and if it is higher than the maximum duty cycle, the frequency increases.

For the proposed converter, approximations have been made in ripple calculation through (2) and (3) for different modes, and K is equal to $2Lf_s/R_O$. The maximum duty cycle is obtained in terms of R_{Omin} (high load), and the minimum amount of duty cycle in terms of R_{Omax} (light load) is obtained. It is noteworthy that the switching frequencies of the first and second outputs do not necessarily change in the same way; only the output switching frequency whose duty cycle value is out of the range mentioned earlier is altered. Also, the switching frequency of the third output is constant.

For the buck mode,

$$\Delta V = \frac{I_O \times (1-\frac{I_O}{\Delta I_L})^2}{f_s \times C} \simeq \frac{I_O}{f_s \times C}, \quad \text{and} \quad D_1 = \sqrt{\frac{4K}{(\frac{2V_{\text{in}}}{V_O}-1)^2-1}}. \tag{2}$$

For the boost mode and the buck-boost mode,

$$\Delta V = \frac{I_O \times [1-\sqrt{K}]}{f_s \times C} \simeq \frac{I_O}{f_s \times C} = \frac{V_O}{R_O \times f_s \times C}, \tag{3}$$

$$D_1 = \sqrt{[(\frac{2V_O}{V_{\text{in}}}-1)^2-1]\frac{K}{4}}, \quad D_1 = -\frac{V_O}{V_{\text{in}}}\sqrt{K}, \tag{4}$$

$$R_{O\max} = \frac{V_O}{\Delta V_{\min} \times C \times f_s}, \quad \text{and} \quad R_{O\min} = \frac{V_O}{\Delta V_{\max} \times C \times f_s}. \tag{5}$$

For the case where two inputs are simultaneously used, there are two types of ripples since there are two phases to charge and discharge each output. Each ripple results from charging the output by each input. If one or both of the duty cycles assigned for charging the inductor is out of range, there will be several modes, only four of which cause the frequency to change. The switching frequency decreases if both duty cycles are less than the corresponding minimum duty cycle. Also, in cases where one or both of the duty cycles are higher than the corresponding maximum duty cycle, the frequency increases.

The maximum and minimum of two output ripples are considered the same. After obtaining R_{Omin} and R_{Omax} through (5), they are placed in the inductor charge duty cycle formula. Afterward, the maximum and minimum inductor charge duty cycle in each phase is obtained based on the desired V_{in}. The maximum and minimum ripple values are considered 3% and 1% of the final output voltage, or V_{ref}, respectively. Now, suppose voltage changes in a small interval due to sudden changes in current are essential in some applications. In that case, similar to the second algorithm, the time step can be considered variable in addition to frequency. This algorithm can be regarded as the fourth algorithm, named "*variable time step - variable frequency*." The red and blue blocks are shown in Fig. 6 are active in this algorithm. Because the frequency change is discrete, a step must be considered and selected for its variation depending on the application. The minimum and maximum switching frequencies are 100 Hz and 10 kHz.

IV. MATLAB Simulation Results

This section provides simulation results of the proposed MISIMO in the MATLAB/Simulink environment. One of the input voltages is 4 V, and the output voltages for boost and buck modes are 7.2 V and 1.8 V, respectively. The inductance of the inductor is equal to 33 μH. The first, second, and third output voltages are filtered with 22-μF, 32-μF, and 100-μF capacitors—see the Appendix section for the reasoning behind parameter selection and the switching frequencies utilized.

A. Boost Mode Analysis of the Proposed Converters

Since the three outputs are independent, each needs a separate transfer function. Therefore, each output's K_p and K_i values [for the proportional-integral (PI) controller] are calculated so that the phase margin of the system is about 60° for the maximum power value considered in each frequency and sampling time of the system. Next, a lookup table can be deployed for each output voltage mode based on the frequency and sampling time. The output voltage check time is modeled with a delay in the transfer function modeling.

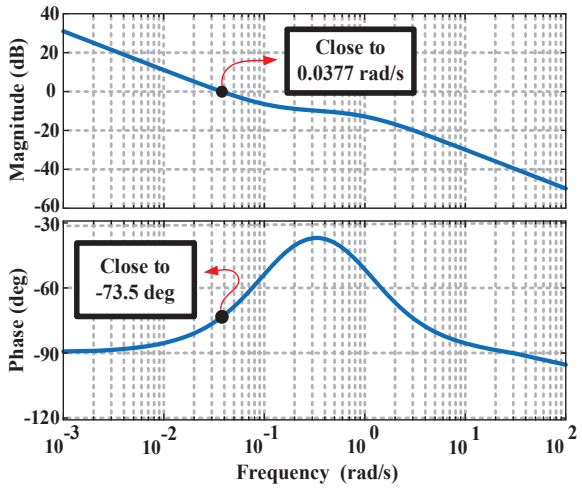

Fig. 9. Bode diagram of the reference-to-output transfer function (i.e, V_{out}/V_{ref}) of the proposed DCM boost converter.

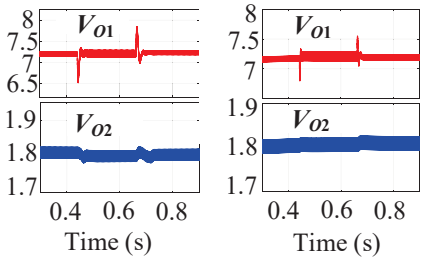

Fig. 10. MATLAB simulation results of output voltages for the time step setting the duty cycle equal to: (a) 10 ms and (b) 1 ms.

For example, for the first output that works in the boost mode—with the switching frequency of 5 kHz, the sampling time of 1 ms, and the output voltage of 7.2 V working at the power of 72 mW and the input voltage of 4 V—the K_p and K_i values are equal to 0.009 and 0.001, respectively. They induce a 73.4° phase margin for the closed-loop system stability, as shown in Fig. 9 simulated in the MATLAB software. The appendix section details the derivation.

B. MATLAB Simulation Results of the Desired MISIMO

In Fig. 10, only one of the inputs is active. As shown in Fig. 10(a), when the current drawn from the first output doubles, the voltage sag at the beginning of the range is about 0.7 V. Every 10 ms, the output voltages are read and compared to the corresponding V_{ref}, then the duty cycles are adjusted. The switching frequency value is constant with 5 kHz and 1 kHz for the first and second outputs, respectively. Typically, the first and second output currents are 10 mA and 1 mA, respectively. If the duty cycles are set with a time step of 1 ms, the voltage drop at the beginning of the current doubling interval is 0.4 V; see Fig. 10(b).

Another test examines the third output with the voltage of 4.2 V, the switching frequency of 10 kHz, and the load current of 40 mA in the buck-boost mode. Two inputs with 3.2 V and 3.8 V are simultaneously active in this test. Fig. 11(a) shows the output voltages waveform, and Fig. 11(b) the ripple of the output voltages and the inductor current. The time step is equal to 10 ms, and by drawing the current twice from the first output, there is no cross-regulation between the outputs according to the dead time.

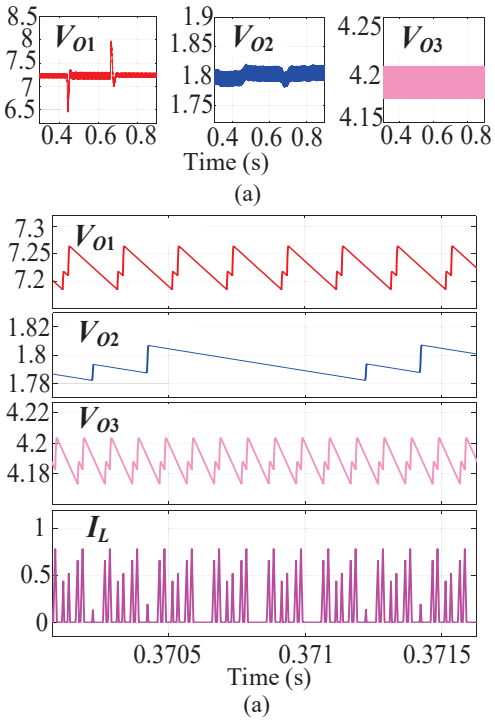

Fig. 11. MATLAB simulation results: (a) output voltages and (b) outputs' ripple and inductor current in some periods.

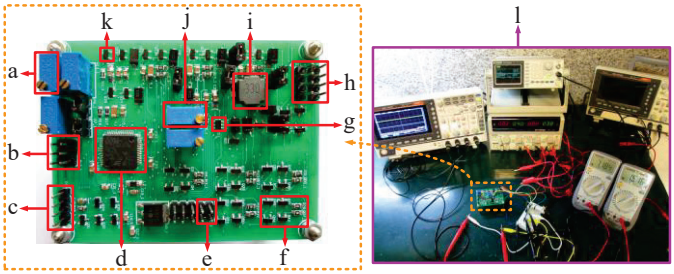

Fig. 12. Hardware setup: (a) output2 load, (b) programmer connection, (c) input voltage source or battery, (d) STM32L476RET6, (e) output voltages, (f) drivers, (g) PMOS power, (h) input voltage sources, (i) inductor, (j) output1 load, (k) NMOS power, and (l) experimental setup.

V. Dynamic Performance and Experimental Results

A. Dynamic Performance

As shown in Fig. 12, a printed circuit board (also known as PCB) is built in order to implement the proposed MISIMO converter and test its performance. The STML476VRET6 microcontroller, the ZXM61N03F NMOS power switches, and the FDC6506P PMOS power switches are used.

The efficiency measured versus the total output power of the proposed converter is shown in Fig. 13. The amount of output loads and input voltages vary in order to get the power range in Fig. 13. The low proportional frequency is one of the primary reasons for having high efficiency at low powers. Also, a brief comparison between the proposed converter and the previously proposed converters is presented in Table I to further illustrate the key features of the proposed MISIMO converter.

B. Experimental Results

Figs. 14–16 show the waveforms of the output voltage, inductor current, and the inductor's right-side voltage (V_L). Some extra tests are performed while the controller employs the proposed method to validate the algorithms. In the first test,

TABLE I
COMPARISONS WITH STATE OF THE ART—VFPWM, PSM, PFM, AND CCM STAND FOR VARIABLE-FREQUENCY PWM, PULSE-SKIPPING MODULATION, PULSE-FREQUENCY MODULATION, AND CONTINUOUS CONDUCTION MODE, RESPECTIVELY

Reference	[24]	[20]	[17]	[23]	[22]	[25]	[19]	Proposed Converter
Process	Discrete	CMOS	Discrete	Discrete	CMOS	Discrete	CMOS	Discrete
Input Voltage (V)	30 20	2–4 3.7–4.2	24 20	18 22	0.05–0.3 0.4–0.8	20 9/40 20	0.03–0.09 0.2–0.7 1.45–1.8	2.2–3.2 2.6–3.8 3–4.2
Output Voltage (V)	21 8	1.8 3.7–4.2	12 8–10	12 8	0.5 1.2	5.25 3/15 32	1 1.3 1.6	7–18 0–1.8/15 3.2–4.2
Output Power	35.4 W	~18 mW	35 W	33 W	20 μW–4 mW	2.4 W/28 W	1 μW–24 mW	1.2 mW–386 mW
Max Switching Frequency (kHz)	40	147	100	80	200	100	250	10
Inductor (μH)	250	47	100	100	4.7	500	4.7	33
Output Capacitor (μF)	2200	1	220	220	1, 10, 100	47	2.2	22, 32, 100
Controller	PWM	PWM	PWM	PSM+PFM	PSM	PWM	PFM	VFPWM
Peaky Efficiency	90%	87.6%	92.1%	–	84.4%	88%	90.2%	92.5%
Adjusting Ability of Switching Frequency	No	No	Yes	No	No	No	Yes	Yes
Current Sensor Number	–	–	m+n	m	–	1	–	–
Operating Mode	CCM & DCM	DCM	CCM & DCM	CCM	DCM	CCM	DCM	DCM
Programmability	Medium	Low	Medium	Medium	Low	Medium	Low	High
Control Flexibility	Medium	Low	Medium	Medium	Low	Medium	Low	High
Extension Capability	Medium	Low	Medium	Medium	Low	Medium	Low	High
Usable in Low-Power Applications	No	Yes	No	No	Yes	No	Yes	Yes
Cost	Medium	High	Medium	Medium	High	Medium	High	Low

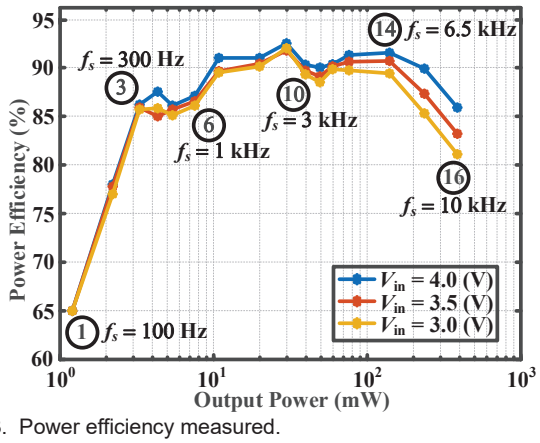

Fig. 13. Power efficiency measured.

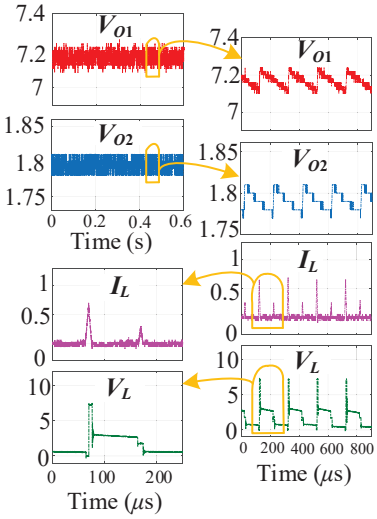

Fig. 14. Experimental results of the MISIMO converter outputs, inductor current, and the inductor's right-side voltage (V_L) for I_{o1} = 10 mA, I_{o2} = 5 mA, f_{s1} = f_{s2} = 5 kHz.

ZCS is examined; see Fig. 17. In the second test, a double current is drawn from the first output, and the microcontroller adjusts the duty cycle by the first, second, and fourth algorithms. Fig. 18 shows the waveform of the output voltages corresponding to each algorithm. In the third test, V_{ref} is changed for the second output, and as shown in Fig. 19(a), the controller performs satisfactorily, and V_{O2} perfectly tracks V_{ref2}. This test indicates that the proposed converter functions in three modes—i.e., buck, buck-boost, and boost modes. In the fourth test, the input voltage has a dc level with a sinusoidal peak-to-

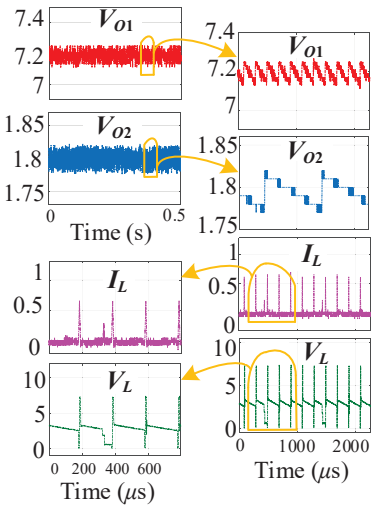

Fig. 15. Experimental results of the MISIMO converter outputs, inductor current, and the inductor's right-side voltage (V_L) for I_{o1} = 10 mA, I_{o2} = 1 mA, f_{s1} = 5 kHz, f_{s2} = 1 kHz.

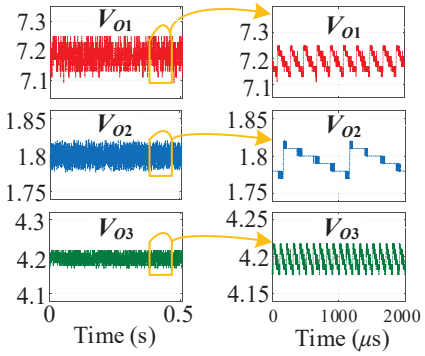

Fig. 16. Experimental results of the MISIMO converter outputs, inductor current, and the inductor's right-side voltage (V_L) for I_{o1} = 10 mA, I_{o2} = 1mA, I_{o3} = 40mA, f_{s1} = 5kHz, f_{s2} = 1kHz, and f_{s3} = 10 kHz.

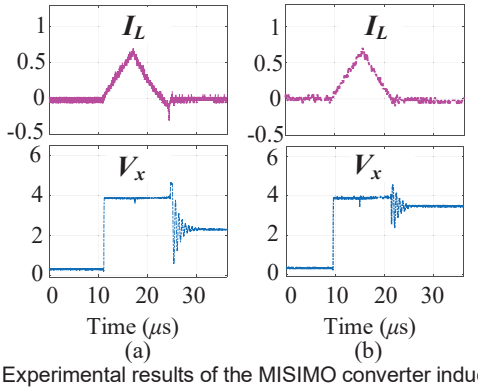

Fig. 17. Experimental results of the MISIMO converter inductor current and voltage to inductor's left side (V_x): (a) output switch is turned off too late and (b) output switch is turned off at the optimum time.

-peak amplitude of 0.9 V; as depicted in Fig. 19(b), the converter works suitably. In the fifth test, two inputs with voltages of 3.8 V and 3.2 V simultaneously charge the first and the second outputs with a constant frequency of 5 kHz; see Fig. 19(c).

VI. Conclusion

This article has proposed a new control methodology for the MISIMO converter. It has been implemented via a discrete design and has been able to have the capabilities that an analog controller can have by using a digital controller. The proposed

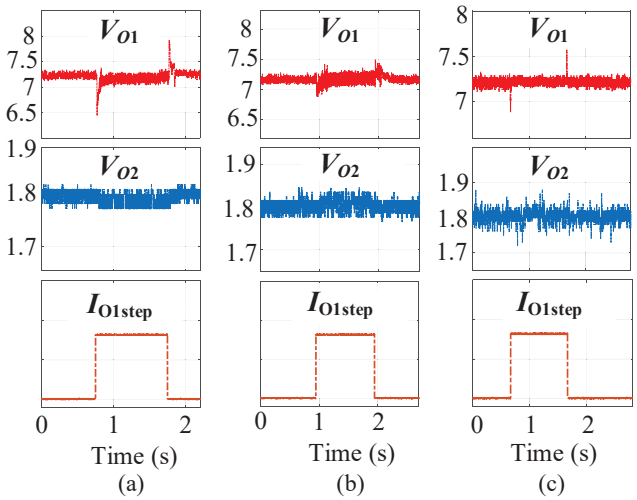

Fig. 18. Experimental results of the MISIMO converter outputs with load step using the: (a) first algorithm with time step = 10 ms, (b) second algorithm with time step = 1 ms, and (c) forth algorithm, in which the frequency is doubled during the doubling current.

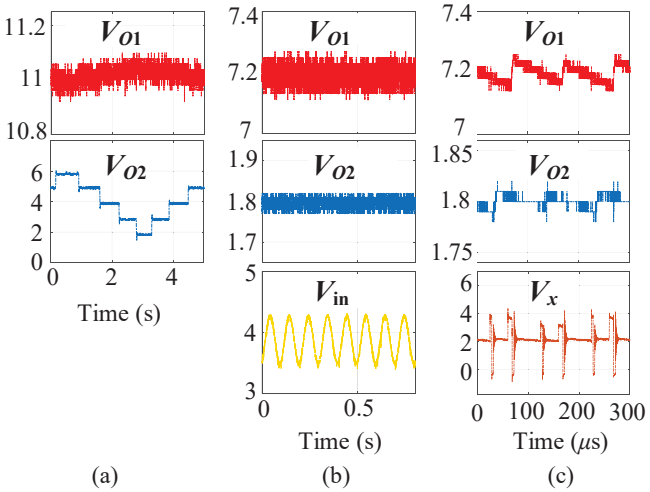

Fig. 19. Experimental results of the MISIMO converter outputs with: (a) variable V_{ref2}, (b) variable input, and (c) V_{in1} and V_{in2} activated.

approach has been employed in low-power, high-efficiency applications due to making the switching frequency low and using the microcontroller's timer/counters by the least amount of CPU turning on so that the microcontroller can be in the standby state most of the time. It has relatively high efficiency at a low-power range; it has 92.5% efficiency at 10 mW. Therefore, it is very economical. Due to the low-power outputs, the four digital algorithms implemented have operated in the DCM operation. Also, through the time-multiplexing control and variable-frequency PWM with the dead time intelligently employed, the outputs have been independently regulated with the capability of having different switching frequencies. Thus, cross-regulation has been reduced. The proposed algorithms have been simulated via MATLAB and examined practically.

Appendix

This converter can work at higher switching frequencies, for example, 1 MHz, 500 kHz, 100 kHz, etc. Suppose the microcontroller clock frequency is set at 10 MHz. If the converter operates at a switching frequency of 500 kHz, the number of the duty cycle steps will be 20 (10 MHz/500 kHz =

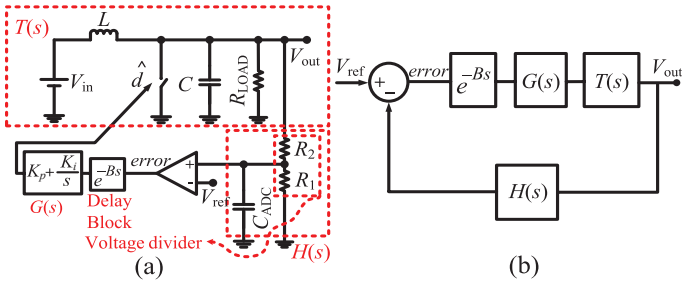

Fig. 20. DCM boost power stage: (a) Laplace model and (b) graph of the proposed controller.

20). If the same converter operates at a switching frequency of 5 kHz, the number of the steps equals 2000. Due to the low power consumption of the outputs, the microcontroller clock frequency and the switching frequency are impossible to be set to large values because the power consumption of the microcontroller and drivers is directly related to the frequency. The CV^2f equation (with f indicating either the clock or switching frequency) attests to that relation. The inductor and the capacitor values of each output must be selected so that the ripple values for each output are between 1% to 3% based on the voltage range and the load amount of each output; see (2) and (3). Fig. 20 shows the boost mode operating in DCM, and below is the derivation of its transfer function $T(s)$—it is the same for the buck and buck-boost modes, as detailed in [26].

$$B = 1 \text{ ms}, 10 \text{ ms}, \ldots, \qquad H(s) = \frac{R_1}{R_1 R_2 C\, s + R_1 + R_2}.$$

$$\frac{V_{\text{out}}}{V_{\text{ref}}} = \frac{e^{-Bs} G(s) T(s)}{1 + e^{-Bs} G(s) T(s) H(s)}, \text{ and } T(s) = \frac{V}{\hat{d}}\bigg|_{V_{\text{in}} = 0} = \frac{G_{d0}}{1 + \dfrac{s}{\omega_p}}.$$

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