A Time-Approximation Filter for Direct RF Transmitter

Shiyu Su, *Member, IEEE*, and Mike Shuo-Wei Chen, *Senior Member, IEEE*

***Abstract*— This article presents a highly programmable time-approximation filter (TAF) that can be embedded in a direct RF transmitter architecture. The proposed filter technique approximates the impulse response of a finite impulse response (FIR) filter with a modulated LO waveform, leading to an equivalent RF bandpass filtering during the frequency up-conversion process. The silicon prototype in 65-nm CMOS achieves an error vector magnitude (EVM) performance of −42 dB for a 20-MHz, 256-QAM signal and −43 dB for a 10-MHz, 1024-QAM signal at 2.4 GHz. Due to TAF, the out-of-band noise floor achieves −158 dBc/Hz at a 100-MHz frequency offset.**

***Index Terms*— Delta–sigma modulator, direct RF transmitter, hybrid digital-to-analog converter (DAC), time approximation, time interleaving, tunable filter.**

I. Introduction

TO MEET the growing demands of mobile access, increasing the bandwidth, spectrum efficiency, and flexibility have been the direction of the wireless revolution over the past few decades. CMOS technology scaling is the main driver of this process, as it can provide high-speed and low-cost devices that favor more digitally intensive designs. Because of the advancement of technology and architecture, a software-defined radio (SDR) transmitter (TX) has been used for its high bandwidth and reconfigurability that support multi-standard, multi-band transmission [1]. The key building block of an SDR TX is a digital-to-analog converter (DAC) that can convert the digital signal into an RF signal with sufficient output power in one step while meeting all the specifications, as shown in Fig. 1(a). However, covering signal bands from baseband to RF with a single wideband DAC is not as power efficient as a conventional heterodyne TX [2]–[5], which mainly consists of a baseband DAC followed by a reconstruction filter, a mixer, and a power amplifier (PA), as shown in Fig. 1(b).

To optimize the tradeoffs between the SDR TX and the conventional heterodyne TX, an RF-DAC-based direct RF TX architecture with the up-conversion function embedded in the DAC via digital mixing has been proposed and investigated, as shown in Fig. 1(c) [6]–[15]. There are two main advantages

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The authors are with the Ming Hsieh Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, CA 90089-0271 USA (e-mail: shiyusu@usc.edu).

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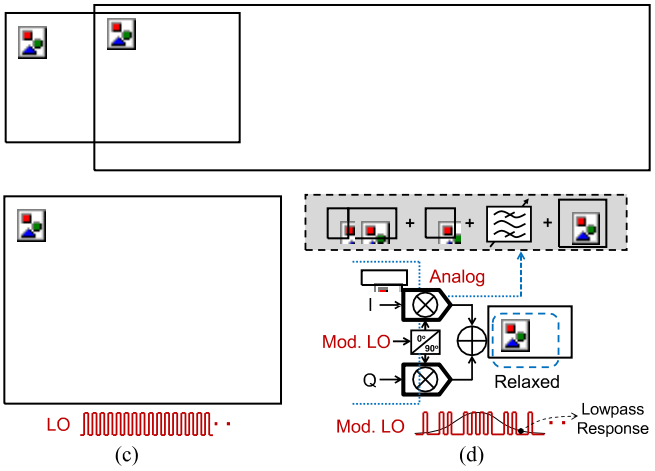


Fig. 1. TX architectures. (a) SDR TX. (b) Conventional heterodyne TX. (c) Direct RF TX. (d) Proposed direct RF TX with an embedded TAF.

of moving analog functions, such as up-conversion and gain control, into the digital domain: 1) digital operation provides power-efficient design with a small area and high reconfigurability and 2) merging the functions of a DAC and a mixer avoids the linearity degradation due to current-to-voltage and voltage-to-current conversions between the two blocks, which is one of the dominant sources of distortion [12].

Compared with conventional heterodyne TXs, one of the most challenging parts of a direct RF TX is suppressing the unwanted noise and spurious tones that are up-converted to the carrier frequency band due to the lack of baseband reconstruction filtering between the DAC and the mixer. A bandpass reconstruction filter in the RF domain is typically required to ensure a low out-of-band (OOB) noise floor that meets emission mask requirements, and the filter should be highly reconfigurable with nearly flat passband and sufficient stopband attenuation for wideband communications. In case of frequency-division duplexing (FDD) systems, additional noise attenuation on the receiver band may be needed to further suppress the TX leakage in order to avoid desensitizing the receiver when the TX and receiver are working concurrently. This low-noise-level requirement makes the design of the filter very challenging given a reasonable power and area budget. In addition, the frequency response and OOB noise attenuation requirements of the filter can vary depending on communication standards, making it difficult to be fully integrated. A variety of techniques, including noise shaping and semi-digital FIR filtering, have been explored in this area of research with design tradeoffs between flexibility, stopband attenuation, and design cost (power and area). More details on these techniques will be discussed in Section II-A.

In this work, we propose a time-approximation filter (TAF) technique for discrete-time (DT) data that embed a bandpass reconstruction filter during the up-conversion process of a direct RF TX, as shown in Fig. 1(d). We approximate the target filter's impulse response via the time-domain LO waveform (i.e., a modulated LO rather than a periodic pulse train), which effectively changes the DAC reconstruction waveform to achieve filtering [16]. Without loss of generality, low-pass TAF can also be embedded during digital-to-analog conversion of a heterodyne TX for baseband filtering. This TAF incurs low overhead due to minimal changes in the LO path and can be easily reconfigured due to the mostly digital operation. Pulsewidth/position modulation techniques have been used to improve the noise performance and power efficiency of digital PAs by approximating input signal in time domain, leading to signal distortion [17], [18]. The TAF only approximates the impulse response of an FIR filter instead of the input signal and hence avoids the signal distortion. A time-interleaved (TI) structure is used for the DAC implementation in order to deliver higher output power while sharpening the filter response of the TAF. In addition to the low OOB noise, a digitally intensive hybrid DAC architecture is applied to the direct RF TX to achieve high linearity and low in-band noise [19]–[21]. Note that the time-modulation concept for continuous-time (CT) data acquisition can be seen in [22]–[24], where the low-pass FIR filter coefficients are varied by modulating the integration time of the sampled signal in combination with the time-division multiplexing scheme. The rest of this article is organized as follows. The proposed TAF technique is introduced in Section II. Section III discusses an eight-way TI structure for the quadrature direct RF TX, and detailed circuit implementation and the experimental results are shown in Sections IV and V, respectively.

II. Proposed Time-Approximation Filter

In this section, we review the existing DAC and filter techniques used in TXs for OOB noise reduction followed by the introduction and analysis of the proposed TAF technique.

A. Overview of Noise Reduction Techniques in TX

Analog filters are widely used for noise and spur suppression in conventional heterodyne TXs. However, the cost and flexibility of the analog filter typically do not scale with technology. Due to the advancement of high-performance DAC, a direct RF TX based on digital filters, i.e., interpolators, and a wideband high-precision DAC become a competitive candidate with maximum relaxation of the reconstruction filter, which can even be avoided by simply relying on the selection capability of the output matching network if the DAC rate is sufficiently high [9], [10]. However, both high speed and high resolution incur penalties in the form of power consumption. In addition, the accuracy requirement of the DAC is very stringent for this type of architecture. Mismatches between DAC elements dramatically degrade the spectral purity, especially for high-speed designs. Sophisticated digital pre-distortion (DPD) or dynamic element matching (DEM) are typically needed to deal with element mismatches. Roverato *et al.* [25] used a noise-shaping technique to achieve a low noise floor at the specific band of interest. Similarly, high-order DEM is required to shape the DAC mismatch errors out of the band of interest. Depending on the applications, the shaped mismatch errors might degrade the noise performance at other passbands, e.g., the TX band. In [26] and [27], sinc^2 reconstruction filtering and intrinsic 20-dB/decade circuit noise attenuation are achieved using charge-based DAC structures. Due to the simplicity and low order of the filters, these structures have limited flexibility and OOB noise attenuation. A semi-digital FIR filter technique was first proposed in [28]; as a baseband filter, it achieves deep OOB noise suppression via precisely controlling the tap weighting of the FIR filter in the analog domain, while the delay of the signal replicas is done in the digital domain. Recently, this mixed-domain FIR technique has been widely used in direct RF TX for RF filtering by leveraging the higher Nyquist zones of the DT FIR filter [29]–[34]. As tap weighting of the FIR filter is stored in the amplitude domain, i.e., the size of a current source or a capacitor, both the accuracy and the flexibility of the filter are relatively limited.

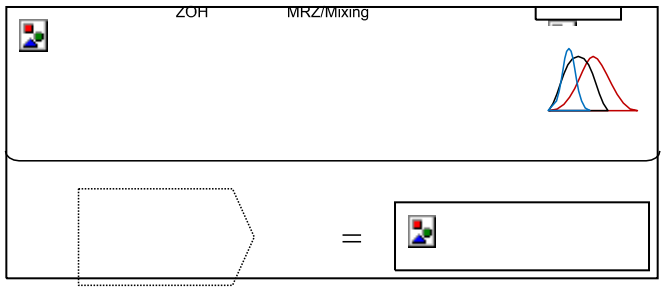


Fig. 2. Overview of DAC reconstructions.

B. Derivation of the Time-Approximation Filter

To overcome the abovementioned limitations, we propose to customize a DAC reconstruction waveform that is highly reconfigurable (digital-like), implementable, low-cost, and, more importantly, has high-frequency selectivity.

1) DAC Reconstruction Waveform: The digital-to-analog conversion process involves two steps: 1) computing the numerical value of the input digital signal in the DT domain ($x_d[n]$) and 2) converting the DT signal into CT via convolving it with the impulse response of a reconstruction waveform ($h(t)$), as shown in Fig. 2. This operation is described by the equation

$$y_h(t) = x_c(t) * h(t) = \sum_{n=-\infty}^{+\infty} x_c(nT_s)h(t - nT_s). \quad (1)$$

Ideally, a sinc-shape impulse response provides perfect reconstruction, but it is not practical to implement due to the infinitely long impulse response. Non-return zero (NRZ) is one of the most commonly used zero-order-hold (ZOH) reconstruction filters, which holds the data for the whole sampling period, i.e., T_s. Each channel of a TI structure holds the data longer than one sampling period, which leads to a lower filter corner. On the other hand, the data duration of a return-zero (RZ)

reconstruction waveform is less than one sampling period, which leads to higher corner frequency with less signal attenuation in the second Nyquist zone [35]. Similarly, mixing and multiple-return-zero (MRZ) reconstructions manipulate the signal gain in higher Nyquist zones to make these zones worth using [12], [36]. Luschas *et al.* [6] proposed a reconstruction filter with sine impulse response using a sinusoidal LO signal. Note that all the aforementioned reconstruction filters only provide first-order filtering, which is typically insufficient for noise attenuation. In addition, they lack flexibility. These concerns can be addressed using a generic FIR reconstruction waveform with the following response:

$$h_{FIR}(t) = \sum_{m=0}^{M-1} \frac{1}{T_{tap}} \left[u\left(t - mT_{tap}\right) - u\left(t - (m+1)T_{tap}\right) \right] \quad (2)$$

where M is the number of FIR filter taps, T_{tap} is the tap delay, and a_m is the filter coefficient of the mth tap. The largest filter coefficient is normalized to unity.

Compared to the conventional way of implementing a semi-digital FIR filter (i.e., replicate, delay, weight, and sum the data), there are two main advantages of modulating the reconstruction waveform for each sample with $h_{FIR}(t)$. First, T_{tap} can be independent of the data rate (i.e., F_s), which provides one more degree of freedom for system optimization. Second, a single DAC can be used to synthesize $h_{FIR}(t)$, instead of replicating DACs to represent different taps of $h_{FIR}(t)$, which leads to a more robust impulse response over the mismatch between DACs. More detailed comparison and analysis is provided in Section III-B.

2) Time Approximation of Impulse Response: In reality, synthesizing a reconstruction waveform with varying amplitude is inefficient, as it requires an extra high-precision DAC for each element of the main DAC. In the proposed TAF, we approximate the amplitude-modulated FIR impulse response (i.e., constant time duration but varying amplitude) with a time-modulated waveform (i.e., constant amplitude but varying time duration). In this way, a conventional DAC used for ZOH reconstruction is sufficient to synthesize the desired reconstruction waveform, which leads to low-cost implementation. Since the time-modulated waveform is digital-like—i.e., toggling between two voltage levels—the proposed TAF avoids the matching between multiple DACs and is highly reconfigurable.

Fig. 3 shows an example of an eight-tap TAF. The original DT impulse response of the target filter is first calculated as the reference. The CT version of the impulse response is generated from the DT impulse response via ZOH, as described in (2). Based on (2) and keeping the corresponding pulses with the same area while maintaining a constant amplitude of the pulses (see Fig. 3), the impulse response after time approximation will be

$$h_{TAF}(t) = \sum_{m=0}^{M-1} \frac{1}{T_{tap}} \left[u\left(t - \frac{(2m+1-a_m)T_{tap}}{2}\right) - u\left(t - \frac{(2m+1+a_m)T_{tap}}{2}\right) \right] \quad (3)$$

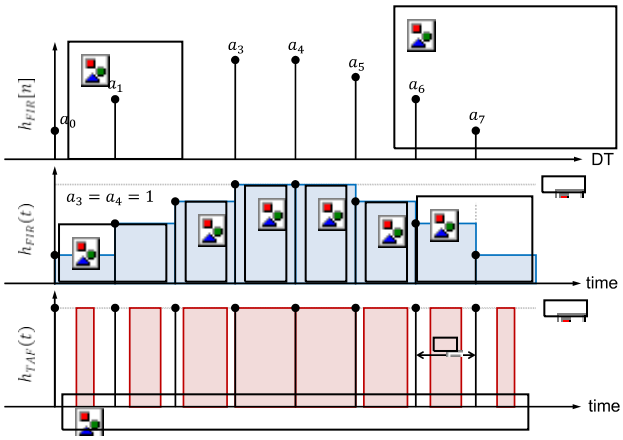


Fig. 3. Impulse responses of conventional FIR filters and associated TAF.

where $M = 8$ and $T_{tap} = 1$ ns in this example. By taking the Fourier transform of (2) and (3), the frequency responses of the conventional FIR filter and the TAF are obtained as

$$H_{FIR}(f) = e^{-j\pi T_{tap} f} \sum_{m=0}^{M-1} a_m \mathrm{sinc}\left(T_{tap} f\right) e^{-j2\pi m T_{tap} f} \quad (4)$$

and

$$H_{TAF}(f) = e^{-j\pi T_{tap} f} \sum_{m=0}^{M-1} a_m \mathrm{sinc}\left(a_m T_{tap} f\right) e^{-j2\pi m T_{tap} f}. \quad (5)$$

The phase terms of (4) and (5) are equal, as we intentionally align the center of the pulses of h_{FIR} and h_{TAF} during the approximation.

From (4) and (5), one can observe a magnitude mismatch between the conventional FIR filter and TAF responses over frequency, as shown in Fig. 4(a), with the eight-tap FIR filter response. This is mainly because of the varying pulse duration of h_{TAF} taps, i.e., $a_m T_{tap}$ from (3), which results in different sinc modulation between H_{FIR} and H_{TAF}. Considering the worst case, by comparing the shortest pulse duration of h_{TAF} (i.e., $a_{min}T_{tap}$) and the uniform pulse duration of h_{FIR} (i.e., T_{tap}) and by referring to (5), we can estimate the boundary of this magnitude mismatch over frequency to the first order as

$$G_{mismatch} = 20 \log_{10} \frac{\mathrm{sinc}\left(a_{min} T_{tap} f\right)}{\mathrm{sinc}\left(T_{tap} f\right)} \quad (6)$$

According to (6), impulse response with larger a_{min} provides less $G_{mismatch}$. Using the same eight-tap FIR filter response, the magnitude mismatch between the conventional FIR filter and the TAF is presented in Fig. 4(a). In a real implementation, there is an additional quantization effect on the TAF's coefficient in time. Assuming that one T_{tap} is divided into N uniform time slots, it is equivalent to using $\log_2(N)$ bits for representing the filter coefficient. The time quantization effect on H_{TAF} can be estimated by quantizing a_m in (5). In this work, N is equal to 8 for each tap of the TAF to guarantee less than 3-dB approximation error due to the time quantization. The approximation error is defined as the magnitude difference between the TAF and the desire filter's frequency responses. Note that the negative filter coefficient is not achievable by the TAF implemented in this prototype. Depending on the target

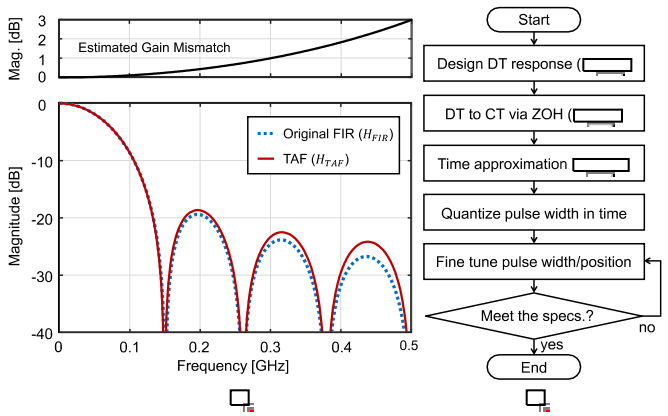


Fig. 4. (a) Frequency responses of conventional FIR filter and TAF. (b) Proposed design flow of TAF impulse response.

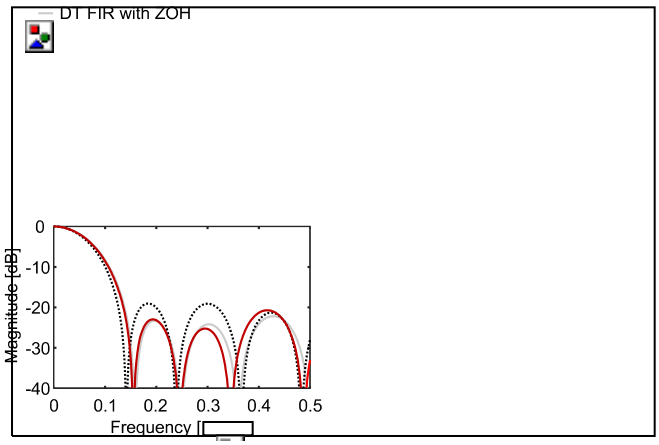


Fig. 5. Impulse and frequency response comparison for an eight-tap and a four-tap TAFs with and without fine-tuning scheme.

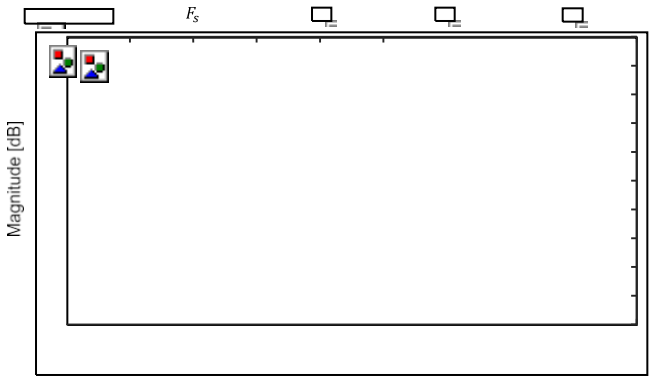


Fig. 6. Frequency response of an eight-tap TAF with a wide span.

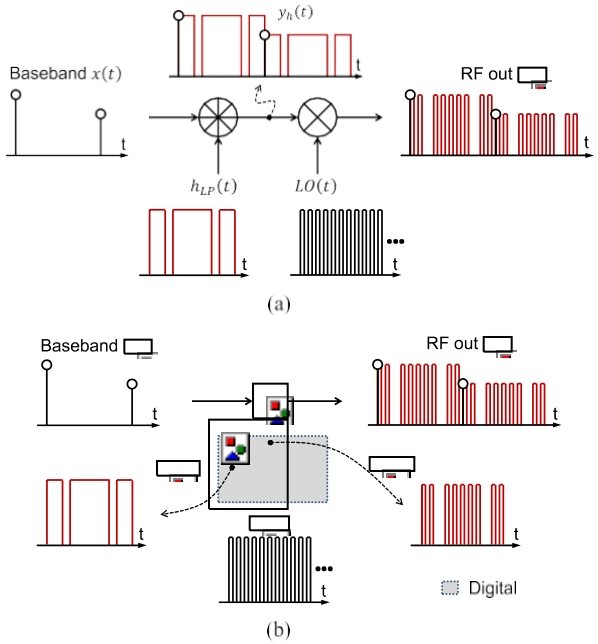


Fig. 7. (a) Low-pass TAF followed by a mixer with a uniform LO. (b) Embedded bandpass TAF during up-conversion via LO modulation.

FIR filter, a TAF might lead to smaller output power/efficiency than the peak (i.e., NRZ ZOH). The output power/efficiency reduction is proportional to the energy that is gated off to present the fractional filter coefficients, assuming that the largest coefficient is normalized to unity. When designing the TAF response, the tradeoff between filter performance and output power/efficiency needs to be considered.

A complete design flow of the TAF response waveform is shown in Fig. 4(b). As aforementioned, the DT FIR filter is first designed based on the system requirements and then converted into CT for time approximation. According to the fastest available clock in the system, the TAF's coefficients are quantized in time by snapping the transitions of $h_{\mathrm{TAF}}(t)$ to the rising edges of the clock. After coefficient quantization, the frequency response of TAF might deviate considerably from the original one. To enhance the filter approximation at the presence of quantization error, we proposed to fine tune the pulse position and width numerically for each tap of the TAF response via adjusting the edges around their original locations, as shown in Fig. 5. The frequency responses of the fine-tuned TAFs align closer to that of the original FIR filter for meeting the approximation error specification. In addition to the close-in noise reduction, fine-tuning can also optimize the TAF response for wideband noise attenuation. Fig. 6 shows the frequency response of an eight-tap TAF with a wide span that covers four sampling replicas. High-frequency humps due to the time-approximation error are suppressed by properly tuning the TAF's impulse response. Other than the approximation error, the TAF performance is also limited by the sampling period (i.e., T_s). For a single-channel structure, the duration of a TAF's impulse response cannot extend over one sampling period. In this work, a TI TAF is proposed to tackle this limitation. More details are elaborated in Section III.

C. Low-Pass-to-Bandpass TAF

A low-pass TAF can be used in a heterodyne TX for baseband reconstruction. On the other hand, applying TAF in a direct RF TX requires creating a bandpass filter response centered at LO frequency. Conventionally, this can be achieved by mixing the low-passed baseband data with a uniform LO signal ($\mathrm{sgn}[\sin(2\pi f_{\mathrm{LO}}t)]$), as shown in Fig. 7(a). According to (1) and assuming

$$\mathrm{LO}(t) = \mathrm{LO}(t - nT_s) \tag{7}$$

the following associative property can be proved:

$$y(t) = \underbrace{[x(t) * h_{\mathrm{LP}}(t)]}_{y_h(t)} \cdot \mathrm{LO}(t) = x(t) * \underbrace{[h_{\mathrm{LP}}(t) \cdot \mathrm{LO}(t)]}_{h_{\mathrm{BP}}(t)}. \quad (8)$$

Based on (8), we combine the baseband TAF pattern generation and the frequency up-conversion into one step to reduce the number of blocks along the signal path, as shown in Fig. 7(b). Note that this combined LO modulation is all done in a digital domain with negligible overhead, which also makes the filter, and hence the direct RF TX, highly reconfigurable. In this work, the carrier period ($1/f_{\mathrm{LO}}$) is chosen to be the time resolution of the LO modulation (bandpass TAF) for lower implementation complexity, which allows a simple gating operation on top of the original uniform LO. Different from the technique used in [17] and [18] that modulates the pulsewidth and position of the input signal, this gating operation uses a time-window pattern to determine whether a particular LO cycle should be preserved or gated off since we only approximate the filter response instead of input signal. The time-window pattern is generated based on the impulse response of the low-pass TAF, which can be precomputed and programmed in an on-chip memory. The stored time-window pattern is then serialized into a single-bit stream and used for LO modulation. This way of synthesizing a bandpass TAF introduces minimum additive noise to the LO path. In addition, there is no timing skew between each tap of the TAF, as its timing is only determined by the zero crossing of LO. More implementation details on LO modulation will be discussed in Section IV.

III. Time-Interleaved TAF

In this section, we discuss a TI DAC architecture [16] and the advantages of combining it with TAF.

A. TX Performance Enhancement

In general, there are several advantages of using a TI DAC over the conventional single-channel DAC. First, for an N-way TI DAC, each channel operates N times slower. The slow data rate for each channel relaxes the timing constraint for both the digital circuitry and the clock distribution. Second, the effective number of bits of a Nyquist DAC increases by $\log_4 N$ or the signal-to-noise ratio increases by N times for an N-way TI structure [37]. Assuming that each channel delivers the same amount of output power as the single-channel DAC, the TI DAC provides higher output power as each channel holds the data sample for a longer period. In this way, the gain requirement of the following analog PA is relaxed.

By combining an NRZ TI DAC architecture with TAF, the time duration of TAF impulse response can be extended beyond one sampling period due to the longer data duration of each TI channel. The longer filter impulse response allows higher stopband attenuation and lower possible corner frequency without sacrificing filter sharpness (see Fig. 8). In addition, given a fixed time resolution for modulating the LO, longer impulse response due to TI also provides more time grids for better time approximation, i.e., higher effective resolution for representing TAF's coefficients.

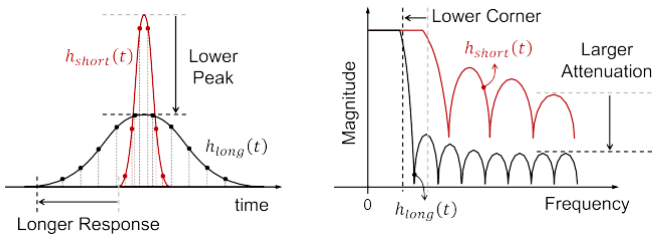


Fig. 8. Long versus short impulse responses.

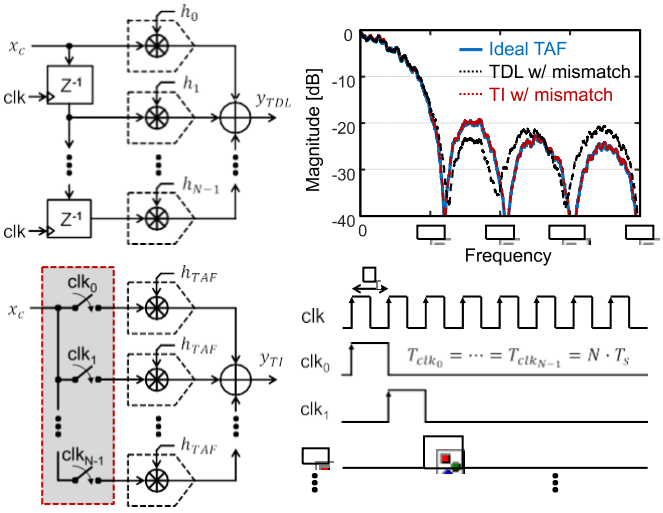


Fig. 9. Conventional TDL versus the proposed TI structures of TAF.

B. Channel Mismatch Effect

Fig. 9 shows two possible ways of extending TAF's impulse response, including the conventional tapped delay line (TDL) and the proposed TI structures. For a fair comparison, the number of TAF's taps and the number of parallel channels are both set to N and the tap delay T_{tap} is set to the sampling period T_s (period of the clock for each TI channel equals $N \cdot T_s$) so that the two structures yield the same filter response, as in

$$h_{\mathrm{TAF}}(t) = \sum_{m=0}^{N-1} h_m(t - mT_s) = \sum_{m=0}^{N-1} p_m(t) \quad (9)$$

where h_m presents the $m$thtap of the TAF, referring to (3), and p_m is the delayed h_m. Note that, for a TI architecture, the number of TAF's taps and the tap delays are relatively independent of the number of TI channels and the data rate. This property provides extra degrees of freedom for TAF design. So far, we assume that all the sub-channel DACs are identical. However, in reality, there is a gain mismatch between channels. We model the mismatch as the weighting of the mth sub-channel DAC, α_m, as in

$$\begin{cases} y_{\mathrm{TDL}}(t) = \sum_{n=0}^{N-1} \sum_{k=-\infty}^{+\infty} x_c[(Nk+n)T_s] * \sum_{m=0}^{N-1} \alpha_m p_m(t) \\ y_{\mathrm{TI}}(t) = \sum_{n=0}^{N-1} \alpha_n \sum_{k=-\infty}^{+\infty} x_c[(Nk+n)T_s] * \sum_{m=0}^{N-1} p_m(t). \end{cases} \quad (10)$$

From (10), the mismatched sub-channel weightings (α_m) change the TAF impulse response via scaling its tap coefficients when using the TDL approach. For the TI structure,

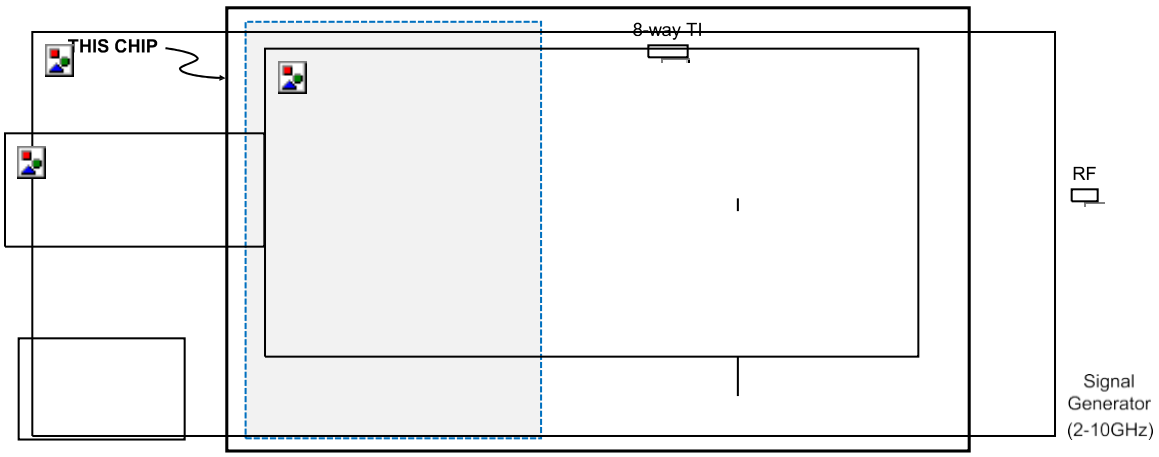


Fig. 10. System block diagram.

the sub-channel mismatch introduces a global gain to the filter response without changing its shape, i.e., the relative relationship between filter taps. Using an eight-tap TAF as an example, simulated frequency responses of the filter with different implementations are shown in Fig. 9. In this simulation, channel mismatch is randomly generated with a standard deviation of 10%. It can be observed that notches of the filter implemented with TDL deviate from that of the ideal TAF response due to the channel mismatch, while the same amount of mismatch has a negligible impact on the frequency response of the TAF with a TI structure.

IV. Circuit Implementation

A. System Block Diagram

Fig. 10 shows a block diagram of the proposed direct RF TX architecture. To derive time-approximation filtering, a modulated LO waveform is created by repetitively gating the uniform LO with a certain time-window pattern to determine whether a particular LO cycle should be preserved or gated off. The time-window pattern is stored in on-chip memory and selected by clocks divided from the uniform LO with proper phases to generate the modulated LO, and this modulated LO is used to up-convert the baseband signal while simultaneously achieving bandpass filtering. The input I/Q baseband signal is upsampled and interpolated off-chip. The test data stream is then programmed in on-chip SRAMs and read by the DACs. Two DAC modes are implemented in this prototype: a 7-bit Nyquist mode and a 16-bit hybrid mode [19]–[21] for achieving a low in-band noise floor via delta–sigma modulation of the input LSBs. For wideband operation and a low OOB noise floor, the DAC operates in the Nyquist mode. In hybrid mode, the DAC takes up to 16-bit digital input and compresses this into 7-bit output. The high in-band dynamic range allows a high-order modulation scheme in the direct RF TX.

Fig. 11 shows the hybrid DAC structure we used in this prototype. The 16-bit digital input data are split into 4-bit MSB and 12-bit LSB. The 4-bit MSB is converted into a thermometer-coded data for good linearity and used to control a unary current-steering DAC array. The 12-bit LSB is compressed to 4 bits by a third-order low-pass DSM and

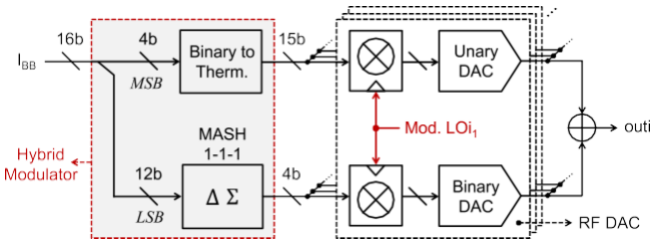


Fig. 11. Hybrid DAC (I Channel).

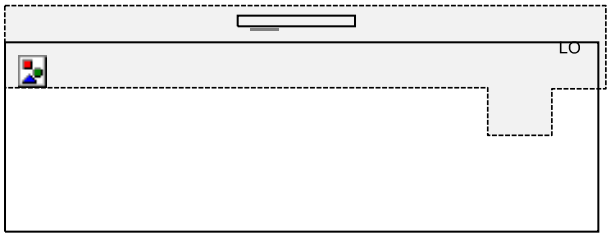


Fig. 12. LO modulator.

used to control a binary current-steering DAC array. The DSM is an unrolled 1-1-1 MASH architecture for high-speed operation.

B. LO Modulator

The LO modulation for TAF is achieved using the high-speed serializer shown in Fig. 12. This serializer mainly consists of memory cells (i.e., DFFs), 2-to-1 MUXs, and a mixing latch. The 64 DFFs are used to store the TAF response patterns and are fully programmable. The stored patterns are read out in sequence via an array of 2-to-1 MUXs that are controlled by multi-frequency and multi-phase clocks. These clocks are divided from the uniform LO signal and trimmed to proper phases via phase detectors and rotators. Finally, the mixing latch clocked by LO is used to synchronize and chop the TAF pattern to generate the desired LO waveform. With this serializer-based LO modulator, only the latch driver and the mixing latch are inserted into the LO path, leading to negligible additive noise in the modulated LO.

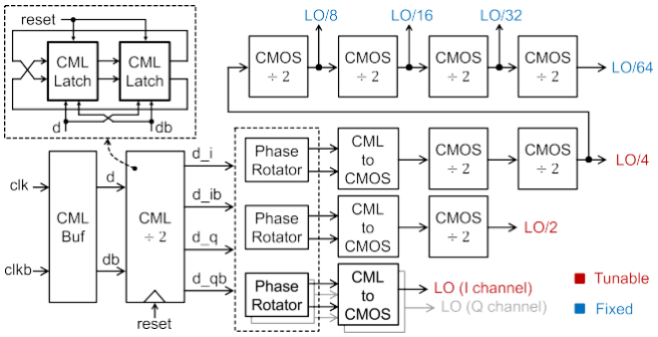


Fig. 13. Clock generator.

C. Clock Generator

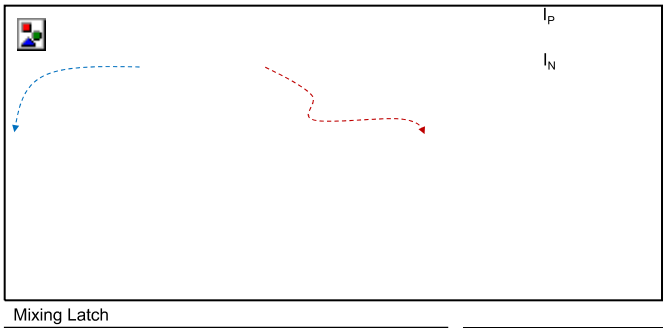
The clock generator used to create multi-frequency multi-phase clocks is shown in Fig. 13. The input clock (2–10 GHz) is sent from the off-chip, buffered by a CML driver and divided into four different phases via a CML divider. The four-phase clocks are then used to interpolate finer clock phases for serializer clock trimming and I/Q timing alignment. After the phase interpolator or phase rotator, the CML signals are amplified to rail-to-rail swing. A set of CMOS frequency dividers are used to generate different clock frequencies. For clocks slower than LO/4, we fix the phases to save the power from additional phase rotators.

D. Mixing Latch

Data synchronization is done using a three-stage latch chain to minimize the input data dependence. The first two latches shown in Fig. 14 form a master–slave DFF that converts the single-end digital input data into a differential and stores it in the first half of the modulated LO period for the mixing latch [35]. The mixing latch applied prior to the DAC element is controlled by the modulated LO for both data synchronization and frequency up-conversion. Multiple operation modes of the mixing latch are used to experiment with different TX configurations for the purpose of chip characterization (see Fig. 14). In mode 1, the mixing function is turned off via S_{MIX} for baseband operation to evaluate the DAC performance. Multiple return-to-zero and chopping operations are implemented to effectively AND and XOR the input signal with LO and achieve different types of mixing in modes 2 and 3, respectively, for comparing the tradeoff between output power and linearity.

E. Output Driver

To maintain an intrinsic linear operation for high spectral efficiency and wide bandwidth, we used a current-steering cell as the DAC element and final output driver (see Fig. 15). Two cascode devices are inserted at the output to increase the DAC output impedance and protect the core switching devices, as the DAC output is connected to the 2.5-V supply for a larger output swing. With a tunable off-chip reference current and an on-chip digitally controlled current bias, tail current of MSB current-steering cell ranged from 0.3 to 1.2 mA. The DAC elements are sized to be relatively large for delivering high output current with sufficient DAC output impedance. Each



Mode	Function
1	Latch
2	Latch+AND
3	Latch+XOR

Fig. 14. Three-stage mixing latch.

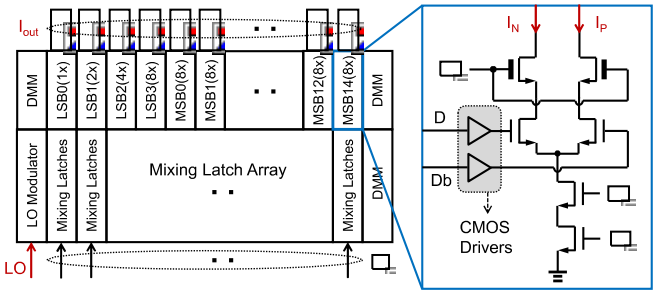


Fig. 15. Floor plan and schematic of current-steering cell.

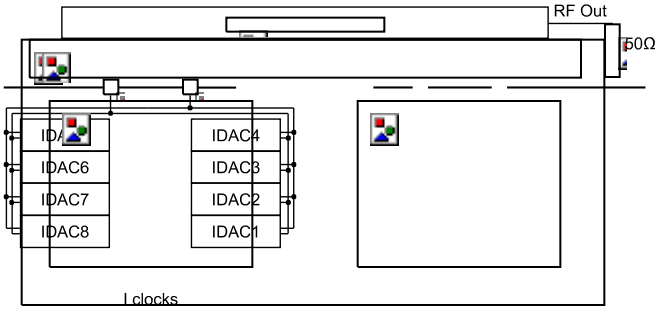


Fig. 16. Floor plan of TI channels.

mixing latch is well-aligned with the corresponding current-steering cell to minimize the timing mismatch. A replica of mixing latch is used as the last stage of the LO modulator. For an eight-way interleaved quadrature structure, there are total 16 current arrays, as shown in Fig. 16. Data and clocks for I and Q DACs are routed together for minimal time skew. Each channel is laid close to its subsequent channels to minimize the spurs due to channel mismatches. The DAC outputs are loaded with inductors. Power combiner for I and Q signals is off-chip with 2:1 impedance transformation ratio.

V. Measurement Results

The silicon prototype is fabricated in 65-nm CMOS technology with a total area of 6.25 mm^2. Fig. 17 shows the die micrograph.

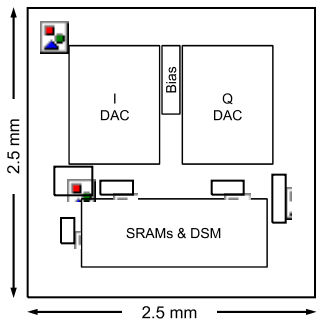


Fig. 17. Die micrograph.

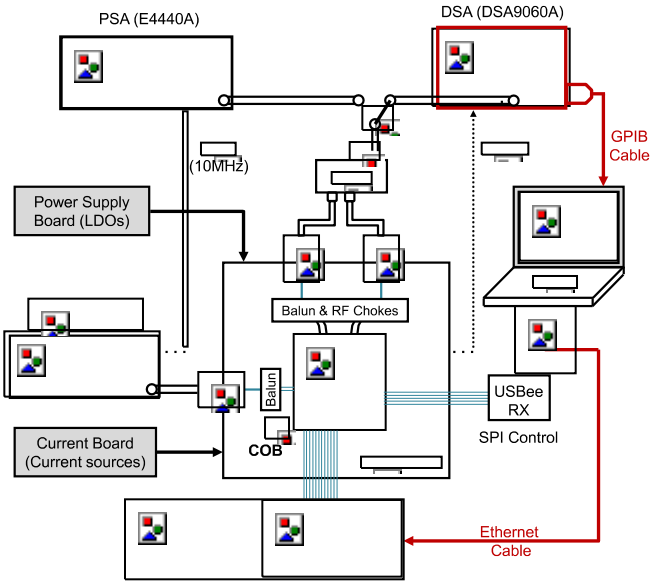


Fig. 18. Test setup.

The prototype chip is directly bonded to the PCB for less bond-wire inductance. The measurement setup is shown in Fig. 18. The power supplies are all generated by LDOs on a customized voltage board. Similarly, bias currents for current-steering cells and the clock generator are provided using a customized current board. The 2–10-GHz clock is synthesized with an E8251A signal generator converted from single end to differential clocks via an LTCC packed wideband balun and sent to the chip. To support long test pattern length, an Agilent 16902A pattern generation module is used for SRAM writing in and sequential control. The differential I/Q output is open-drain and terminated with a 50-Ω load (i.e., the equipment) via power combiners, which includes SMD RF chokes, baluns, and a discrete hybrid. A spectrum analyzer is used to monitor the RF output spectrum and perform two-tone and ACLR tests, while the error vector magnitude (EVM) test is done via a wideband oscilloscope and vector signal analysis tool.

To decouple the non-idealities of mixing and TAF operations from the digital-to-analog conversion, we first characterize the TI DACs at baseband by reconfiguring the mixing latch into a conventional latch that has no mixing function embedded. Fig. 19 shows the baseband two-tone spectrum of the I/Q-DAC at 625 MS/s, which corresponds to a 5-GHz effective LO in the RF mode, i.e., the clock of the latch is a

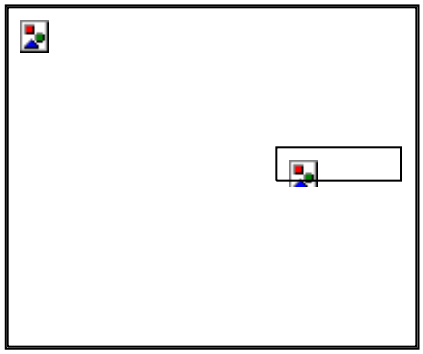


Fig. 19. Measured two-tone spectrum of I/Q-DAC at baseband.

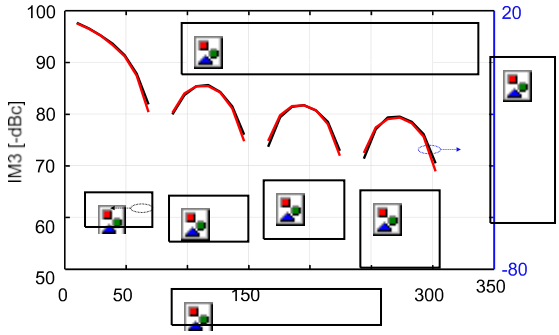


Fig. 20. Measured IM3 and signal power at baseband with F_s = 625 MS/s.

5-GHz LO signal divided from a 10-GHz external clock and it is further divided down for data clocking. The IM3 measures −64.5 dBc at 68 MHz. The measured IM3 over different signal frequencies and the corresponding signal power are shown in Fig. 20. The average value is around 60 dB over the Nyquist band. The first notch of the sinc located at 1/8 data rate (F_s) is due to the NRZ TI structure.

When the mixing switch of the mixing latch is turned on (see Fig. 14), the TX operates in the RF mode. With continuous-wave tests, the peak output power of the TX measures 23 dBm at 0.9 GHz and 15 dBm at 2.4 GHz, with the drain efficiency of 20.4% and 3.5%, respectively. The power and efficiency drop from the peak is mainly due to impedance mismatch over frequency, which can be resolved via impedance tuning [38]. Note that a class-A driver is used in this prototype for its intrinsic linearity by trading off the power efficiency. Depending on system specifications, switching-mode drivers in combination of DPD can be used to achieve high power efficiency with decent linearity and noise performance [32], [33], [38], [39]. Fig. 21(a) shows the spectrum and the corresponding constellation plot of a 20-MHz, 256-QAM signal at 2.4 GHz. Limited by the size of on-chip SRAM, several rounds of data capture are performed to construct the constellations. The EVM measures −42 dB. Similarly, Fig. 21(b) shows the spectrum and the constellation plot of a 10-MHz, 1024-QAM signal. The EVM measures −43 dB. To validate the TX operation with a different LO frequency, Fig. 22 shows the measured constellations of a 40- and 20-MHz 64 QAM signal at 4.4 GHz; the EVM measures −35 and −36 dB, respectively. All the measurement data are collected without applying any DPD. The TX intrinsically achieves high linearity via a current-steering operation.

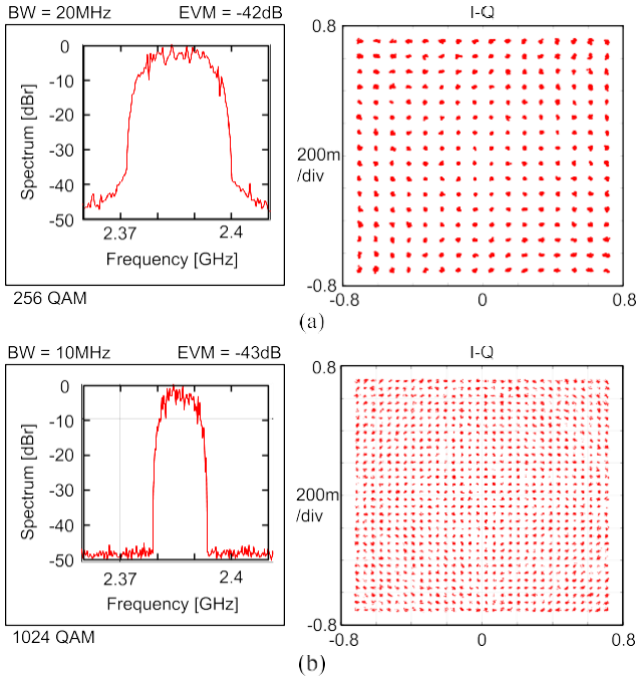


Fig. 21. Measured spectra and constellation plots for (a) 256-QAM signal and (b) 1024-QAM signal at 2.4 GHz.

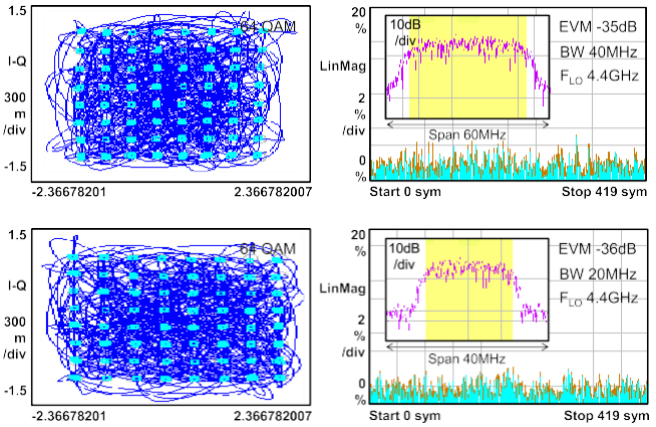


Fig. 22. Measured constellation plots for 64-QAM signals at 4.4 GHz.

Fig. 23(a) shows the impulse responses of filters that are used to prove the effectiveness and flexibility of TAF. The associated frequency responses of the filters and the noise transfer function (NTF) of the DSM used in the hybrid DAC are shown in Fig. 23(b). An LPF1 configuration corresponds to the NRZ TI structure. It potentially allows low corner frequency of the filter but with limited passband flatness and stopband attenuation, which can be improved by the LPF2 configuration. An LPF3 configuration provides more noise attenuation at a specific band of interest by a tradeoff in the attenuation at other bands. The different TAF impulse responses are experimented with to prove the filter's reconfigurability. The measured Nyquist-mode NSD at 2.4 GHz is plotted in Fig. 23(c). Compared to a conventional RZ-TI direct RF TX, the proposed TAF achieves 20–25-dB more OOB noise attenuation over the Nyquist band (using an LPF1/LPF2 configuration). The lowest NSD measures −158 dBc/Hz with a bandwidth of 5 MHz and the average NSD over a 20-MHz bandwidth measures −155 dBc/Hz at −100-MHz offset from the carrier frequency (LPF3). The measured NSD in the hybrid DAC mode is shown in Fig. 23(d). A lower close-in noise floor is achieved as the DAC resolution is increased from 7 to 16 bits. The far-out OOB noise shaped by the DSM is suppressed to be less than +20 dBc/Hz due to the TAF.

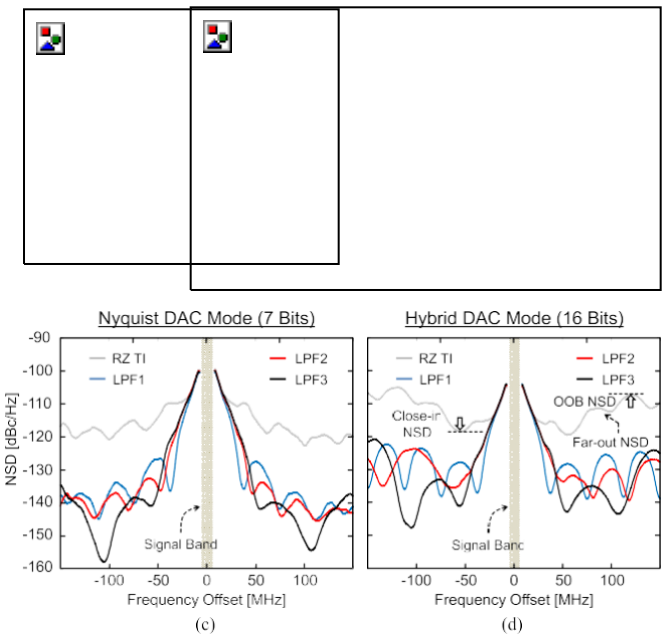


Fig. 23. Measured NSD at 2.4 GHz.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ARTS

		This work	[13] ISSCC'17	[14] JSSC'18	[25] JSSC'17		
Architecture		**Digital IQ**	Digital Polar	Digital IQ	Digital IQ	Digital IQ	Digital IQ
Matching Network		**Off-chip**	On-chip	Off-chip	On-chip	Off-chip	Off-chip
Process	[nm]	**65**	28	40	28	28	65
Active Area	[mm^2]	**1.68**	1.3	0.21	0.82	0.22	0.35
Supply	[V]	**1/2.5**	1/1.1/1.3	1.1/2	0.9/1.5	0.9/1.1	1.2
Resolution	[bits]	**7-16**	15	9	10	12	11
F_{LO} Range	[GHz]	**0.9-5.2**	0.7-2.8	0.9-3.1	0.85-0.9	0.9/2.4	2.4-2.7
F_s Range	[MS/s]	**112-625**	N/A-2800	250-750	850-900	500	1200-1350
P_{sat} Range	[dBm]	**2-23**	6-12*	5-9.2	6	3.5/3.5	2*
F_{LO}	[GHz]	**2.4**	2.54	3	0.9	2.4	2.5
P_{out}	[dBm]	**11**	6	1	3	-3.5	2.6
η_{system}	[%]	**1.05**	2.9	4.8	1.3	1.8	0.72
Bandwidth	[MHz]	**20**	40	57	20	20	17
EVM	[dB]	**-42**	-28.9	-30	N/A	-36	-32.4
ACLR1	[dB]	**-42**	-41.9	-44	-61	-47	-42.8
ACLR2	[dB]	**-55.3**	-52.9	N/A	N/A	-59	-46.2
Noise Floor @Offset Freq.	[dBc/Hz] [MHz]	**-155/-158** -100/+100**	-151/-152 -120/+120	-136/-140 -170/+170	-158*** -30/+30	-159*** -45/+45	-143/-145 -500/+500
Reconstruction Filter		**TAF**	Sinc	Sinc$^{1-3}$	Noise Shaping	Sinc^2	2-tap FIR
Modulation		**SC 256 QAM**	2xLTE20 64 QAM	SC 64 QAM	LTE /	Multi-tone 64 QAM	OFDM 64 QAM

* Measured average output power
** Measured NSD over a 5-MHz bandwidth.
*** Measured from upper or lower side is not specified
P_{sat} – Peak output power.
P_{out} – Average output power.
N/A – Not available.

Table I summarizes the performance of this work and compares it with a few state-of-the-art digital direct RF TXs.

It shows that this work operates over a wide LO range with outstanding EVM and ACLR among the medium/low output power, high-linearity direct RF TXs. Without using analog filters or increasing the data rate, a −158-dBc/Hz OOB NSD is achieved by digitally modulating the LO, i.e., TAF. Note that as the TAF impulse response is fully programmable, it provides better flexibility than the other reconstruction schemes and potentially facilitates FDD operation.

VI. Conclusion

This article demonstrated a highly flexible direct RF TX with a programmable TAF embedded in the up-conversion process that approximates an FIR filter impulse response in time. This TAF incurs low implementation overhead due to minimal changes in the LO pathway and the mostly digital operation. A TI structure is applied to further increase the output power and to enhance the TAF performance. As a generic mixed-signal technique, the application of TAF is not limited by the TX architecture and the type of output driver; it potentially can be used in digital PAs (classes D, E, F, and so on) to achieve high power, high efficiency, and low OOB noise.

References

[1] J. Mitola, "The software radio architecture," *IEEE Commun. Mag.*, vol. 33, no. 5, pp. 26–38, May 1995.

[2] V. Giannini, M. Ingels, T. Sano, B. Debaillie, J. Borremans, and J. Craninckx, "A multiband LTE SAW-less modulator with −160 dBc/Hz RX-band noise in 40 nm LP CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 374–376.

[3] M. Ingels. Y. Furuta, X. Zhang, S. Cha, and J. Craninckx, "A multiband 40 nm CMOS LTE SAW-less modulator with −60 dBc C-IM3," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 338–339.

[4] Y.-H. Chen, N. Fong, B. Xu, and C. Wang, "An LTE SAW-less transmitter using 33% duty-cycle LO signals for harmonic suppression," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[5] V. Bhagavatula *et al.*, "A SAW-less reconfigurable multimode transmitter with a voltage-mode harmonic-reject mixer in 14 nm FinFET CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 220–221.

[6] S. Luschas, R. Schreier, and H.-S. Lee, "Radio frequency digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1462–1467, Sep. 2004.

[7] P. Eloranta *et al.*, "A multimode transmitter in 0.13 μm CMOS using direct-digital RF modulator," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007.

[8] J. Mehta *et al.*, "A 0.8 mm^2 all-digital SAW-less polar transmitter in 65 nm EDGE SoC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 58–59.

[9] Z. Boos *et al.*, "A fully digital multimode polar transmitter employing 17 b RF DAC in 3G mode," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 376–378.

[10] J. Xiao *et al.*, "A 13-bit 9 GS/s RF DAC-based broadband transmitter in 28 nm CMOS," in *Proc. Symp. VLSI Circuits*, Jun. 2013, pp. C262–C263.

[11] M. Ingels, X. Zhang, K. Raczkowski, S. Cha, P. Palmers, and J. Craninckx, "A linear 28 nm CMOS digital transmitter with 2× 12 bit up to LO baseband sampling and −58dBc C-IM3," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sept. 2014, pp. 379–382.

[12] E. Bechthum, G. I. Radulov, J. Briaire, G. J. G. M. Geelen, and A. H. M. van Roermund, "A wideband RF mixing-DAC achieving IMD <-82 dBc up to 1.9 GHz," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1374–1384, Jun. 2016.

[13] M. Fulde *et al.*, "A digital multimode polar transmitter supporting 40 MHz LTE carrier aggregation in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 218–219.

[14] M. Mehrpoo, M. Hashemi, Y. Shen, L. C. N. de Vreede, and M. S. Alavi, "A wideband linear *I/Q*-interleaving DDRM," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1361–1373, May 2018.

[15] Y. Shen, R. Bootsman, M. S. Alavi, and L. de Vreede, "A 0.5–3 GHz I/Q interleaved direct-digital RF modulator with up to 320 MHz modulation bandwidth in 40 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Mar. 2020, pp. 1–4.

[16] S. Su and M. S.-W. Chen, "A 1–5 GHz direct-digital RF modulator with an embedded time-approximation filter achieving −43 dB EVM at 1024 QAM," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. C20–C21.

[17] M. Park, M. H. Perrott, and R. B. Staszewski, "An amplitude resolution improvement of an RF-DAC employing pulsewidth modulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 11, pp. 2590–2603, Nov. 2011.

[18] J. S. Walling *et al.*, "A class-E PA with pulse-width and pulse-position modulation in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1668–1678, Jun. 2009.

[19] S. Su, T.-I Tsai, P. K, Sharma, and M. S.-W. Chen, "A 12 bit 1 GS/s dual-rate hybrid DAC with an 8 GS/s unrolled pipeline delta-sigma modulator achieving > 75 dB SFDR over the Nyquist band," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 896–907, Apr. 2015.

[20] S. Su and M. S.-W. Chen, "A 12-bit 2 GS/s dual-rate hybrid DAC with pulsed-error pre-distortion and in-band noise cancellation achieving > 74 dBc SFDR and < -80 dBc IM3 up to 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2963–2978, Dec. 2016.

[21] S. Su and M. S.-W. Chen, "A 16-bit 12-GS/s single-/dual-rate DAC with a successive bandpass delta-sigma modulator achieving <−67-dBc IM3 within DC to 6-GHz tunable passbands," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3517–3527, Dec. 2018.

[22] Y. Tsividis, "Signal processors with transfer function coefficients determined by timing," *IEEE Trans. Circuits Syst.*, vol. CS-29, no. 12, pp. 807–817, Dec. 1982.

[23] D. Vallancourt and Y. P. Tsividis, "A fully programmable sampled-data analog CMOS filter with transfer-function coefficients determined by timing," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 6, pp. 1022–1030, Dec. 1987.

[24] D. Vallancourt and Y. P. Tsividis, "Timing-controlled fully programmable analogue signal processors using switched continuous-time filters," *IEEE Trans. Circuits Syst.*, vol. CS-35, no. 8, pp. 947–954, 1988.

[25] E. Roverato *et al.*, "All-digital LTE SAW-less transmitter with DSP-based programming of RX-band noise," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3434–3445, Dec. 2017.

[26] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "An incremental-charge-based digital transmitter with built-in filtering," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3065–3076, Dec. 2015.

[27] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "A 0.22 mm^2 CMOS resistive charge-based direct-launch digital transmitter with −159 dBc/Hz out-of-band noise," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 250–252.

[28] D. K. Su and B. A. Wooley, "A CMOS oversampling D/A converter with a current-mode semidigital reconstruction filter," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1224–1233, Dec. 1993.

[29] W. M. Gaber, P. Wambacq, J. Craninckx, and M. Ingels, "A CMOS IQ direct digital RF modulator with embedded RF FIR-based quantization noise filter," in *Proc. ESSCIRC*, Sep. 2011, pp. 139–142.

[30] S. Fukuda, S. Miya, M. Io, K. Hamashita, and B. Nauta, "Direct-digital modulation (DIDIMO) transmitter with −156 dBc/Hz RX-band noise using FIR structure," in *Proc. ESSCIRC*, Sep. 2012, pp. 53–56.

[31] S. M. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A bandpass RF-DAC with embedded FIR reconstruction filter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 2370–2379.

[32] R. Bhat and H. Krishnaswamy, "A watt-level 2.4 GHz RF I/Q power DAC transmitter with integrated mixed-domain FIR filtering of quantization noise in 65 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 413–416.

[33] R. Bhat, J. Zhou, and H. Krishnaswamy, "Wideband mixed-domain multi-tap finite-impulse response filtering of out-of-band noise floor in watt-class digital transmitters," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3405–3420, Dec. 2017.

[34] R.-C. Marin, A. Frappé, B. Stefanelli, P. Cathelin, A. Cathelin, and A. Kaiser, "Digital RF transmitter with single-bit M-driven switched-capacitor RF DAC and embedded band filter in 28-nm FD-SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3200–3209, Jul. 2019.

[35] C. Erdmann *et al.*, "A 330 mW 14 b 6.8 GS/s dual-mode RF DAC in 16 nm FinFET achieving −70.8 dBc ACPR in a 20 MHz channel at 5.2 GHz," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 280–281.

[36] L. Duncan *et al.*, "A 10-bit DC-20-GHz multiple-return-to-zero DAC with > 48-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3262–3275, Dec. 2017.
[37] S. Balasubramanian *et al.*, "Systematic analysis of interleaved digital-to-analog converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 882–886, Dec. 2011.
[38] W. M. Gabor, P. Wambacq, J. Craninckx, and M. Ingels, "A 21-dBm *I/Q* digital transmitter using stacked output stage in 28-nm bulk CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4744–4757, Nov. 2017.
[39] A. Zhang and M. S.-W. Chen, "A watt-level phase-interleaved multi-subharmonic switching digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3452–3465, Dec. 2019.
[40] A. Pozsgay, T. Zounes, R. Hossain, M. Boulemnakher, V. Knopik, and S. Grange, "A fully digital 65 nm CMOS transmitter for the 2.4-to-2.7 GHz WiFi/WiMAX bands using 5.4 GHz RF DACs," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 360–619.

Shiyu Su (Member, IEEE) received the B.S. degree from the Beijing University of Post and Telecommunication, Beijing, China, and Queen Mary, University of London, London, U.K., in 2011, and the M.S. and Ph.D. degrees from the University of Southern California (USC), Los Angeles, CA, USA, in 2013 and 2019, all in electrical engineering.

His research interests include high-speed data converters, digital phase-locked loop, wireless/wireline transceiver, and analog/mixed-signal design automation.

Dr. Su was a recipient of the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award for 2017–2018 and the IEEE Solid-State Circuits Society (SSCS) Student Travel Grant Award for 2019–2020. He is a Ming Hsieh Institute Scholar from 2019 to 2020.

Mike Shuo-Wei Chen (Senior Member, IEEE) received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1998, and the M.S. and Ph.D. degrees from the University of California at Berkeley, Berkeley, CA, USA, in 2002 and 2006, all in electrical engineering.

As a Graduate Student Researcher, he proposed and demonstrated the asynchronous SAR ADC architecture, which has been adopted today for low-power high-speed analog-to-digital conversion products in industry. He is currently an Associate Professor with the Electrical Engineering Department, University of Southern California (USC), and holds the Colleen and Roberto Padovani Early Career Chair position. At USC, he leads an analog mixed-signal circuit group, focusing on data converter, wireless, wireline, computing, and design methodology. His research group has been exploring new circuit architectures that excel beyond the technology limitation, as exemplified in their recent works in power amplifier (PA), analog-to-digital converter (ADC), digital-to-analog converter (DAC), and phase-locked loop (PLL). From 2006 to 2010, he has been a member of the Analog IC Group, Atheros Communications (now Qualcomm Atheros), San Jose, CA, USA, working on mixed-signal and RF circuits for various wireless communication products.

Dr. Chen was a recipient of the Qualcomm Faculty Award in 2019, the NSF Faculty Early Career Development (CAREER) Award and the DARPA Young Faculty Award (YFA) in 2014, the Analog Devices Outstanding Student Award for recognition in IC design in 2006, and UC Regents' Fellowship at Berkeley in 2000. He also achieved an honorable mention in the Asian Pacific Mathematics Olympiad in 1994.