Design and Validation of a 20 kVA, Fully Cryogenic, 2-Level GaN Based Current Source Inverter for Full Electric Aircrafts

Mustafeez-ul-Hassan, *Graduate Student Member, IEEE*, Asif Imran Emon, *Graduate Student Member, IEEE*, Fang Luo, *Senior Member, IEEE*, and Vyacheslav Solovyov

***Abstract*—This paper presents design of a cryogenic power electronics converter using wide bandgap (WBG) devices. A 20 kVA two-level current source inverter (2L-CSI) is designed and validated under both room temperature (RT) and cryogenic temperature (CT) of 77 K. CSI have been neglected because of physically large and heavy DC link inductor as compared to DC link capacitor of voltage source inverters (VSI). However, higher power, together with operation at CT in full electric aircrafts (FEA), makes them superior in size, volume and power quality. The advantage in volume is primarily attributed to utilization of air-core inductors with superconducting tapes as DC link storage elements. Therefore, a 2L-CSI with both power stage and associated components at CT is designed and evaluated. As part of converter development, commercially off the shelf (COTS) products including integrated circuits (ICs), isolated auxiliary power supplies, and passive components were utilized. Numerous laboratory prototypes of cryogenic subsystems were built to screen out the cryo-compatible components. Based on components screening, converter subsystems, namely gate driver (GD) board and double pulse test (DPT) platform, were also developed. Characterization of these subsystems were performed both at RT and CT, where both individual and integrated testing was carried out.**

***Index Terms*—Cryogenic electronics, Power converter, Aircraft propulsion, Wide band gap (WBG) devices, Current source inverter (CSI)**

I. Introduction

Future aviation industry faces numerous challenges, including improved overall efficiency and volumetric density, reduced emissions and lowered dependence on carbon-based fuels. With the aviation industry emitting 780 million tonnes of CO_2 in 2015, the number is expected to substantially increase as global aviation industry demand grows in the future [1]. In response to the forecasted situation, international civil aviation organization (ICAO) set goals of not only keeping CO_2 emissions at 2020 level, but also targetting a 50 % reduction in net CO_2 emissions by 2050, as of 2005 levels [2]. In order to realize low carbon propulsion targets, national aeronautics and space administration (NASA) has adopted two primary paths: enabling the use of alternative fuels, and shifting to innovative propulsion systems [3]. Being environmentally friendly in the long term, electrification of aircraft propulsion systems has attracted numerous researchers from government agencies, industry, and academia. Electrification of aircrafts will not only reduce consumption of carbon based fuel, but will also result in reduced mass and better energy management [4]. In this regard, numerous classifications on the basis of quantity of electrification have been made. Aircrafts replacing non-propulsive components such as mechanical, hydraulic and pneumatic systems are referred either as more electric aircraft (MEA), or all electric aircraft (AEA). On the contrary, aircrafts targeted at replacing all the propulsive power by electric means are referred as fully electric aircrafts (FEA). Numerous studies have revealed the importance of hybrid electric propulsion (HEP) and turbo electric propulsion (TEP) as an intermediate step and short term goal towards electrified propulsion (EP) systems or FEA [5]–[8].

Although HEP and TEP serve as a step forward towards FEA, the battery energy storage has been identified as key bottleneck towards feasibility of hybridization of commercial aircraft. In order to address the long term challenges associated with FEA, NASA has funded exploring the usage of liquid hydrogen (LH_2) energy storage for FEA [9]. The project namely cryogenic high efficiency electrical technologies for aircraft (CHEETA) aims at developing a FEA that has an on-board cryogenic system to store LH_2, which will be used for fuel cell energy conversion. The concept of using LH_2 was influenced by its being a highly efficient, safe and clean alternative source of energy [10]; besides having significantly higher specific energy over modern battery systems [11] being employed in HEP. Furthermore, the presence of an on-board cryogenic system enables the utilization of highly efficient superconducting transmission lines, machines, and cryogenic power electronics conversion systems.

A. Introduction to Different Cryogenic Systems and Their Benefits

A cryogenic temperature (CT) is classified primarily to be below 123 K where cryogenic environment can be created with the help of liquid nitrogen (LN_2, 77 K), LH_2 (33 K) or liquid helium (LHe_2, 4 K). Considering the increased applications of cryogenic systems in future commercial aircrafts, power

This paper was submitted on December 31, 2021, revised on March 27, 2022 and accepted on May 04, 2022. The name of the corresponding author is Fang Luo.

Mustafeez-ul-Hassan is with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY 11794-2350 and Department of Electrical Engineering, University of Engineering and Technology, Lahore 54890, Pakistan (e-mail: mustafeez.hassan@stonybrook.edu and mustafeezulhassan@uet.edu.pk). Asif Imran Emon, and Fang Luo are with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY 11794-2350 (e-mail: asifimran.emon@stonybrook.edu, and fang.luo@stonybrook.edu), whereas Vyacheslav Solovyov is with Brookhaven Technology Group Inc., Stony Brook, NY 11794 (e-mail: slowa@brookhaventech.com)

electronics converters are envisioned to play a significant role. These converters, combined together with superconducting motors, magnetic energy storage modules and cables, will enable reduced weight and volume, higher power efficiencies, and therefore superior overall performance [12]. A cryogenic system where superconducting machines have multi-megawatt ratings offer reduced weights and smaller volumes, and are cheap in costs [13]; the overall increase in power efficiency is primarily attributed to improved performance of semiconductor devices, as they offer reduced conduction losses, and increased switching speeds [13]–[16]. Furthermore, such systems are not only limited to future commercial and military aircrafts, but cryogenic power electronics converters (CPEC) find their potential applications in medical diagnostics, multi-megawatt wind power generation, superconducting magnetic energy storage devices (SMES), cargo ships and instrumentation.

B. Review of Commercially Available Components for CPEC

1) Power Semiconductor Devices

Characterization of power electronics devices at CT plays an important role in determining the performance of cryogenic converters. Numerous articles have been published discussing characterization and advantages associated in operating semiconductor devices around CT. Amongst the active devices, Si MOSFETs and IGBTs have been shown to offer reduced on-state resistance and breakdown voltage, faster switching times but increased gate threshold voltage [13]–[15], [17]. Although the on-state resistance decreases, the reduction in break down voltage may ultimately lead to higher device resistance. On the contrary, wide-band gap (WBG) devices have shown conflicting behaviour where SiC offers increased on-state resistance and gate threshold voltage, stable breakdown voltage and switching speeds, however a GaN high electron mobility transistor (HEMT) shows reduced on-state resistance, faster switching times, and stable breakdown and threshold voltages [13], [17].

2) Passive Components

Several papers have reported on properties of passive components with reduction in temperatures [18]–[22]. From the studies conducted, it can be concluded that most of the capacitors show degradation either in capacitance value, equivalent series resistance (ESR) or displacement factor. Only negative-positive-zero (NP0) and polypropylene sulfide (PPS) based capacitors have been shown to offer stable capacitance and ESR [18]. Similar to capacitors, inductors have also been characterized in several literature [23]–[33]. As a summary, it can be concluded from these articles that only powdered cores, specifically molypermalloy powder (MPP) core and high flux core (HFC) have been shown to offer stable inductance and increased quality factor with reduction in temperature. A brief review about passive components has been reported in [17].

C. Review of State-of-the-Art CPEC

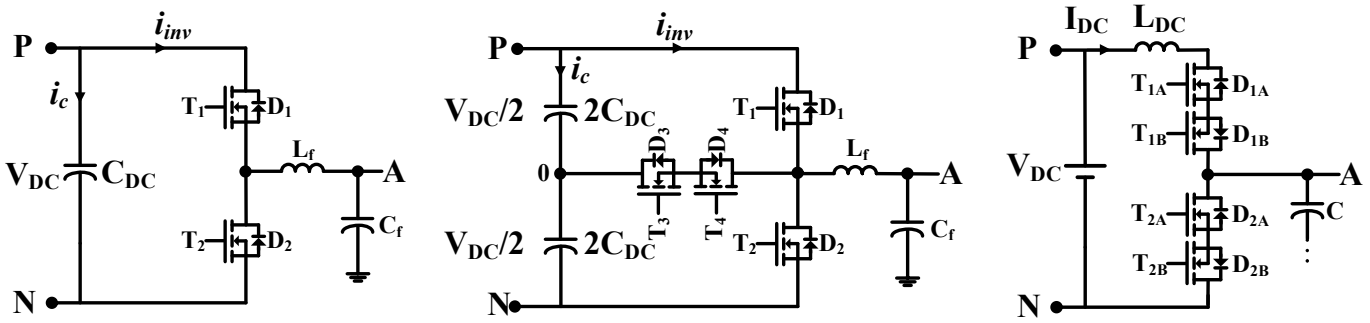
Although much research has been done on characterization of semiconductors and passive components at CT, very few converters are reported for such applications. Furthermore, the converters developed are generally reported to have lower power ratings, and control circuitry placed outside the cryo-environment. In this section of the paper, review about both DC-DC and DC-AC converter topologies developed for CTs is provided. The review focuses on converter power ratings, type of semiconductor devices used, and nature of filtering components employed.

1) DC-DC Converters

Majority of the cryogenic converters developed so-far are of DC-DC conversion type. A 175 W pulse width modulated (PWM) buck type DC-DC converter was designed and tested at LN_2 temperature in [34]. The converter was operated at a 50 kHz switching frequency using Si devices, with an efficiency improvement of 1.2 % at LN_2 temperature. MPP core and polypropylene film capacitors were utilized for filtering purposes, while the power circuit and filter components were placed inside the chamber. Similarly [35], [36] presented the performance of a 60 W three-level buck converter operating down to 77 K at a switching frequency of 50 kHz. Performance of hard and soft switching 500 W buck type converter was reported for a temperature down to 20 K in [37]. In the paper, authors used different power MOSFET devices and diodes for the study, and found maximum reduction of semiconductor losses to be 85 %. For the experimentation, both the power and gate drive circuit were placed in CT. A 24 VDC, 20 W full bridge DC motor drive for ultra-wide temperature range (43 K – 393 K) was developed in [38], [39]. The targeted permanent magnet DC motor drive was developed and tested until 89 K using Si devices. A similar 150 W PWM boost type converter was reported in [40], [41] for a wide operating temperature range with an input of 24 VDC and 48 VDC output. The converter operates with Si devices and has an efficiency of 92.2 % at around 90 K, with the power circuitry and the MPP based input energy storage inductor being placed inside the cold environment. [42] reported the performance difference for a boost converter operating at RT and LN_2 temperature. Authors reported the soft switching configuration at LN_2 temperature to be the most efficient in terms of semiconductor losses. Out of all the DC-DC converters designed and tested for low temperatures, [43] presented the highest power rating of 40 kW boost converter using CoolMOS MOSFETs and high temperature superconducting (HTS) inductor. HTS normally behave as superconductors above 77 K up until $\sim$ 100 K. For the converter developed, 85 % reduction in terms of conduction losses, and 87 % reduction in overall system was reported down to LN_2 operation compared to RT performance.

2) DC-AC Converters

Unlike DC-DC converters, much less has been reported on low temperature DC-AC converters. A 40 kW three-level active neutral point clamped converter (3L-ANPC) was designed using Si devices in [44]. The converter was designed with 1 kVDC for an output of 3 kHz fundamental frequency, whereas switching frequency of 140 kHz was adopted. Inspite of the reduction in breakdown voltage and increase in gate threshold voltage, Si based devices were used for the intended cryogenic operation of converter. Furthermore,



(a) 2L-VSI (b) 3L-TNPC-VSI (c) 2L-CSI

Fig. 1: Topologies considered for MW class converter

numerous Si based devices were put in series to compensate for the lowered breakdown voltage, which leads to increased gate driving complexity and sophisticated control. Additional SiC based Schottky barrier diode was configured to control reverse recovery losses, a material which has shown to offer increased losses at CT. The converter also places the gate driving circuitry away from the power devices which may affect the device performance and control. Similarly a single phase three level flying capacitor multi-level inverter was developed for near cryogenic operating temperature in [45], [46]. The inverter was designed for a load voltage of 45 V with DC link rated at 150 VDC using 200 V GaN field effect transistors (FETs). Although the efficiency and loss analysis has been provided for temperatures until 133 K, there is no information about the output voltage/current shape and quality at 133 K. Furthermore, the ratings of power and voltage considered are way lower than intended application of hybrid aircraft. The latest development in DC-AC converter design has been reported in the design of a mega-watt (MW) class cryogenically cooled inverter [47]. Two 500 kW, 1 kVDC, three level active neutral point clamped (3L-ANPC) inverters have been paralleled through interleaved inductors for an output voltage of 600 V. The inverter was developed using SiC devices operating at a switching frequency of 70 kHz with space vector modulation (SVM) using SiC devices. Although testing of converter was carried out both at RT and LN_2, utilizing SiC based devices for lower temperatures is not preferable because of increased conduction losses and gate threshold voltage. Additionally, all the gate driving and auxiliary components are placed at RT.

From the review of converters, it can be observed that converters designed for cryogenic applications have low power ratings. Also, Si based devices have been used in most of the designs, whereas SiC and GaN based devices have been used in just one design each. Additionally, all the DC-AC converters employed are primarily voltage source inverters (VSI) where a DC link storage capacitor is used. On the contrary, no analysis has been conducted for a current source inverter (CSI) for such an application. CSIs historically have been neglected because of commercially unavailable reverse voltage blocking (RVB) devices, and therefore increased conduction losses. Additionally, DC link storage inductor possess greater challenge in justifying the power density of inverter. Considering the application of converters in cryogenic applications, superconducting inductor should be thoroughly evaluated in conjunction with a two-level CSI (2L-CSI).

D. Organization of Paper

This paper discusses the design trade-offs and analysis of a fully cryogenic MW class inverter for FEA, and presents the necessary guidelines. Section II describes the converter design trade off studies particularly for cryogenic temperatures, and establishes the basis for converter design comparison. Section III presents the design and development of fully cryogenic converter subsystems with successful testing until 77 K. In section IV, discussion about design, development and validation of a complete cryogenic converter system is presented. Section V is dedicated to challenges in development of cryogenic conversion systems, while the last section concludes and presents the future work.

II. Comparative Study and Tradeoffs for Design of CPEC

Before designing the real converter for cryogenic applications, the most feasible converter topology should be down-selected at first. A comprehensive comparison of the converter in terms of DC link storage, volume of passive components, efficiency and electromagnetic interference (EMI) should be carried out to find the optimal topology. The paper considers three basic converter topologies: (a) two level VSI (2L-VSI), (b) three level t-type neutral point clamped inverter VSI (3L-TNPC-VSI) and (c) 2L-CSI. Phase leg configurations of all three converter topologies are shown in Fig. 1. The power considered for such an analysis should be in multi-MW range as suggested by NASA for EP [48]. Therefore a 2.5 MW converter will be considered as a baseline design in this paper. In order to find the optimal topology for such an application, numerous factors were considered together to formulate a figure of merit (FOM) for the converters.

A. Design Tradeoff for Energy Storage Components in CPEC

As a first index of FOM, energy storage of DC link capacitors and inductors in VSI and CSI is compared. This energy storage will be proportional to the magnitude of capacitor and inductor, and thus the resultant volume as well. Considering the DC link for VSI to be V_{DC} with energy storage capacitor C_{DC}; and I_{DC} with energy storage to be L_{DC} for CSI; the

energy storage for both the converter types can be related as:

$$W_{C_{DC,VSI}} = \frac{1}{2} C_{DC} V_{DC}^2$$
$$W_{L_{DC,CSI}} = \frac{1}{2} L_{DC} I_{DC}^2 \quad (1)$$

Further, assuming both the converter types to be ideal and feeding a symmetrical load at V_{LL-RMS} for a power of P, and SVM control; the energy storage ratio for the VSI and CSI can be rearranged as:

$$\frac{1}{2} C_{DC} \left(\sqrt{2} V_{LL-RMS}\right)^2 = \frac{1}{2} L_{DC} \left(\sqrt{\frac{2}{3}} \frac{P}{V_{LL-RMS}}\right)^2$$
$$\implies \frac{C_{DC}}{L_{DC}} \propto \frac{V_{C_{DC}}}{V_{L_{DC}}} = \frac{P^2}{3 V_{LL-RMS}^4} \quad (2)$$

As can be inferred from (2), DC link capacitor for VSI grows quadratically with power, whereas inductor for CSI grows quartically with load voltage. Therefore, power and output voltage influence the selection of DC link storage components, and this ratio may help optimally select the converter. It is worth noting that this relation is irrespective of volumetric scaling between DC-link components of both the converter types considered.

In order to have a baseline about converter topology, variable power rating from 1-2.5 MW was considered for load voltage (V_{LL-RMS}) of 600 V and 800 V. As can be seen from Fig. 2, energy storage ratio exceeds unity for all the powers considered for 600 V, whereas it exceeds beyond 1.25 MW for 800 V. This ratio indicates a VSI to be offering greater volumes for DC link storage elements for MW class inverters, therefore favoring a CSI from the perspective of volumetric density.

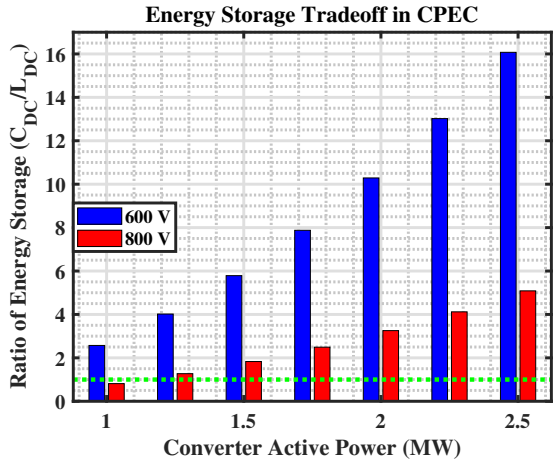


Fig. 2: Comparison on the basis of energy storage

Apart from lower load voltage favoring a CSI, a lower DC link voltage also supports a CSI from the perspective of smaller energy storage. Considering a fixed energy/power content, higher DC link current is required at reduced voltages, therefore resulting in a lower value of L_{DC} for a CSI. For inductor development, numerous core materials can be considered, however an air-core inductor together with superconducting tapes can be employed for high power/current applications, especially at CT. It is worth mentioning that the loss in relative permeability (μ_r) while using air-core inductor gets compensated by much higher current carrying capability of conductors at CT [33]; therefore, resulting in reduced volume of DC link energy storage of a CSI. Furthermore, the problems associated with different core materials in terms of hysteresis and core losses, and limited saturation flux density can also be avoided using air-core inductors.

B. Volume Estimation for Passive Components in CSI and VSI

This subsection discusses the dimensioning of filter components since 30 % of volume of any converter is occupied by them [49], so it is important to have an appropriate estimate of their magnitude, and volume. These filter components primarily comprise of different configurations of inductors and capacitors, where input storage capacitors are required at the DC link for VSIs, and output filter capacitors are required for CSI. Conversely input storage inductors are required at the DC link of CSIs, and LC type output filter is considered for VSIs to have comparable total harmonic distortion (THD). For the volume estimation, converter rating of 2.5 MW generating an output V_{LL-RMS} of 600 V are considered. The equivalent DC link voltages of 1000 VDC and 540 VDC are considered for VSIs and CSIs respectively with SVM as modulation technique [50]. To validate the design of passive components, simulation models were developed in MATLAB and LTspice, and design specifications were verified.

1) Sizing of DC link storage in CSI and VSI

An estimate about input DC link capacitors based upon ripple current can be made from [51], however actual values maybe limited by the current rating [52]. DC link storage capacitors for VSI can be identified from Fig. 1a and 1b. Similarly DC link storage inductor for CSI can be estimated from [53] and can be identified in Fig. 1c. Both the components can be dimensioned using (3), where f_{sw} is the converter switching frequency, and ΔV_{DC} and ΔI_{DC} represent the ripple in DC link voltage and current respectively. For the calculations of DC link storage elements, voltage ripple and current ripple percentage of 5 % was used for VSI and CSI respectively. Summary about DC link sizing for all the converter types considered is presented in Table I where nearest commercially off the shelf (COTS) components are tabulated.

$$C_{DC} = \frac{P}{\left(V_{DC} \Delta V_{DC} \pm 0.5 \Delta V_{DC}^2\right) f_{sw}}$$
$$L_{DC} = \frac{V_{LL-RMS}}{4 f_{sw} \Delta I_{DC}} \quad (3)$$

2) Sizing of AC link filters in CSI and VSI

Output filter combination for converter depends upon the type and sensitivity of the load. Although a fully superconducting machine (SCM) for CT results in 3.5 times power to weight ratio as compared to other configurations, it is very sensitive to AC losses [54]. Therefore, converter output voltage should have lower THD and better power quality. To determine the output filter, voltage THD limit of 3 % was considered for the analysis. To achieve this, an LC type filter combination is

Table I: Sizing of DC link storage and AC link filter components

Property	2L-VSI	3L-TNPC-VSI	2L-CSI
C_{DC}	1500 μF, 1150 VDC	2×3000 μF, 630 VDC	—
L_{DC}	—	—	25 μH, 3290 A
C_f	3×65 μF, 400 VAC	3×60 μF, 400 VAC	—
L_f	6.15 μH, 3400 A	4.61 μH, 3400 A	—
C	—	—	3×430 μF, 400 VAC

considered for VSIs and can be designed using (4), whereas already existing dv/dt filter should be sufficient for CSI. In the equations, ΔI_{max} represents the peak-peak ripple current, whereas f_{res} is the resonance frequency.

$$\begin{aligned} L_f &= \frac{V_{DC}}{3\sqrt{2}\pi f_{sw}\Delta I_{max}} \\ C_f &= \frac{1}{4\pi^2 f_{res}^2 L_f} \\ C &= \frac{I_{DC}}{4 f_{sw}\Delta V_{LL-RMS}} \end{aligned} \tag{4}$$

A summary about AC link filter sizing for all the converter types considered is also provided in Table I.

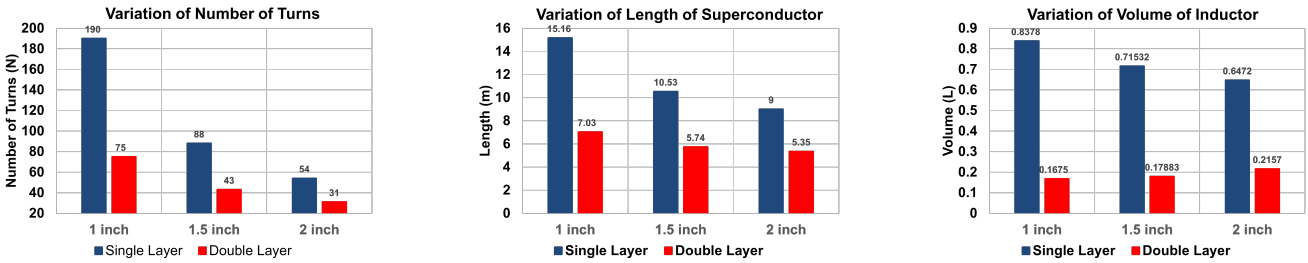
3) Overall Volume Comparison of DC link storage and AC link Passive Components

Having determined the magnitudes of different filtering components, comparison amongst the topologies is extended to determination of volume occupied by them. To determine the volume for inductors, numerous inductor types commonly used for CT applications were considered. From the literature, it can be concluded that ferrite and amorphous materials not only loose their permeability, but their core losses also increase, whereas powdered cores show stable operation [17]. Considering the MW range of power, numerous powdered cores need to be paralleled to justify area product Ap [55], therefore resulting in huge volume and weight. On the contrary, coreless inductors with superconducting wires/tapes were considered for the analysis, and found them to be more suitable for such low temperature and high-power applications. Coreless inductors not only offer zero core losses, but also offer no limitation on saturation flux density [33]. Numerous superconducting tapes such as magnesium diboride (MgB_2) or yttrium barium copper oxide (YBCO) can be utilized for such inductor building applications, but YBCO type superconductor was considered in this application; with a conservative value of current density to be 200 A/mm^2. Such superconductor was wound in a multilayer cylindrical orientation to furnish the inductors specified in Table I. As part of inductor optimization process, single and double layered windings were wound around various diameters of aluminum cylinders (serving as inductor former). The optimization process for L_{DC} has been shown in Fig. 3. As can be seen from Fig. 3a, winding the superconducting tapes around 2-inch diameter inductor former using a double layered structure not only offers the least number of turns, but also results in least length of superconductor as shown in Fig. 3b. Therefore, L_{DC} will give volume of around 0.2157 litre by having 31 turns in double layered structure as shown in Fig. 3c. The approach was extended to determination of volume for output filter inductors of VSIs and optimized volume with such an approach is displayed in Fig. 4a.

Similar to inductor optimization, optimization of capacitors was also carried out. PPS capacitors are considered for the comparison because of their negligible variation in capacitance and reduced ESR at CT [17]. Capacitors from numerous vendors were selected and the one offering the best combination of volume and ESR is being considered in the analysis. Based upon the manufacturer provided data-sheet [56], variation of capacitor volume was studied and plotted in Fig. 4b for all the three topologies, whereas overall volume of converter (sum of inductors and capacitors) is shown in Fig. 4c. It can be seen from the overall volume comparison that 2L-CSI occupies the least of volume in terms of passive components.

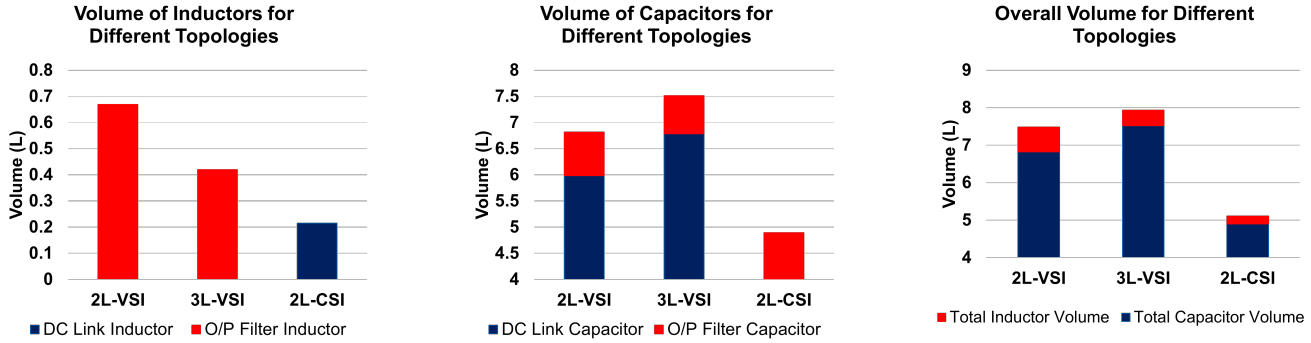
C. EMI Performance Comparison Between 2L-VSI and 2L-CSI

In this subsection, comparison between 2L-VSI and 2L-CSI will be carried out based on conducted EMI. 3L-VSI



(a) Required turns variation (b) Required length variation (c) Inductor volume variation

Fig. 3: Optimization of L_{DC} for 2L-CSI



(a) Volume of inductors (b) Volume of capacitors (c) Total volume of filter components

Fig. 4: Variation of volume with topology

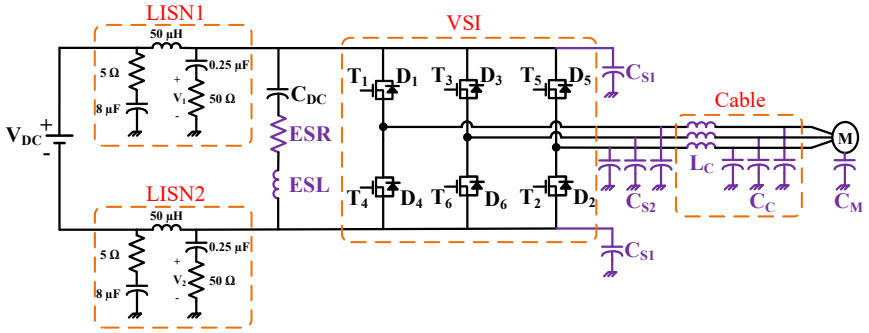
is omitted from the comparison as 4c suggests the highest volume for passive components for this topology. For the analysis, LTspice based simulations were carried out for the two converter topologies with numerous parasitics elements as shown in Fig. 5a and 5c.

Typical parasitics considered for the comparion are shown in Fig. 5a and 5c. Values of 200 pF and 560 pF were considered for the stray components $C_{s1}/C_{s2}/C_{s3}$ and C_M respectively, whereas 100 nH and 50 pF were adopted for L_c and C_c respectively for cable length of 1-m. The simulations were carried out for output power of 2.5 MW at 600 V_{LL-RMS} while using real device models from the manufacturer. For the DC link, values calculated in section II-B were utilized. Furthermore, switch node parasitic capacitances, stray capacitance from DC link to ground, cable parasitic elements and motor model were also simulated, and kept uniform for both the converters as discussed in [57]. Both common mode (CM) and differential mode (DM) EMI spectra was determined and plotted as shown in Fig. 5b and 5d respectively. For the analysis, a MIL-461 based LISN was considered and was connected at the input side of converter.

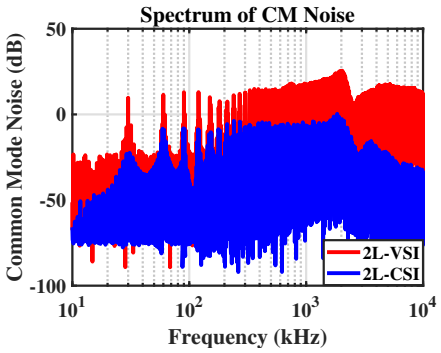
The EMI spectrum for a 2L-CSI was further extended by including equivalent parallel capacitance (EPC) of L_{DC}. It was found that EPC forms a self-resonating parallel LC tank which can contribute to the conducted noise. It was also found that a 2L-CSI still offers lower noise spectrum even after consideration of EPC. However, the value of EPC needs to be optimized and the methods to limit EPC of inductors can be found from [55], [58].

D. Summary of Design Tradeoffs for CPEC

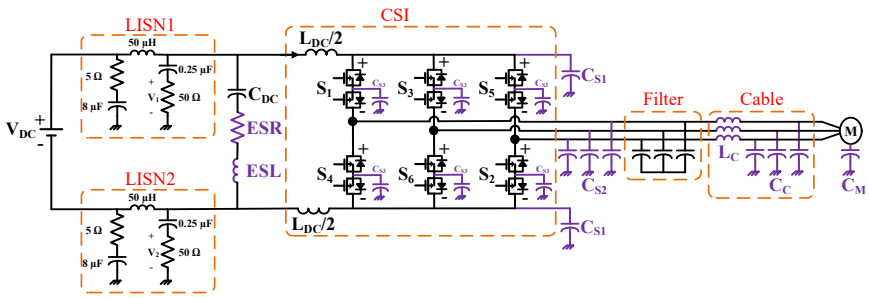
From the analysis conducted above, it can be easily observed that a 2L-CSI offers advantages in terms of smaller



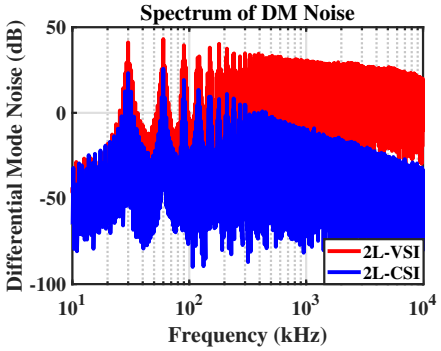
(a) 2L-VSI with parasitics and LISN



(b) CM noise measured across LISN



(c) 2L-CSI with parasitics and LSIN



(d) DM noise measured across LISN

Fig. 5: Variation of volume with topology

DC link storage inductor size as compared to capacitor size in VSI. The collective volume of passive components both at the DC and AC link was found to be least with 2L-CSI while using an air-core inductor with superconducting material. Additionaly, an estimate about conducted EMI was also made which supports 2L-CSI in terms of lesser interference generated, hence smaller sizes of required filters. Furthermore, a CSI inherently offers better power quality and THD at the output, thus helping in reducing AC losses in SCM [57]. On the contrary, disadvantage of higher conduction losses can be neutralized by utilizing monolithically integrated bidirectional RVB devices [59].

Considering the importance of all the factors discussed above, a 2L-CSI was acknowledged to be more feasible for MW scale power conversion systems for cryogenic applications. Therefore, a 2L-CSI converter will be designed, analyzed and tested in rest of the paper.

III. Design and Demonstration of CPEC Subsystems

From the perspective of a power electronics converters, a majority of the converters designed have utilized Si devices [37], [42], [44]. Despite the optimal operating performance of GaN devices at CT ($<$ 123 K), only single power electronics converter has been built using GaN FETs [45] and has been tested until 133 K only. One of the reasons for the uncommon emergence of GaN converters at CT maybe attributed to non-availability of gate drivers at such low temperatures [60]. Until date, none of the gate drivers have been reported to operate successfully at CT. Since GaN based devices are extremely sensitive to fast switching signals and layout [61], operating them at low temperatures further increases their switching speeds [62]. This adds to the already existing complexity levels, and therefore the design of a reliable, repeatable, and resilient gate drive configuration for such devices will be extremely important for upcoming applications [60].

A. Design of Gate Driver at CT

In almost all of the converters built for CT applications, gate drivers (GD) and auxiliary components have been placed outside the cryogenic environment. This type of arrangement can perform satisfactorily if switching devices are Si based, whereas making GaN devices work with such an arrangement will be extremely difficult. Considering the superior performance of GaN devices at CT, together with absence of any low temperature GD; this section of paper targets at successful implementation of a LN_2 immersed GD. Implementation of a gate driving printed circuit board (PCB) for such low temperatures is susceptible to numerous challenges including: (a) choice of passive components such as decoupling capacitors, resistors, common mode chokes, (b) choice of integrated circuits (IC) such as gate driving IC, (c) choice of diodes such as Zener diode, rectifier, (d) choice of manufacturing material such as PCB material, soldering material, interconnects, (e) selection of isolated auxiliary power supply (APS).

A noise tolerant and LN_2 temperature resilient gate driver was designed to overcome the challenges discussed previously. The GD was successfully tested at RT as well at CT under both unloaded and loaded conditions. In the proposed CT GD, all the components will be placed inside low temperature environment. Since a typical GD consists of a buffer IC, a gate driving IC and an APS, the overall configuration for the proposed LN_2 immersed GD is shown in Fig. 6.

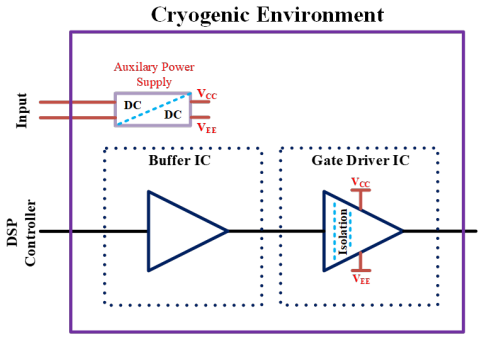


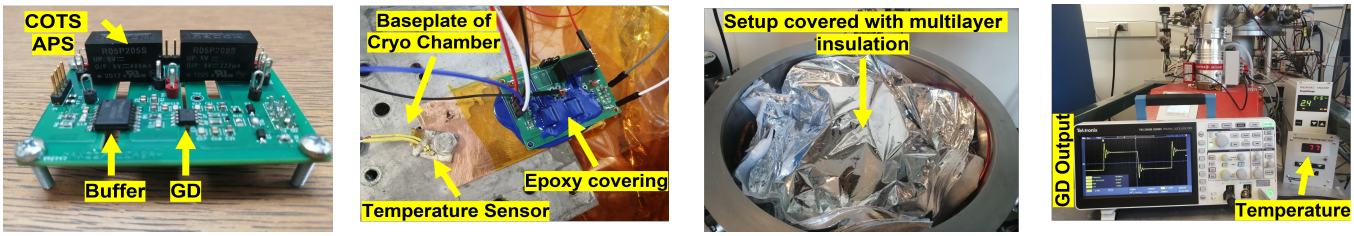
Fig. 6: Structure of the GD

1) Selection of Gate Driver Components at CT

For a well-functioning GD, both the ICs and APS should be compatible with extreme low temperatures. For such purpose, numerous COTS APS were tested and characterized in laboratory at both RT and LN_2 temperatures. Since most of the COTS available in the market use ferrite-based core materials, it is nearly impossible to find a COTS APS which can work at extremely low temperatures. The reason for their failure may be attributed to increased power losses, reduced inductance, and quality factor at extreme low temperatures [17]. Similarly, a buffer stage is also added to offer high impedance to microcontroller, whereas a gate driving stage is designed to source and sink high gate-source currents for GaN switching devices. Considering the ICs required in a GD board, numerous technologies like bipolar junction transistor (BJT) or complementary metal-oxide-semiconductor (CMOS) are commercially available in abundance. For the CT, CMOS devices are good candidates as they offer improved performance in the switching speed [63], whereas BJT is not preferred as they suffer from significant decrease of current gain [64]. In the design of gate driver, passive components were also selected to be CT compatible e.g., nano-crystalline based inductors and common mode chokes were used because of their increased permeability and saturation flux density with reduced temperatures [17]. Additionally, ceramic based NP0 and X5R decoupling capacitors were employed because of their negligible variation of capacitance and dissipation factor with temperature. For the resistors, thin film material was selected for prototyping the board. Normal PCB material consisting of FR-4 was selected for the fabrication of the board while Sn42/Bi57.6/Ag0.4 solder paste was used to solder different components.

2) Laboratory Prototyping of CT Gate Driver and Test Results

Four-layered PCBs were designed for prototyping five different GD ICs with similar board layout and auxiliary components. Two versions of boards were later developed. For the first version of GD PCB, R05P209S APS was employed



(a) GD at RT (b) Baseplate connection (c) Multilayer insulation (d) 77 K operation

Fig. 7: Various steps during characterization of GD

assuming its successful operation at CT. Fig. 7a shows the first version of GD prototyped with dual stage isolation.

For the cryogenic testing, a conduction-cooled cryogenic setup was used for cryogenic testing. Briefly, an 18 inch stainless steel chamber integrated an A230 CryoMech single-stage cryopump. The chamber was evacuated to 10^{-6} Torr by a Pfeiffer HiCube 80 Eco Turbomolecular Pump System. The system reached 25 K base temperature after 4 hours of cryo-compressor operation. The assembled gate driver board was thermally anchored to a 2 mm thick copper plate by a thermally-conductive epoxy, StyCast 2850FT. A 50 μm thick film of Kapton was bonded to the copper plate to insulate the GD circuitry. The copper plate was tightened with baseplate of chamber, where the cold/base-plate temperature was measured by a Si-diode cryogenic temperature sensor (LakeShore 420 model) as shown in Fig. 7b. To prevent heat loss by radiation, the GD assembly was encompassed by a copper radiation shield and ten layers of Mylar multi-layer insulation, as shown in Fig. 7c. Finally, the GD was tested until temperature of 77 K, where successful operation at 200 kHz and 50 % duty cycle is shown on oscilloscope in Fig. 7d. All the measurements for characterization of this setup were taken outside the chamber with Tektronix TBS 2000 B oscilloscope. During the test setup, it was ensured to have minimal length of measurement connections. Complete test setup containing the cryo chamber alongside measurement equipment is shown in Fig. 8.

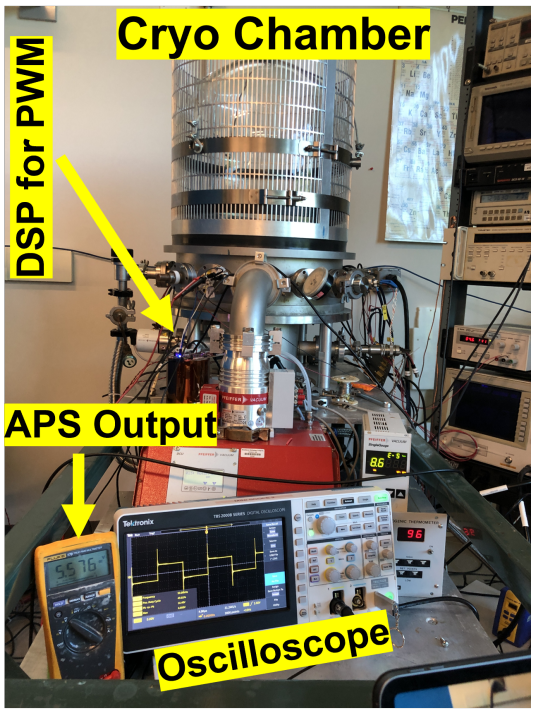


Fig. 8: Outside view of cryo chamber

Having gone through repetitive testing and characterizing the components of GD board at CT, two gate driving ICs were found to be working up to 77 K. However, only single CMOS based buffer IC, i.e. ISO7820 was utilized which was found to be promising till LN_2 temperature. Only one of several combinations of COTS APS showed promising operation. A brief summary about performance of GD ICs and APS with temperatures is provided in Table II and III respectively.

B. Cryogenic Double Pulse Test Platform for Validation of Gate Driver and Device Characterization

Based upon the observations and experimentation of the first GD board, a second version was developed specifically for LN_2 applications. This version incorporates all the components already tested to be operating fine at reduced temperatures.

1) Hardware Development of Double Pulse Test (DPT) Platform

Having developed a successfully operating GD board at LN_2 temperature, a DPT platform was also developed for GaN HEMT. GD boards together with DPT board would not only represent the real switching behaviour, but the switching properties of device can also be determined. For this purpose, GaN systems 650 V, 60 A device GS66516T was used on the DPT board, whereas finalized version of single and dual channel cryogenic GD boards were prototyped as shown in Fig. 9a and 9b respectively. The GD (daughter) boards are designed to be modular, and can be attached to DPT (mother) board as shown together in Fig. 9c. For the DPT board, PPS capacitors by Vishay were employed as main DC link capacitors while X5R high voltage decoupling capacitors were used due to non-availability of NP0 capacitors at such high voltages.

2) Dynamic Characterization of GaN Device and Comparison Between RT and 77 K Operation

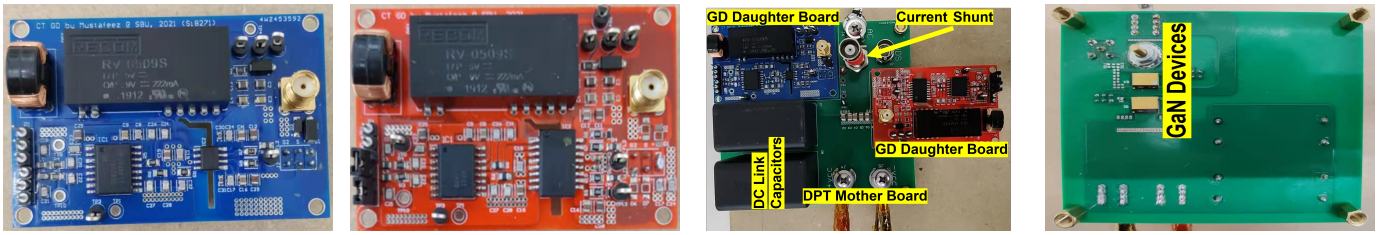
This subsection of the paper compares different quantities for both RT and LN_2 tests performed. RT testing of designed DPT and GD boards was conducted before subjecting them to LN_2 temperature as shown in Fig. 10a. DPTs performed at RT were repeated at LN_2, as shown in Fig. 10b, with similar turn-on and turn-off times to compare the performance of the switching device. In order to be consistent with measurements,

Table II: Summary of performance of gate driver ICs with temperature

Property	SI8271	SI8235AD	UCC21540A	MAX22702	ADUM4221
Fabrication Process	—	—	BiCMOS	BiCMOS	Monolithic
Technology	SiC	Si	—	SiC	—
Minimum Temperature	77 K	∼ 130 K	∼ 93 K	∼ 130 K	77 K

Table III: Summary of performance of COTS APS with temperature

Part Number	Manufacturer	Power (W)	Performance at LN_2	Efficiency at LN_2
PEM2-S5-D5-S	CUI INC	2	Consistent	Reduced to 30 %
PEME1-S12-S12-S	CUI INC	1	Consistent	Reduced to 34 %
MDS01M-12	Meanwell Web	1	Consistent	Reduced to 24 %
MDS01L-12	Meanwell Web	1	Consistent	Stopped working
TRV 1-1212M	Traco Power	1	Consistent	Stopped working
RV-0509S	Recom Power	2	Sometimes mal-operates	Negligible Reduction
R05P209S	Recom Power	2	Inconsistent	Negligible Reduction

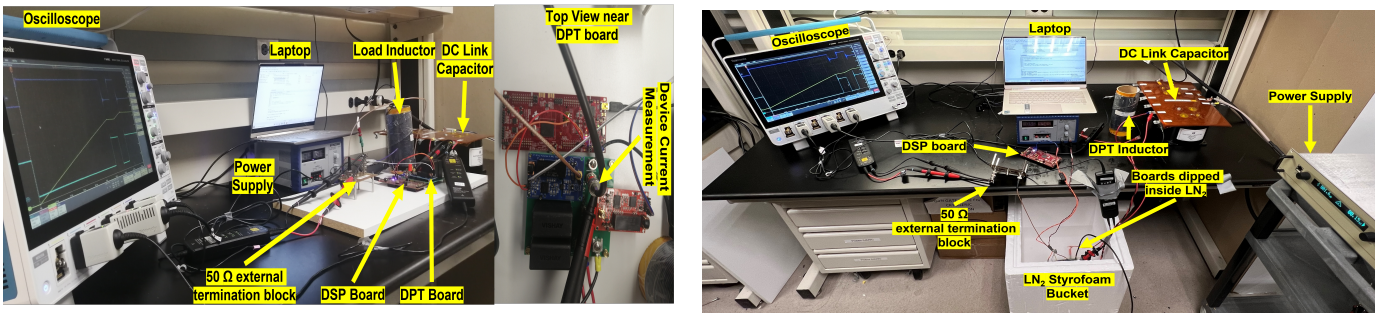


(a) Single channel CT GD (b) Dual channel CT GD (c) Top view of CT DPT (d) Bottom view of CT DPT

Fig. 9: Development of converter subsystems at CT

similar probes were employed both for RT and LN_2 testing. For the measurements, 1 GHz bandwidth oscilloscope by Tektronix was utilized, whereas active probes of 200 MHz bandwidth labelled as THDP0200 were employed for gate-source and drain-source voltage measurements. For the gate-source voltage measurements, SMA based co-axial cable with 50 Ω external termination was used to avoid inserting active probe inside LN_2 dewar. A 2 GHz, 101 mΩ current shunt labelled SSDN-10 was also placed onto DPT board to monitor the device current. During the measurements, it was ensured the Bayonet Neil-Concelman (BNC) cable for gate-source voltage and device current were terminated properly. Furthermore, numerous combinations were adopted to measure drain-source voltage from inside LN_2 dewar; inserting jaws of active probe inside it was found to be the workable solution. It was observed that jaws of active probes become stiff inside LN_2, but is still functional unlike passive probes. Therefore, only active probes (with limited bandwidth) can be used for drain source voltage measurements inside the dewar.

Utilizing the CT- setup shown in Fig. 10b, DPT tests inside LN_2 Styrofoam bucket have been performed for numerous DC link voltages and load currents. Based upon the DPT



(a) RT-setup (b) CT-setup

Fig. 10: Double pulse test setups at different temperatures

performance, difference was observed in device switching characteristics. As seen from Fig. 11a and 11b, GaN based switching device turns off quickly at LN_2. As a result, the peak overshoot voltage, device dv/dt and di/dt at turn off were recorded to be higher as compared to RT; this trend was found to be generic for all the voltages considered for device current of 30 A. Similarly, faster turn-on behaviour of switching device can also be observed from Fig. 11d and 11e for low temperatures. The time improvement for turn-off and turn-on was measured to be around 100 nsec and 20 nsec respectively, and no significant variation was observed with change in operating voltage. This improvement in turn-on and turn-off time will directly influence the switching performance of the device.

Based upon the switching performance determination of GaN device at RT and LN_2, switching loss calculations were performed using 10 % I_{DS}/V_{DS} and 90 % V_{DS}/I_{DS} criterion [65]. Furthermore, a method of V-I alignment with deskew adjustment was adopted for precise calculations of the losses as elaborated in [61]. It is worth mentioning that V-I alignment with deskew adjustment was repeated inside LN_2 dewar before measuring the actual circuit parameters to properly calibrate the system and avoid any errors. The turn-on and turn-off switching losses at two temperatures and blocking voltage of 400 VDC are presented in Fig. 11c and Fig. 11f respectively. It can be observed that increase in switching speed has resulted in significant reduction in losses. In the past literature, dynamic characterization of GaN HEMTs has only been reported until 133 K [47], [66], and loss analysis below this temperature is being reported for the first time.

3) Summary and Details of Components for CPEC Subsystems

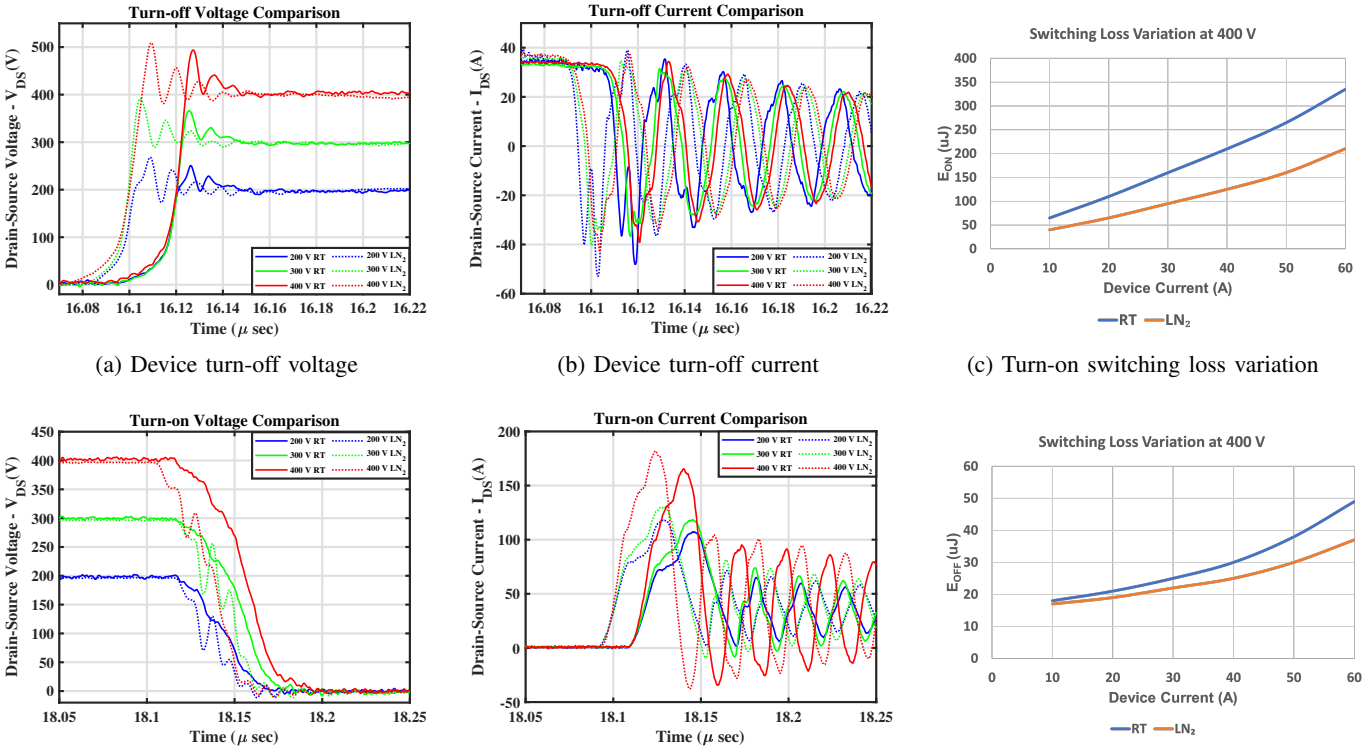
As observed from the results presented, designed GD does not only work at extreme low temperatures e.g., LN_2, but also controls the switching device quite amicably since no mis-triggering, and/or jittering was observed during the DPT tests conducted. Therefore, the proposed GD can successfully be employed in future device characterization, as well as CPEC systems. Details about the important components used in GD and DPT board are presented in Table IV.

IV. Fully CPEC Design, Integration and Demonstration

This section of the paper focuses at designing and demonstrating a 2L-CSI inverter for cryogenic applications. The choice of topology has been primarily dictated by advantages in terms of lower volume, better source and load side power quality, and lower magnitudes of conducted EMI as presented in section II. For a 2L-CSI, the advantage in volume is influenced by air-core inductors using superconductor materials, whereas better source and load side power quality affects the operation and performance of superconducting transmission lines, and machines respectively.

A. Design of a Three Phase 2L-CSI CPEC

A three phase current source inverter of 20 kVA with an output voltage of 300 V_{LL-RMS} has been designed in this paper. Since device blocking voltage for current source inverter



(a) Device turn-off voltage (b) Device turn-off current (c) Turn-on switching loss variation

(d) Device turn-on voltage (e) Device turn-on current (f) Turn-off switching loss variation

Fig. 11: RT and LN_2 comparison of switching device

Table IV: Details of components used in finalized design

Component	Part Number	Specification
Gate Driving ICs	Silicon Labs Si8271	200 $V/nsec$ CMTI
	Analog Devices ADuM4221	150 $V/nsec$ CMTI
Buffer IC	Texas Instruments ISO7820x	CMOS
Auxiliary Power Supply	Recom Power RV-0509S	5 to 9 V converter
Common Mode Choke	Würth Elektronik 7448011008	
Decoupling Capacitors	NP0 or X5R	Numerous voltage levels
Resistors	Thin Film	Least temperature coefficient
Zener Diodes	SMAZ6V2-13-F, DDZ9685-7	1 W, 0.5 W
Solder Paste	Sn42/Bi57.6/Ag0.4	
DC link capacitor	MKP1848C62580JP4	Polypropylene
GaN switches	GS66516T	650 V, 60 A

is dictated by peak of output voltage, output voltage of 300 V was selected as limited by availability of commercially available discrete devices, suitable for cryogenic applications.

1) Selection of Semiconductor Device for 2L-CSI

Based upon the device characterization results reported in literature [13]–[17], only Si MOSFET and GaN HEMT show better performance towards CT. Therefore GaN based discrete device, GS66516T, is used for the analysis. This device is the highest voltage and current rating commercially available GaN product (till the date of publication), that also has been characterized to perform better at reduced temperatures [62]. Furthermore, its dynamic characterization at LN_2 was performed for the first time in section III as shown in Fig. 11. Since a 2L-CSI needs a bi-directional current and RVB switch, two devices were connected in anti-series configuration known as common source (CS) configuration. CS is simple to configure with commercially available GDs, hence reduced gate driving complexities, and bi-directional current carrying capability [67], whereas it has similar semiconductor losses as common drain (CD) configuration. However, a monolithic CD bi-directional switching device can be designed to have the same on-state resistance as a standard switch [68].

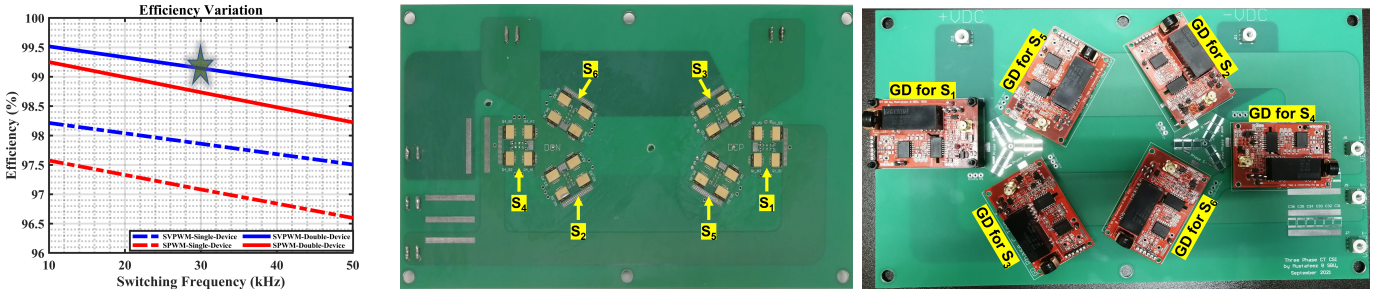
In order to optimize the performance, a parametric sweep with frequency, device number and modulation technique was conducted for CS configuration using [69]. A combination of minimum of two devices per position results in efficiencies above 99 % with SVM as shown in Fig. 12a. Therefore, two devices were paralleled per switching position in the converter layout to achieve 99+ % efficiencies, while the switching frequency was limited to be 30 kHz to fulfill the minimum power efficiency at RT.

2) Power Loop Design and Optimization for 2L-CSI

Considering the sensitivity of GaN devices to converter layout and parasitics involved, switching cell of 2L-CSI needs to be optimized as it affects the transient voltages and device performance [70]. Furthermore, power loop inductance of all three cells should be symmetrical to reduce the circulating currents. In order to fulfill both the objectives, all the switching cells were placed on a "Y" shape configuration whereas vertical power loop placement was used to reduce the board inductance. A six layer PCB containing devices on the bottom side and decoupling capacitors on top side was designed where forward current was distributed in even layers while return path was provided by the odd layers. This type of configuration resulted in maximum cancellation of flux, hence an optimized power loop inductance alongside reduced common source inductance (CSI) was achieved for better operating performance. To validate the concept, the layout was exported into Ansys Q3D and parasitics analysis was performed. The power loop inductance between switching cells "S1-S3", "S3-S5" and "S5-S1" was found not only to be symmetrical, but also resulted in the least of inductance of 3.85 nH reported for any CSI. The designed PCB with switching devices soldered is shown in Fig. 12b where switch numbering is similar to Fig. 5c.

3) Selection of Passive Components for 2L-CSI

For a 2L-CSI, primarily two types of passive components are involved: DC link storage inductor L_{DC} and output filter



(a) Selection of device number and modulation technique

(b) Bottom side of power board containing GaN devices

(c) Top side of power board containing GD daughter boards

Fig. 12: 2L-CSI converter design and development

capacitor C, as labelled in Fig. 1c. For the DC link inductor, design of an air-core inductor was considered using superconducting magnetic tape YBCO, whereas PPS capacitors by Vishay were used in design.

4) Converter Layout Considerations

Having successfully characterized the switching device and GD, the designed subsystems were employed for the design of whole converter. Three phase inverter was envisioned to be decomposed into: (a) Power board, containing switching devices, (b) Six gate driver boards, containing cryo compatible components, and (c) Filter capacitor board, containing output filter capacitor. Considering the bi-directional RVB switches to be in CS configuration as shown in Fig. 5c, the overall converter structure requires six dual channel GD boards. It is worth mentioning that GD board with IC ADuM4221 can be used to drive two channels independently, therefore the same GD board has the feature to control two CS configured switching devices. Furthermore, all the boards have been configured to be identical, so they can replace each other in DPT board or power board. The assembled power board alongside GD daughter boards is presented in Fig. 12c.

B. Room Temperature Testing of 2L-CSI

In order to carry out testing of whole inverter, all the boards mentioned were populated with respective components, and tested individually, whereas collective testing was carried out as per following sequence.

1) Double Pulse Evaluation of Switching Cells

Before carrying out the inverter testing, DPT was performed on all switching cells as identified in [71] under rated conditions. Since two 60 A devices are paralleled per position, peak current of 120 A must be pushed at rated voltage. This not only helps in characterizing the power loop inductance, but information about collective switching losses and gate driving capability were also analyzed. For the accuracy of measurements, passive probe TPP0850 of 800 MHz bandwidth and 1000 V was used for measuring device voltage, whereas rogowski coil TRCP0600 was used for load current measurement. As seen from Fig. 13a, a peak load current of around 102 A was pushed at 395 V, whereas Fig. 13b shows the ringing frequency of device voltage to be 138 MHz. Considering C_{oss} of 135 pF at 400 V, the power loop inductance can be calculated to be 5.2781 nH which fairly agrees to the Ansys Q3D extracted value. The relatively higher measured value of inductance is related to additional inductance being introduced by the packages of four pair of GaN devices in a switching loop [72]. Similar DPTs were extended to all six switching cells to ensure the switching performance is not only identical, but there also is no influence on non-switching devices.

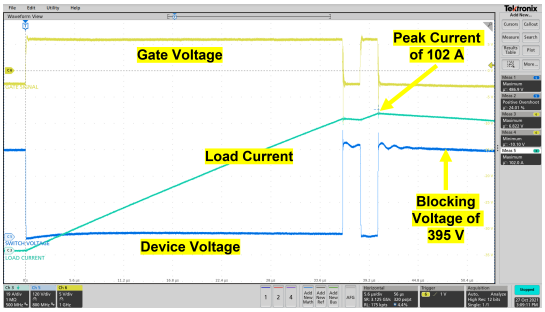
2) Integrated Testing of 2L-CSI

Having performed the DPT on all the switching loops, whole inverter setup was integrated as shown in Fig. 14a. For the evaluation of inverter, a 391 μH MPP core inductor was utilized as DC link energy storage (because of non-operation of superconductors at RT). The converter feeding a three phase resistive load was driven by a laboratory power supply. In order to test the converter continuously under higher operating voltages, a commercially available heat-sink was utilized to keep the devices under safe operating temperatures.

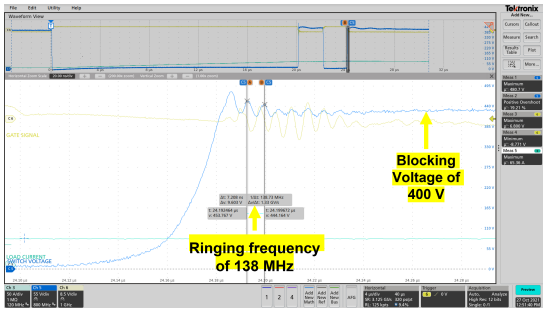
A three phase unified SVM was utilized as a modulation technique [73], whereas a cyclone IV field-programmable gate array (FPGA) was used for the generation of twelve PWM signals. For the safe transition of current from phase-phase, an overlap time of 650 nsec was configured amongst the alternate phases. Similarly a delay time of 1.3 μsec between two switches of all the CS configurations was established to ensure a uni-directional current flow during the commutation process, hence preventing phase-phase short circuit across output capacitors [74]. Using the switch convention shown in Fig. 5c, the PWM for a CS configuration has been divided into top and bottom switch and is shown in 14b. Integrating the system together, the inverter was run continuously at DC link voltage of 62 V, whereas V_{LL-RMS} of 110 V was recorded. The three phase output voltage, switch node and input DC link voltage, and inductor current are presented in Fig. 15a and 15b. Additionally, converter output voltages, input DC link voltage and DC link current during start-up has also been recorded in Fig. 15c. It is worth mentioning that testing a CSI is different from VSI as most of the commercially available power supplies can be high voltage but not high current. Therefore, testing a CSI ideally requires a constant current supply which is uncommon. This limitation restricts rated voltage testing of the designed converter as it requires a current supply capable of delivering $\sim$ 75 A.

C. Development of Superconducting Inductor

To demonstrate a superconducting inductor, L_{DC} was assumed to be split into two equal inductors (12.5 μH each), as

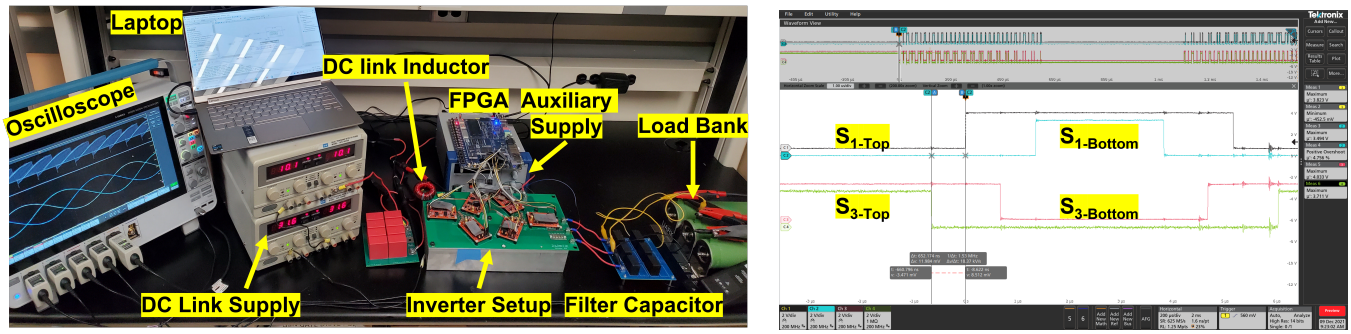


(a) DPT on a switching cell with two paralleled devices



(b) Ringing frequency of device voltage

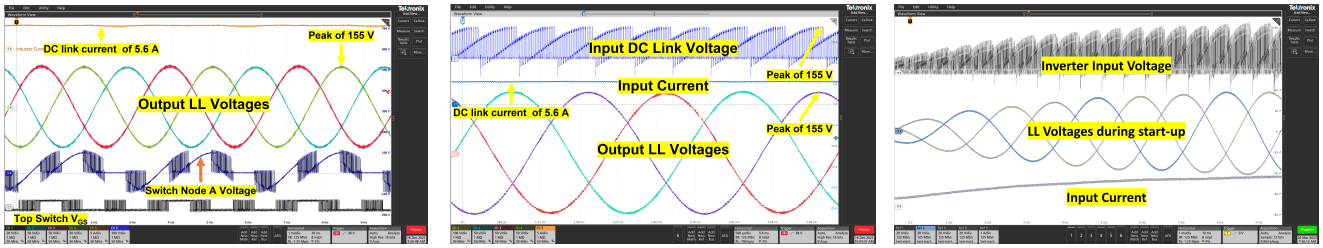
Fig. 13: Characterization of CS configured switching cell with two paralleled devices



(a) Whole inverter setup

(b) PWM generation for top and bottom switches for a CS configuration

Fig. 14: 2L-CSI converter setup and PWM waveform



(a) Converter switch node voltage and DC link current

(b) Converter output and DC link voltage

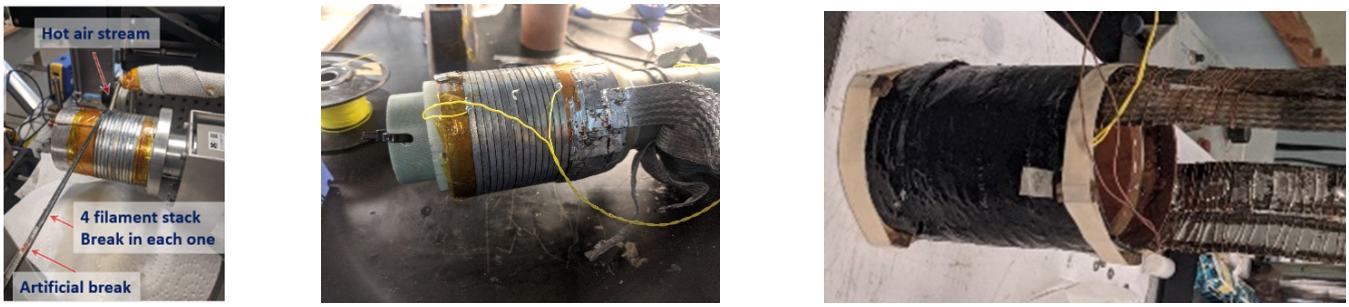
(c) Converter response during start-up

Fig. 15: Test results of inverter at RT

shown in Fig. 5c. A copper tube of 3.93 inch (10 cm) outer diameter was selected to prototype the initial version of inductor. The tube was cut in half, lengthwise and crosswise to avoid the superconducting current shunting. For the superconducting cable, 2 mm wide exfoliated YBCO coupons manufactured from a standard second-generation tape supplied by American Superconductor Corp were used [75]. The exfoliated tapes, initially 10 mm wide, were sliced into 2 mm wide filaments by a fiber laser (STI 80 W model). The filament can be described as a 1.2 mm thick YBCO layer attached to 75 mm thick copper foil. For inductor forming, 14 turn single-layer coil was accomplished resulting in measured inductance of 13 μH with bode 100 vector network analyzer. It can be realized that inductor value matched well with the designed value (12.5 μH each), and two such inductors can be put in positive and negative of DC link supply to make a current source configuration. The process of winding the coil has been shown in Fig. 16a, whereas Fig. 16b, shows a wound coil with voltage drop sensing leads. The finished coil was vacuum impregnated with Stycast 2850FL epoxy, as shown in Fig. 16c to have good thermal conduction. The inductor developed was successfully tested at 77 K for a minimum current of 600 A, and thus can successfully be employed for converter applications.

D. Cryogenic Temperature Testing

With the cryogenic converter setup illustrated in Fig. 17, converter tests were repeated under similar conditions as of RT. For the experimentation, a Styrofoam bucket was used to contain LN_2 in which output filter capacitor, and heat-sink were submerged. Switching devices of the power stage were mounted onto heat-sink through a silicone elastomer thermal insulating material (TIM). While operating the inverter at similar input and load conditions, the overall inverter efficiency was measured to be increasing by 0.3 % which is expected



(a) Coil winding process

(b) Wound coil with voltage drop sense leads

(c) Test coil after epxoy impregnation and mounting current leads

Fig. 16: Development of superconducting inductor

to improve when % loading increases. Using the efficiency

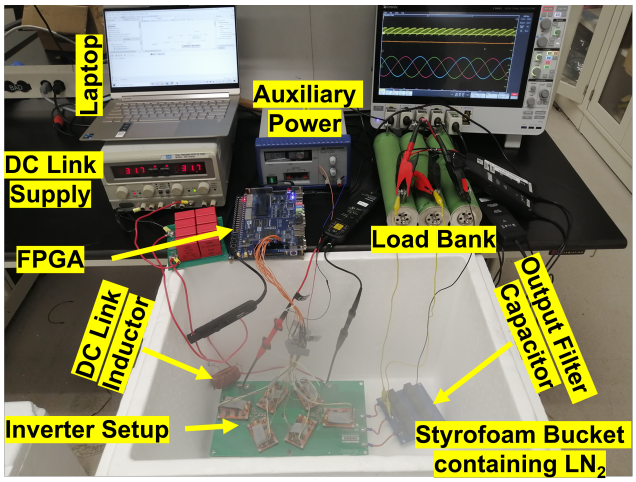


Fig. 17: Cryogenic setup of inverter

measurements, the actual device junction temperature can be estimated using thermal resistances of all the series interconnects: R_{th-js}, R_{th-tim} and R_{th-sa}. By utilizing the manufacturer provided values, device junction temperature under these conditions was calculated to be $\sim$ 82.34 K. It is worth mentioning that whole inverter, including GD board, DC link inductor and output filter capacitor were not completely immersed inside LN_2. This was deliberately done as otherwise the process of debugging and taking measurements would have been extremely difficult. The difficulty is associated in draining and re-pouring of LN_2 back and fourth into the Styrofoam bucket while the converter components are already dipped inside. Furthermore, after every alternate cycle of RT and LN_2 exposure, the converter components go through excessive icing, and de-icing, which can lead to short circuits of components if not properly attended, but also takes lots of time to dry up.

E. Discussion on Converter Performance at RT and CT

A three phase 2L-CSI was developed and tested successfully at RT and CT with similar source and load conditions. An efficiency improvement of 0.7 % was observed at load demand of 300 W. Although the idea of utilizing COTS components for a fully cryogenic converter was implemented, numerous challenges and avenues need to be addressed. Fom the experience of working with LN_2, it was realized that either cryo-chambers, or cold plate (carrying liquid cryogen) must be designed for testing a cryogenic system. Such a setup will not only ensure reliable connections of components, easy measurements and debugging, but will also be critical from the perspective of safety. Therefore, proper design and sizing of cooling mechanisms must be considered in further development of cryogenic converters.

V. Discussion on Challenges in Developing CPEC

Although CPEC systems are expected to offer better efficiency and density, development of fully cryogenic converter systems is in the initial phases, and needs lots of development and experimental characterization. The advantages associated with cryogenic operating temperatures brings attraction, but also poses numerous challenges which should be considered. Based upon the experience in designing a cryogenic converter, a few of them are summarized here.

A. Device Selection for CPEC

Amongst the active switching devices, Si devices have been shown to offer improved performance at CT, and are also available in abundance, yet the reduction in device blocking voltage limits the device operating voltage. On the contrary, even though GaN HEMTS amongst WBG devices have shown better performance in all the variables of interest, still the highest voltage COTS device characterized for CT is limited to 650 V only [76]. Considering this limit on device voltage, series cascading of devices can be a possible solution but it leads to numerous other challenges. A few of them include a larger power loop, asymmetrical dynamic performance of devices, and complex gate driving circuitry. Therefore, development of CPEC systems is limited to lower voltages until suitability of higher voltage GaN devices gets proven for cryogenic applications.

B. Uncertainty in Operation of ICs and APS at CT

One of the biggest challenge is availability and development of CT compatible gate driver circuitry. Since the GD boards themselves need numerous components, careful selection and characterization of all the individual building elements must be given thorough consideration. The first and foremost challenge is to find CMOS ICs, where most of them either work on BiCMOS, DMOS or other technologies. Furthermore, its very difficult to know which fabrication process and technology was used in IC manufacturing as its not so commonly available in device data-sheet. Therefore, the only possible way of finding the correct option is by carrying out rigorous testing and evaluation.

Having found a CMOS IC is only halfway through the solution, as few ICs can possibly under perform, or may not work at all for the intended CT operation. A similar experience is put down to elaborate the difference. From authors' experience, it was observed that not all the similar components perform well at CT. For example, state-of-the-art isolated gate driver Si8271 was found to be working until 120 K in [47], whereas it was observed to be working till 133 K in [66] and [60]. During the characterization of GD ICs, similar experiences were encountered by the authors. Upon replacing and re-characterizing, every other Si8271 IC gives the opportunity to be workable as low as LN_2 temperature. On the contrary, the other GD ADuM4221 and buffer IC ISO7820x were found to be operational most of the times.

Similar characterization issues occurred with APS RV-0509S as it has been found to malfunction sometimes. One of the approaches followed by authors was doing its individual characterization at CT for atleast three times for extended duration of time spanning from 6-8 hours. While characterizing is important, test conditions should also be extended to numerous load conditions, with and without exposing to cold start operation. This kind of characterization approach helped

authors find the APS which can work together with GD boards constituting a full three phase converter.

C. Inaccurate Temperature Assessment

Another challenge is inaccurate assessment of temperature, particularly with conduction cooled cryogenic chambers. From the experimentation, it was found that if any of the component is left uncovered by epoxy coating, it might not have the same temperature as the actual base-plate of the chamber. This difference in temperature is governed by the power loss inside the equipment under test (EUT) and might be negligible if there is not much heat loss by the EUT. In order to avoid misreading, whole PCB must be fully epoxy hardened to ensure thermal conduction of whole EUT with the base-plate of the chamber. However, this temperature assessment is no more an issue if liquid cryogens are used for cooling purposes; such as utilizing LN_2 dewar maintains 77 K across the whole EUT immersed inside.

D. Challenges in High Voltage Measurements in CT

One of the most important challenge is related to measurement of fast rising/falling high voltage electrical signals at CT. The challenge becomes more critical when the CPEC systems incorporate high switching GaN devices. A typical example of this is measuring a device voltage V_{DS} inside a cryo-chamber or LN_2 dewar. Since not much has been reported on cryogenic measurements, numerous compensation networks were tried but signal shape and integrity was found to be getting lost in this whole process. Finally, jaws of active probe were inserted inside LN_2 dewar to take the measurements, but a better method for this should be researched upon.

However, low voltage signals such as V_{GS} can easily be measured by employing SMA connectors, BNC cables and 50 Ω external terminations. It is worth mentioning that external terminations play an important role by damping the reflection and refraction of waves.

VI. Conclusion and Future Work

In this paper, the design, analysis and operation of a cryogenically cooled 2L-CSI inverter for FEA is presented. The paper emphasized the importance of CPEC systems in FEA, and reviewed the converter design trade-offs for such applications. From the considered parameters like volume, power quality and energy content: a 2L-CSI has been found to be more appropriate while considering superconducting inductors. Therefore, a 20 kVA, 300 V, three phase 2L-CSI with most suitable WBG GaN device has been designed and tested at room and cryogenic temperature. The minimum device junction temperature is estimated to be $\sim$ 82.34 K. The converter was successfully run at V_{LL-RMS} of 110 V at both RT and LN_2 temperature, and an efficiency improvement of 0.7 $\%$ was measured under light load conditions.

As part of converter development, numerous cryogenic subsystems including GD boards and double pulse test (DPT) platforms using COTS components were also developed. Both the boards were integrated and their performance was successfully tested at RT and inside LN_2, 77 K environment. Using the designed subsystems, dynamic characterization of GaN HEMT was performed for the first time where the time delay for turn-off and turn-on was reduced by 100 nsec and 20 nsec respectively. Therefore, overall switching loss reduction of as much as 62 $\%$ was observed at device rated current. The paper also provides complete list of the COTS components which were utilized in the design. Furthermore, a brief discussion about the challenges encountered in the development of cryogenic inverter is also carried out.

As part of future work, converter testing under rated conditions is on-going and results with superconducting inductor will be provided in future publications. Furthermore, the authors would like to extend the testing to even lower temperatures such as $\sim$ 20 K.

Acknowledgement

The authors would like to acknowledge the financial support lended by NASA to carry out this research under ULI: Development of the Cryogenic Hydrogen-Energy Electric Transport Aircraft (CHEETA) Design Concept under award number 80NSSC19M0125. Furthermore, NSF CAREER award numbered 1846917 titled Semiconductor-Based EMI Mitigation Architecture for Future Power Electronics Systems is also acknowledged. The authors would also like to thank Vivian Su, Donald McMahon and Steven Holder for their valuable feedback in finalizing the grammatical structure of the paper.

References

[1] [Online]. Available: https://www.atag.org/facts-figures.html
[2] [Online]. Available: https://www.icao.int/environmental-protection/pages/envreport10.aspx
[3] [Online]. Available: https://www.nasa.gov/sites/default/files/atoms/files/sip-2017-03-23-17-high.pdf
[4] B. Rahrovi and M. Ehsani, "A review of the more electric aircraft power electronics," in *2019 IEEE Texas Power and Energy Conference (TPEC)*, 2019, pp. 1–6.
[5] G. E. Wroblewski and P. J. Ansell, "Mission analysis and emissions for conventional and hybrid-electric commercial transport aircraft," *2018 AIAA Aerospace Sciences Meeting*, 2018.
[6] K. R. Antcliff, M. D. Guynn, T. Marien, D. P. Wells, S. J. Schneider, and M. J. Tong, "Mission analysis and aircraft sizing of a hybrid-electric regional aircraft," *54th AIAA Aerospace Sciences Meeting*, 2016.
[7] C. Friedrich and P. Robertson, "Hybrid-electric propulsion for aircraft," *Journal of Aircraft*, vol. 52, no. 1, p. 176–189, 2015.
[8] C. Pornet, C. Gologan, P. C. Vratny, A. Seitz, O. Schmitz, A. T. Isikveren, and M. Hornung, "Methodology for sizing and performance assessment of hybrid energy aircraft," *Journal of Aircraft*, vol. 52, no. 1, p. 341–352, 2015.
[9] [Online]. Available: https://www.energy.gov/sites/prod/files/2020/12/f81/hfto-h2-airports-workshop-2020-schneider.pdf
[10] [Online]. Available: https://weber.itn.liu.se/~clryd/KURSER/TNK027/Kurslitteratur2011/CRYOPLANE.pdf
[11] [Online]. Available: https://www.energy.gov/sites/default/files/2014/03/f9/thomas_fcev_vs_battery_evs.pdf
[12] K. Rajashekara and B. Akin, "Cryogenic power conversion systems: The next step in the evolution of power electronics technology." *IEEE Electrification Magazine*, vol. 1, no. 2, pp. 64–73, 2013.
[13] ——, "A review of cryogenic power electronics-status and applications," in *2013 International Electric Machines & Drives Conference*. IEEE, 2013, pp. 899–904.
[14] S. Yang, "Cryogenic characteristics of igbts," Ph.D. dissertation, University of Birmingham, 2005.
[15] R. Singh and B. J. Baliga, *Cryogenic operation of silicon power devices*. Springer Science & Business Media, 2012.
[16] C. Jia, "Experimental investigation of semiconductor losses in cryogenic dc-dc converters," Ph.D. dissertation, University of Birmingham, 2008.
[17] H. Gui, R. Chen, J. Niu, Z. Zhang, L. M. Tolbert, F. Wang, B. J. Blalock, D. Costinett, and B. B. Choi, "Review of power electronics components at cryogenic temperatures," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 5144–5156, 2020.

[18] A. Hammoud and E. Overton, "Low temperature characterization of ceramic and film power capacitors," in *Proceedings of Conference on Electrical Insulation and Dielectric Phenomena - CEIDP '96*, vol. 2, 1996, pp. 701–704 vol.2.

[19] R. Patterson, A. Hammond, and S. Gerber, "Evaluation of capacitors at cryogenic temperatures for space applications," in *Conference Record of the 1998 IEEE International Symposium on Electrical Insulation (Cat. No.98CH36239)*, vol. 2, 1998, pp. 468–471 vol.2.

[20] M.-J. Pan, "Performance of capacitors under dc bias at liquid nitrogen temperature," *Cryogenics*, vol. 45, no. 6, pp. 463–467, 2005.

[21] G. Bank and W. Virginia, "Cryogenic measurements of surface mount multi-layer ceramic chip capacitors," 2009.

[22] C. Park, J. Wei, S. Singh, S. Narra, L. Graber, and M. Imperatore, "The characteristics of film capacitors at room temperature and in liquid nitrogen," in *2018 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*. IEEE, 2018, pp. 1–7.

[23] J. Gniewek and E. Ploge, "Cryogenic behavior of selected magnetic materials," *Journal of research of the NBS-Engineering and Instrumentation*, vol. 69, no. 3, pp. 225–236, 1965.

[24] G. F. Dionne, "Properties of ferrites at low temperatures," *Journal of applied physics*, vol. 81, no. 8, pp. 5064–5069, 1997.

[25] T. Pannaparayil, R. Marande, and S. Komarneni, "Magnetic properties of high-density mn-zn ferrites," *Journal of applied physics*, vol. 69, no. 8, pp. 5349–5351, 1991.

[26] S. S. Gerber, "Performance of high-frequency high-flux magnetic cores at cryogenic temperatures," in *IECEC'02. 2002 37th Intersociety Energy Conversion Engineering Conference, 2002.* IEEE, 2002, pp. 249–254.

[27] M. Chen, Y. J. Yu, L. Y. Xiao, Q. L. Wang, W. Chung, K. Kim, and S. Baang, "The magnetic properties of the ferromagnetic materials used for hts transformers at 77 k," *IEEE transactions on applied superconductivity*, vol. 13, no. 2, pp. 2313–2316, 2003.

[28] H. P. Quach and T. C. Chui, "Low temperature magnetic properties of metglas 2714a and its potential use as core material for emi filters," *Cryogenics*, vol. 44, no. 6-8, pp. 445–449, 2004.

[29] J. Claassen, "Inductor design for cryogenic power electronics," *IEEE transactions on applied superconductivity*, vol. 15, no. 2, pp. 2385–2388, 2005.

[30] B. Jankowski, D. Kapelski, M. Karbowiak, M. Przybylski, and B. Ślusarek, "Influence of cryogenic temperature on magnetic properties of soft magnetic composites," *Powder Metallurgy*, vol. 57, no. 2, pp. 155–160, 2014.

[31] O. Azofeifa and C. B. Barth, "Inductor loss estimation of a single phase 3-level gallium nitride inverter under cryogenic conditions," in *2018 IEEE Power and Energy Conference at Illinois (PECI)*. IEEE, 2018, pp. 1–7.

[32] R. Chen, Z. Dong, Z. Zhang, H. Gui, J. Niu, R. Ren, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett *et al.*, "Core characterization and inductor design investigation at low temperature," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2018, pp. 4218–4225.

[33] C. Park, O. Obadolagbonyi, and L. Graber, "Cryogenic power electronics: Capacitors and inductors," in *IOP Conference Series: Materials Science and Engineering*, vol. 756, no. 1. IOP Publishing, 2020, p. 012010.

[34] B. Ray, S. S. Gerber, R. L. Patterson, and I. T. Myers, "Low-temperature operation of a buck dc/dc converter," in *Proceedings of 1995 IEEE Applied Power Electronics Conference and Exposition-APEC'95*, vol. 2. IEEE, 1995, pp. 941–946.

[35] F. F. Perez-Guerrero, B. Ray, and R. L. Patterson, "Low temperature operation of a three-level buck dc-dc converter," in *IECEC-97 Proceedings of the Thirty-Second Intersociety Energy Conversion Engineering Conference (Cat. No. 97CH6203)*, vol. 2. IEEE, 1997, pp. 1415–1420.

[36] F. Perez-Guerrero, K. Venkatesan, B. Ray, and R. Patterson, "Low temperature performance of a closed loop three level buck converter," in *Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99 (Cat. No. 99TH8475)*, vol. 1. IEEE, 1999, pp. 58–62.

[37] C. Jia and A. Forsyth, "Evaluation of semiconductor losses in cryogenic dc-dc converters," in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, vol. 2. IEEE, 2006, pp. 1–5.

[38] J. Bourne, R. Schupbach, B. Hollosi, J. Di, A. Lostetter, and H. A. Mantooth, "Ultra-wide temperature (-230 c to 130 c) dc-motor drive with sige asynchronous controller," in *2008 IEEE Aerospace Conference*. IEEE, 2008, pp. 1–15.

[39] J. Garrett, R. Schupbach, A. B. Lostetter, and H. A. Mantooth, "Development of a dc motor drive for extreme cold environments," in *2007 IEEE Aerospace Conference*. IEEE, 2007, pp. 1–12.

[40] B. Ray and R. L. Patterson, "Wide temperature operation of a pwm dc-dc convertor," in *IAS'95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, vol. 2. IEEE, 1995, pp. 971–976.

[41] B. Ray, S. S. Gerber, R. L. Patterson, and J. E. Dickman, "Low temperature performance of a boost converter with mpp and hts inductors," in *Proceedings of Applied Power Electronics Conference. APEC'96*, vol. 2. IEEE, 1996, pp. 883–888.

[42] H. Li, D. Liu, and C. A. Luongo, "Investigation of potential benefits of mosfets hard-switching and soft-switching converters at cryogenic temperature," *IEEE transactions on applied superconductivity*, vol. 15, no. 2, pp. 2376–2380, 2005.

[43] X. Y. Chen, J. X. Jin, M. G. Tang, J. Feng, H. Y. Luo, L. Y. Li, Q. Xu, and H. L. Zou, "An efficient boost chopper integrated with cryogenic mosfets and hts inductor," *IEEE Transactions on Applied Superconductivity*, vol. 26, no. 7, pp. 1–6, 2016.

[44] H. Gui, Z. Zhang, R. Chen, R. Ren, J. Niu, H. Li, Z. Dong, C. Timms, F. Wang, L. M. Tolbert, B. J. Blalock, D. Costinett, and B. B. Choi, "Development of high-power high switching frequency cryogenically cooled inverter for aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5670–5682, 2020.

[45] C. B. Barth, T. Foulkes, O. Azofeifa, J. Colmenares, K. Coulson, N. Miljkovic, and R. C. N. Pilawa-Podgurski, "Design, operation, and loss characterization of a 1-kw gan-based three-level converter at cryogenic temperatures," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 040–12 052, 2020.

[46] C. Barth, J. Colmenares, T. Foulkes, K. Coulson, J. Sotelo, T. Modeer, N. Miljkovic, and R. C. Pilawa-Podgurski, "Experimental evaluation of a 1 kw, single-phase, 3-level gallium nitride inverter in extreme cold environment," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 717–723.

[47] R. Chen and F. F. Wang, "Sic and gan devices with cryogenic cooling," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 315–326, 2021.

[48] N. Madavan, "A nasa perspective on electric propulsion technologies for large commercial aircraft," in *International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles and the International Transportation Electrification Conference (ESARS-ITEC)*, no. ARC-E-DAA-TN37026, 2016.

[49] P. Karutz, S. Round, M. Heldwein, and J. Kolar, "Ultra compact three-phase pwm rectifier," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, 2007, pp. 816–822.

[50] M. Rashid, *Power electronics handbook: devices, circuits, and applications, ser*. Academic Press. Elsevier, 2010.

[51] R. Lai, F. Wang, R. Burgos, Y. Pei, D. Boroyevich, B. Wang, T. A. Lipo, V. D. Immanuel, and K. J. Karimi, "A systematic topology evaluation methodology for high-density three-phase pwm ac-ac converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2665–2680, 2008.

[52] A. M. Hava, U. Ayhan, and V. V. Aban, "A dc bus capacitor design method for various inverter applications," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4592–4599.

[53] H. Dai and T. M. Jahns, "Comparative investigation of pwm current-source inverters for future machine drives using high-frequency wide-bandgap power switches," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2601–2608.

[54] M. Corduan, M. Boll, R. Bause, M. P. Oomen, M. Filipenko, and M. Noe, "Topology comparison of superconducting ac machines for hybrid electric aircraft," *IEEE Transactions on Applied Superconductivity*, vol. 30, no. 2, pp. 1–10, 2020.

[55] C. W. T. McLyman, *Transformer and inductor design handbook*. Dekker New York,, USA, 1988.

[56] [Online]. Available: https://www.wima.de/wp-content/uploads/media/e_WIMA_DC_Link_MKP_4.pdf

[57] M. ul Hassan, A. I. Emon, H. Peng, C. Kushan, and F. Luo, "Investigation on conducted emi for single and parallel connected inverters," in *2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021, pp. 1–6.

[58] M. Zdanowski, K. Kostov, J. Rabkowski, R. Barlik, and H.-P. Nee, "Design and evaluation of reduced self-capacitance inductor in dc/dc converters with fast-switching sic transistors," *IEEE transactions on power electronics*, vol. 29, no. 5, pp. 2492–2499, 2013.

[59] C. Kuring, O. Hilt, J. Böcker, M. Wolf, S. Dieckerhoff, and J. Würfl, "Novel monolithically integrated bidirectional gan hemt," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 876–883.

[60] Y. Wei, M. M. Hossain, R. Sweeting, and A. Mantooth, "Functionality and performance evaluation of gate drivers under cryogenic temperature," in *2021 IEEE Aerospace Conference (50100)*, 2021, pp. 1–9.
[61] E. A. Jones, "Review and characterization of gallium nitride power devices," 2016.
[62] R. Ren, H. Gui, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, D. Costinett, B. J. Blalock, and B. B. Choi, "Characterization and failure analysis of 650-v enhancement-mode gan hemt for cryogenically cooled power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 66–76, 2020.
[63] R. Singh and B. Baliga, "Cryogenic operation of power bipolar transistors," in *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics*, 1994, pp. 243–248.
[64] W. Clark, B. El-Kareh, R. Pires, S. Titcomb, and R. Anderson, "Low temperature cmos-a brief review," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 3, pp. 397–404, 1992.
[65] [Online]. Available: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_application/application_notes/gfm347/GFM347_1e_Double_Pulse_Testing.pdf
[66] R. Ren, H. Gui, Z. Zhang, R. Chen, J. Niu, F. Wang, L. M. Tolbert, D. Costinett, B. J. Blalock, and B. B. Choi, "Characterization and failure analysis of 650-v enhancement-mode gan hemt for cryogenically cooled power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 66–76, 2019.
[67] T. Friedli, S. D. Round, D. Hassler, and J. W. Kolar, "Design and performance of a 200-khz all-sic jfet current dc-link back-to-back converter," *IEEE Transactions on Industry Applications*, vol. 45, no. 5, pp. 1868–1878, 2009.
[68] H. Dai, R. A. Torres, T. M. Jahns, and B. Sarlioglu, "An h8 current-source inverter using wide bandgap bidirectional switches," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2019, pp. 2361–2368.
[69] M. ul Hassan, Z. Yuan, A. I. Emon, and F. Luo, "A framework for high density converter electrical-thermal-mechanical co-design and co-optimization for mea application," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 3120–3125.
[70] L. G. A. Rodrigues, G. Lefèvre, J. Martin, and J.-P. Ferrieux, "Switching cell design optimization of sic-based power modules for current source inverter applications," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1–P.10.
[71] J. Martin, A. Bier, S. Catellani, L. G. Alves-Rodrigues, and F. Barruel, "A high efficiency 5.3 kw current source inverter (csi) prototype using 1.2 kv silicon carbide (sic) bi-directional voltage switches in hard switching," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2016, pp. 1–8.
[72] M. Valente, F. Iannuzzo, Y. Yang, and E. Gurpinar, "Performance analysis of a single-phase gan-based 3l-anpc inverter for photovoltaic applications," in *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, 2018, pp. 1–8.
[73] Q. Lei, B. Wang, and F. Peng, "Unified space vector pwm control for current source inverter," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4696–4702.
[74] H. Dai, R. A. Torres, T. M. Jahns, and B. Sarlioglu, "Characterization and implementation of hybrid reverse-voltage-blocking and bidirectional switches using wbg devices in emerging motor drive applications," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 297–304.
[75] V. Solovyov and P. Farrell, "Exfoliated ybco filaments for second-generation superconducting cable," *Superconductor Science and Technology*, vol. 30, no. 1, p. 014006, 2016.
[76] Z. Zhang, H. Gui, R. Ren, F. Wang, L. M. Tolbert, D. J. Costinett, and B. J. Blalock, "Characterization of wide bandgap semiconductor devices for cryogenically-cooled power electronics in aircraft applications," in *2018 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*. IEEE, 2018, pp. 1–8.

Mustafeez-ul-Hassan (Graduate Student Member, IEEE) received his B.Sc and M.Sc in electrical engineering from University of Engineering and Technology, Lahore, Pakistan, in 2013 and 2017 respectively. He is currently a third year Ph.D. student at Stony Brook University (SUNY Stony Brook), Stony Brook, NY, USA. His research interests include design of DC-AC and DC-DC converters using modern Wide Band Gap (WBG) devices for high frequency and high-power density converters for cryogenically cooled aircraft applications. He is holding a prestigious Fulbright scholarship and faculty development program (FDP) by higher education commission (HEC), Pakistan for his higher education.

Asif Imran Emon (Graduate Student Member, IEEE) received his B.Sc. in Electrical and Electronic Engineering from Chittagong University of Engineering and Technology (CUET) in 2015. He received his M.S in 2020 from University of Arkansas, Fayetteville, Arkansas, USA with a concentration in high-density power electronics packaging. He was an Intern at GE Global Research, Niskayuna, NY during the summer of 2021 and at Apple Inc., Cupertino, CA in 2022 for 07 months. He is currently a Ph.D. student at Stony Brook University (SUNY Stony Brook), Stony Brook, NY, USA. His research interests include power module packaging of wide band-gap devices, efficient energy conversion and electromagnetic interference and compatibility analysis in motor Drive.

Fang Luo (Senior Member, IEEE) received the bachelor's and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, and jointly from Virginia Tech, Blacksburg, VA, USA, in 2003 and 2010, respectively, He is an Empire Innovation Associate Professor and the Director with Spellman High Voltage Laboratory, Stony Brook University (SUNY Stony Brook), Stony Brook, NY, USA, with his background in power electronics. He was an Assistant Professor with Electrical Engineering Department, University of Arkansas, Fayetteville, AR, USA, from 2017 to 2020, and a Research Assistant Professor with the Ohio State University, Columbus, OH, USA, from 2014 to 2017. He was a Visiting Ph.D. Student from 2007 to 2010, and then a Postdoctoral Researcher from 2010 to 2014, both with Virginia Tech. His research interests include high power-density converter design, high-density EMI filter design and integration, and power module packaging/integration for wide band-gap devices. Dr. Luo is a member of AIAA and ASME. He was the recipient of the NSF CAREER Award.

Vyacheslav Solovyov received the Master's of Science in Solid State Physics from Moscow Institute for Physics and Technology in 1989, and Ph.D. in Solid State Physics from Kiev Institute for Metal Physics in 1995. In 1997 he joined Brookhaven National Laboratory as a research scientist. In 2015 he joined Brookhaven Technology Group, a private company. He is a co-author of 69 peer-reviewed publications. He is a receiver of 2015 RD 100 Award R, "Active superconducting fault current limiter". His research interests included application of high-temperature superconductivity for power and energy markets.