1200 V/650 V/160 A SiC+Si IGBT 3L Hybrid T-Type NPC Power Module With Enhanced EMI Shielding

Asif Imran Emon, Zhao Yuan, Abdul Basit Mirza, Amol Deshpande, Mustafeez Ul Hassan, and Fang Luo

***Abstract*—Three-level (3L) inverters suffer from higher parasitic inductance due to the increased number of series-connected switches in a single current commutation loop (CCL) results in a larger size of CCL compared to their two-level (2L) counterparts. As such, semiconductors are subjected to higher voltage stress and severe ringing at the switching transient. While silicon carbide's (SiC) faster switching speed improves overall efficiency by reducing switching loss, the faster voltage, and current gradient (dv/dt and di/dt) generate electromagnetic interference (EMI) noise, requiring a larger and complicated filter stage design. To solve this problem, an optimized 3L T-type neutral point clamped power module has been proposed with a hybrid combination of the switch (SiC MOSFET + Si IGBT) rated for 1200 V/160 A. Two direct bonded copper (DBC) substrates have been stacked to have a vertical power loop using laser-drilled vias, which provides low commutation loop inductance as low as 4.6 nH for the major CCLs including the wire bond. Other associated CCLs have also been identified and optimized. Additional DBC in the package will be acting as an EMI shield. The EMI noise has been compared to a traditional power module and a 21 dB reduction of common-mode noise has been observed.**

***Index Terms*—Electromagnetic interference (EMI) shielding, hybrid power module, Three-level (3L) T-type neutral point clamped (NPC).**

I. Introduction

THREE-LEVEL (3L), T-type neutral point clamped (NPC) topology is getting attention in renewable energy generation application, high-speed motor drives, and hybrid turbo-electric aircraft propulsion system [1]–[3]. 3L converters are more desirable than 2L converters as they come with higher converter efficiency, lesser voltage stress in device, lower total harmonic distortion, resulting in lower total harmonic machine loss and reduced input and output filter requirement [4]. Moreover, it has been shown in the literature that, 3L T-type NPC topology provides maximum efficiency and lower cost compared to other 3L topologies such as 3L NPC, 3L active NPC, and 3L flying capacitor topology in certain range of operating condition due to its low switch count, lesser number of isolated gate driver requirements, and simple operation principle [5], [6]. Due to improved material properties offered by wide bandgap (WBG) devices such as silicon carbide (SiC), lowering the dimension of die size and high-speed switching has become possible resulting in lower switching loss [7]. As the switching loss is optimized, the switching frequency can be pushed around hundreds of kHz. As SiC MOSFETs enable higher efficiency than Si IGBTs in power converters due to their fast switching ability, the overall increased efficiency of the inverter can be achieved [8]. However, the state-of-the-art die dimension and cost of the SiC is the bottleneck for high power application. To block higher voltage with tolerable leakage current, the length of the drift region of the transistors needs to be increased which incurs additional ON-state resistance. To achieve the capability of pumping high current through the transistor chip, the area of the die increases [9]. To address this issue, a hybrid switch, composed of SiC and Si IGBT by adjusting their gating sequence has been proposed [17] and the concept is demonstrated for T-type NPC topology. In this configuration, lower switching loss from SiC and lower conduction loss from IGBT can be achieved at the same time by soft switching the Si IGBT by controlling the gating sequence. However, due to the long tail current in IGBT during turn OFF, the hybrid switch is limited by the minimum duty cycle and maximum switching frequency constrain. Current ratio between Si and SiC also needs to be optimized to ensure the integrity of the hard switching SiC device. In addition to that, it involves system complexity in gate driver design and power loop optimization during the layout [10].

Hence, to reduce the system complexity, the hybrid switch concept is modified and a new switch combination comprises Si IGBT, SiC MOSFET Schottky diode is proposed as shown in Fig. 2. Si IGBTs with SiC Schottky diode constitute the clamping leg and SiC MOSFETs are placed in the half-bridge position. IGBT's in the clamping leg will be soft switching under the unity power factor; hence, the introduction of Si IGBT will not contribute to additional switching loss [11].

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Asif Imran Emon, Abdul Basit Mirza, and Fang Luo are with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY 11794 USA (e-mail: asifimran.emon@stonybrook.edu; abdulbasit.mirza@stonybrook.edu; fang.luo@stonybrook.edu).

Zhao Yuan is with the ELEG, University of Arkansas Fayetteville, Fayetteville, AR 72701 USA (e-mail: zhaoyuan@uark.edu).

Amol Deshpande is with the Department of Electrical Engineering, University of Arkansas Fayetteville, Fayetteville, AR 72701 USA (e-mail: ardeshpa@uark.edu).

Mustafeez Ul Hassan is with the Stony Brook University, Stony Brook, NY 11794 USA (e-mail: mustafeez.hassan@stonybrook.edu).

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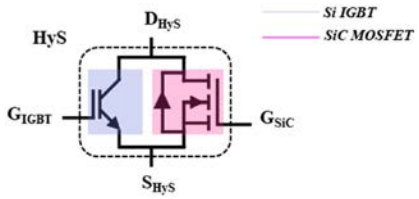

Fig. 1. Hybrid switch structure [9].

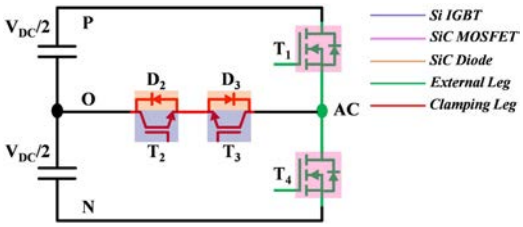

Fig. 2. Hybrid combination of the switch in T-type NPC topology.

Despite having the capacity to achieve faster switching speed, the layout of the power stage and device package itself impedes fully harnessing the advantage offered by the WBG devices due to the associated parasitics [12]–[14]. In high-speed switching transient, the device suffers from excessive voltage stress from voltage overshoot, which harms the reliability of the system and curtails overall lifetime [15]. Evaluation of the commutation loop in the particular topology and optimization of layout accordingly can reduce the parasitics and electromagnetic interference (EMI) noise despite using traditional packaging technology [16], [17]. P-cell, N-cell concept brought a substantial improvement in optimizing half-bridge phase leg topology, where switches constituting the commutation loop placed adjacent to each other to reduce the loop area [18]. Utilizing the same concept, Wang *et al.* introduced symmetrical power loop design using a "double-ended source" busbar structure [19] in a 15 kW multichip SiC module. It reduced the circulating current, and improved the dynamic current sharing among paralleled die in a two-dimensional (2-D) power loop on single direct bonded copper (DBC) substrate. To further reduce the loop inductance, hybrid-packaging structure (PCB+DBC or DBC+DBC) has been proposed [20], [21]. Semiconductor chips are attached in the DBC while the additional PCB constitutes a vertical or 3-D power loop. Vertical power loop enables mutual cancellation of magnetic flux and brings a substantial reduction in commutation loop inductance, reported as low as 3.3 nH. X. Lyu *et al.* demonstrated vertical power loop concept using a single DBC substrate achieving 1.1 nH. Through hole vias in the DBC substrate enabled the implementation of vertical power loop. To isolate the bottom copper from the heatsink, thermal interface material has been used which curtails the thermal performance of the module [22]. A similar concept has been demonstrated by Dutta *et al.* using multiple DBCs with spring-loaded interconnect in LTCC interposer [23].

All these reported works were done for packaging half-bridge phase leg only. Cree has its common source module, which is widely used with their half-bridge phase leg to constitute 3L T-type NPC that involves a complex busbar design due to optimization of multiple loops and interaction between the loops through coupling [24], [25]. Here, in addition to the module parasitics, busbar inductance is also added to the power loop. The lowest 3L T-type NPC busbar inductance reported in the literature is 11 nH without including module inductance [26]. Hence, there is a demand of packaging the topology itself in single module.

In commercial space, Infineon, Onsemi, Semikron, Vincotech, and Microsemi have their individual T-type NPC module with 2-D power loop. Infineon's T-type NPC module comes in "EconoPACK" and press-fit type "Easy 2B/1B" package [27]. Onsemi's 1200 V rated T-type NPC IGBT module comes in their Q0 and Q2 pack with press-fit pins [28]. Semikrons has commercialized its 3L T-type NPC module in the "Semix5p" package for 1200 and 1700 V applications [29]. Microsemi has brought their 3L T-type NPC IGBT module in its press-fit "SP3F" package for 1200 V applications [30]. Vincotech's T-type NPC module is rated for 600/1200 V application and packaged in their press-fit "Flow" package and PCB/DBC hybrid "X4" package [31]. All the reported packages from commercial space are the modification of their pre-existing half-bridge phase leg packages and the lowest loop inductance reported so far is 14 nH [27]. Hence, there is room for research in active integration of the T-type NPC topology in a single module with systematic analysis.

The concept of vertical commutation loop was reported for 2-L converters [20], [21]. In multilevel converter topology, the scenario is different. It is shown that with increased number of power loops, optimization of stray inductance and reduction of interaction among the loops become much more difficult than in 2L converters [26]. In 3L T-type NPC topology, we have five different loops that needs to be optimized simultaneously. The first contribution of this article is that the article proposes a systematic approach to optimize multiple commutation loops simultaneously also taking care of interaction between the loops, which is important for multilevel converters. The second contribution is that this approach introduces an integrated EMI shield to self-contain the common-mode (CM) EMI noise inside the module. Experiment shows a reduction of 21 dB CM noise by proposed scheme. The third contribution of this article is to present a systematic approach toward global optimization, where stray inductances and CM EMI from the module is reduced by a balanced trade-off with thermal resistance. This proposed design methodology of co-optimization of thermomechanical and electrical parameters by implementation of vertical power loop can be extended for other multilevel topologies.

The organization of the article is as follows. In Section II, the stray inductance optimization technique using vertical power loop is explained, and stacked-DBC-based module structure is introduced followed by the analysis of the associated power loops in 3L TNPC and their optimization in the proposed structure. Section III describes the fabrication steps, while in Section IV the switching result of the fabricated module is presented. In Section V, the EMI performance of the module is modeled, and finally validated by experimental results. The

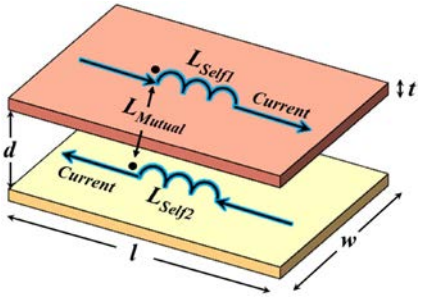

Fig. 3. Mutual inductance cancellation.

thermal performance is discussed in Section VI with the simulation result and loss calculation process. Finally, the article has been concluded in Section VII by discussing the findings and scope of future research.

II. Low Inductive Package With Stacked DBC

A. Mutual Inductance Cancellation in Vertical Loop

In the conventional packages with 2-D power loop, commutation loop inductance can be optimized by reducing the loop area. However, during the layout, the minimum spacing between the dies needed to be maintained to meet the insulation as well as thermal dissipation requirements.

Moreover, total inductance also depends on the number of wire bonds employed per semiconductor die and the diameter of each wire. Selection of the bond number and gauge depends on the surface area of the chip and the total current to be handled. As such, the maximum achievable reduction of inductance by reducing the size of the power loop has a boundary in the conventional packages. To further reduce the parasitic inductance, the vertical power loop is one of the preferable options. This method can utilize the mutual inductance cancellation effect to reduce the parasitic inductance significantly, as shown in Fig. 3.

This technology has been adopted in the laminated busbar design and low inductance PCB design [34], [35]. Total power loop inductance can be expressed as

$$L_{\text{Total}} = L_{S1} + L_{S2} - 2L_M \tag{1}$$

where L_{S1} and L_{S2} are the self-inductances of top and bottom trace, respectively, and L_M is the mutual inductance in between them. Self-inductance depends on the width (w), thickness (t), and length (l) of the trace, while the mutual inductance depends on one more variable; the distance between the two current carrying traces (d). Self-inductance and mutual inductance can be calculated using the equation listed as follows:

$$L_S = 2l\left[\ln\left(\frac{2l}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{l}\right)\right] \tag{2}$$

$$L_M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d} + \sqrt{1+\left(\frac{l}{d}\right)^2}\right) - \sqrt{1+\left(\frac{d}{l}\right)^2} + \frac{d}{l}\right. . \tag{3}$$

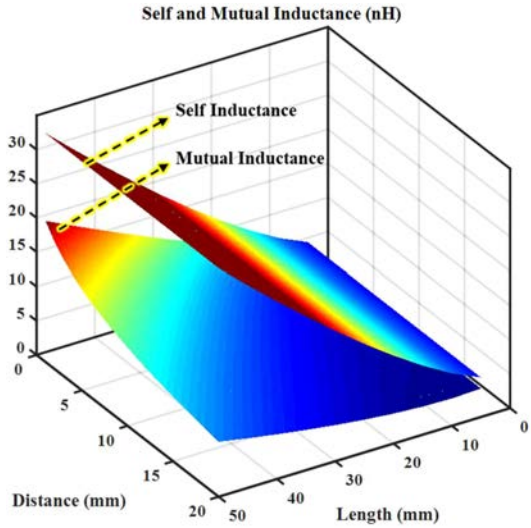

Fig. 4. Impacts of length and distance of traces on the inductance.

Effect of interlayer distance and trace length on the value of self and mutual inductance has been shown in Fig. 4. To maximize the reduction of inductance, interlayer distance and length of current-carrying trace should be minimized.

B. Introduction to the Proposed Module Structure

The designed T-type NPC module consists of two DBCs made of aluminum nitride (AlN) substrate due to its high thermal conductivity compared to other choices. Beryllium oxide (BeO) based substrate has the best thermal conductivity (200–250 W/mK) and high dielectric constant, which makes it suitable to be used as the substrate. Nevertheless, it is unfeasible as the powder of BeO is extremely poisonous to human health. It produces toxic gas by the reaction between Cu, BeO, and O_2 at 1065°C –1085°C, which is needed to make copper on the BeO substrate. On the other hand, AlN's thermal conductivity is around 150–170 W/mK which is higher than other available ceramics such as Al_2O_3 (20–30 W/mK) and Si_3N_4 (60–70 W/mK), hence chosen as the material for DBC substrate.

LASER drilled through hole vias on the top DBC makes the interconnection between two stacked substrates. The structure of the module with appropriate labels has been shown in Fig. 5. Input terminals and output terminals are placed in the opposite direction for the ease of installation of the module in system-level design. Protruding gate driver pins for four individual switching positions are located in the middle. In Fig. 6, the internal view of the module is revealed.

C. Inductance Optimization for All Associated Power Loops

The switching states of a 3L T-type NPC topology can be defined as P, O, and N. States of switches and output is included in Table I.

With real load when power factor is not unity, the overall operating region can be spaced in four quadrants as shown in Fig. 7 depending on the current and voltage polarity.

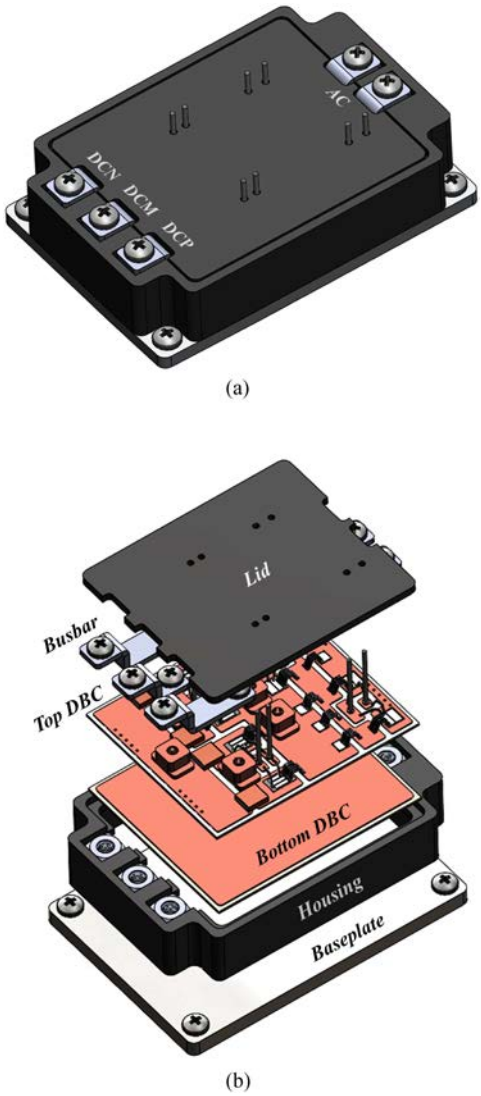

Fig. 5. Structure of the proposed module. (a) CAD drawing of the module. (b) Exploded view of the module.

TABLE I
SWITCHING STATES OF 3L T-TYPE NPC

State	V_{out}	T_1	T_2	T_3	T_4
P	$+V_{DC}/2$	On	on	off	off
O	0	Off	on	on	off
N	$-V_{DC}/2$	Off	off	on	on

In each quadrant, 3L T-type NPC topology shows a unique commutation loop. During the transition between state P↔O, when current is positive or coming out of the cell, switch position marked as T_1, T_2, and D_3 will constitute the commutation loop. T_1 (SiC) will be hard switching and T_2 (IGBT) will be soft switching. This commutation loop represents the first quadrant operation mode shown in Fig. 7. Similarly, for the transition of states O↔N but current in negative direction or entering the cell, switch position T_4 (SiC), T_3 (IGBT), and D_2 will constitute the power loop. This one represents the third quadrant operation mode. For unity, lagging or leading power factor, the peak current will appear between first and third quadrant and it is the most desirable operation mode as only SiC devices will be hard switching and IGBT's will be soft switching. Therefore, the power loops in first and third quadrant is given most importance in the layout. However, for the other two operation modes, IGBTs will be hard switching and the switching loss will be aggravated. Hence, from a layout point of view, irrespective of switching scheme, these loops need to be optimized with the same importance as well.

TABLE II
EXTRACTED LOOP INDUCTANCES

	Commutation Loops in 3L Operation				2L Operation
	CCL1	CCL2	CCL3	CCL4	
Inductance (nH)	4.6	4.93	4.6	4.93	8.02

For the transition between states O↔N and when current is positive or leaving out of the cell, T_4, T_2, and D_3 will constitute the power loop and this represents the second quadrant operation mode. During this mode of operation, T_2 (IGBT) will be hard switched and majority of the switching loss will be coming from this switching position. On the other hand, during the transition of states P↔O, but current in negative direction or entering into the cell this instance, T_1, T_3, and D_2 will constitute the commutation loop and it represents the fourth quadrant operation mode. In this configuration, the body diode of the T_1 will be conducting and T_3 (IGBT) will be hard switched. All these loops are shown in red in Fig. 8 along with their physical location in the module.

Again, the external loop between the switch T_1 and T_4 needs attention as well. For instance, when the transition is happening between O↔N, and T_4 is hard switched ON, the voltage stress across the T_1 will be doubled. It would happen the same way for T_4 during P↔O transition when T_1 is hard switched ON. Moreover, in light load condition to operate the module as a 2L inverter, current will commutate between T_1 and T_4. Optimization of this loop is also done as shown in Fig. 9 and an overall optimized layout has been achieved finally.

After optimizing the loops, the stray inductances of individual loops have been extracted using Q3D including bonding wires. The result has been presented in Table II.

III. FABRICATION OF THE MODULE

The fabrication process starts with the preparation of the two AlN DBCs. Using $FeCl_3$ solution, DBCs are etched according to the layout. After that, top DBC is drilled using LASER. The inner wall of those holes is plated using thick plated copper process to make them conductive. Once the DBCs are ready, attachments and assembly process has been carried out. Two different kinds of solder paste with different melting temperature have been used during reflow soldering steps. A 3 mm thick nickel-plated copper baseplate is used as heat spreader at the bottom of the module.

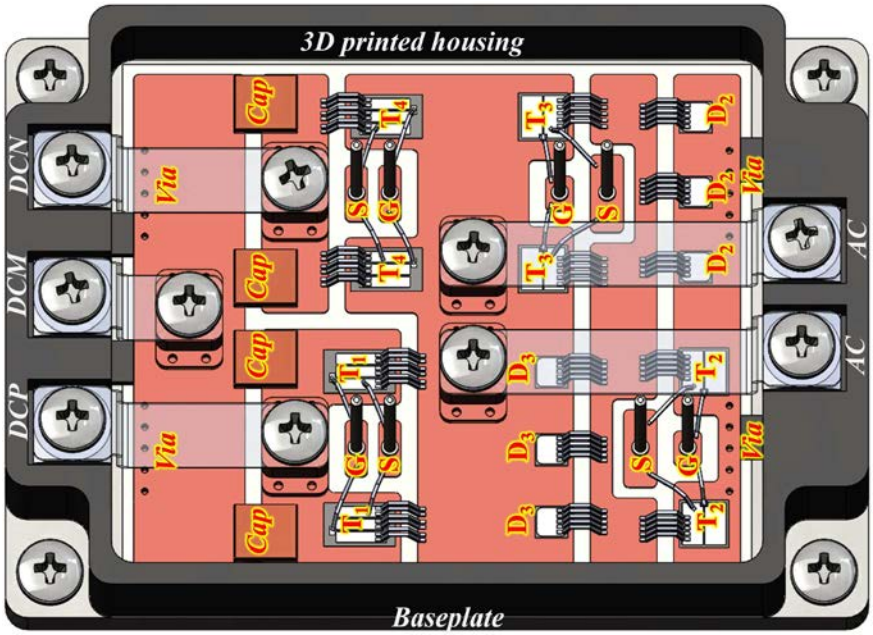

Fig. 6. Internal layout of the module.

TABLE III
INFORMATION OF THE DIES USED

	Information of Selected Die				
	Manufacturer	Part Number	Rated Voltage (V)	Rated Current (A)	Operating Temperature Range (°C)
SiC MOSFET	Cree	CPM2-1200-0025B	1200	98	-40 to +175
Si IGBT	OnSemi	NGTD21T65F2	650	45	-55 to +175
SiC Diode	Cree	CPW5-0650-Z050B	650	50	-55 to +175

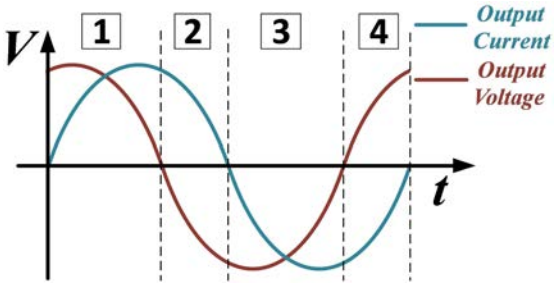

Fig. 7. Four operating region when p.f ≠ 1.

Attachment process starts by applying solder paste to the top surface of the baseplate using stencil. Bottom DBC is placed on top of it. Custom-built graphite fixture has been used so that the components are aligned. Next, same solder paste is dispensed on the top surface of the bottom DBC and top DBC is stacked on top of that. Finally, the top surface of the top DBC is stencil printed and semiconductor chips are placed on their designated locations. Everything is attached together by a single reflow soldering using SAC 305 solder paste of melting temperature 220°C.

Once the semiconductor chips were attached, wire bonding has been done using manual wire bonder machine. For gate connection, 5 mil aluminum wire bond and for power routing, 12 mil aluminum wire bonds have been used. Next, the gate pins and screw terminals for busbar connection and decoupling capacitors are attached using Pb37Sn63 eutectics solder paste of 183°C melting temperature.

Fig. 10 shows fabrication steps of the module, while Table III gives a list of semiconductor dies and their properties.

IV. Experiment Results

After the fabrication of the module, to evaluate the switching performance, set of standard double pulse test has been performed. As explained in the Section II, during 3L operation, there are four separate commutation loops. For 3L operation, as the commutation loops 1 and 3 have very similar loop with close stray inductance, only loop 1 is tested. It is true for loops 2 and 4. Hence, loop 2 is tested for this case. For 3L case, all the commutation loops individually see the half of dc link voltage, so V_{DS} is at 400 V and load current is pushed around 80 A. Moreover, there is another commutation loop coming from 2L operation of the module where the clamping leg is not involved. A separate test is done to verify the switching characteristics of that loop. For 2L operation, V_{DS} is kept at 800 V and the device current was pushed around 160 A. Device current measurement

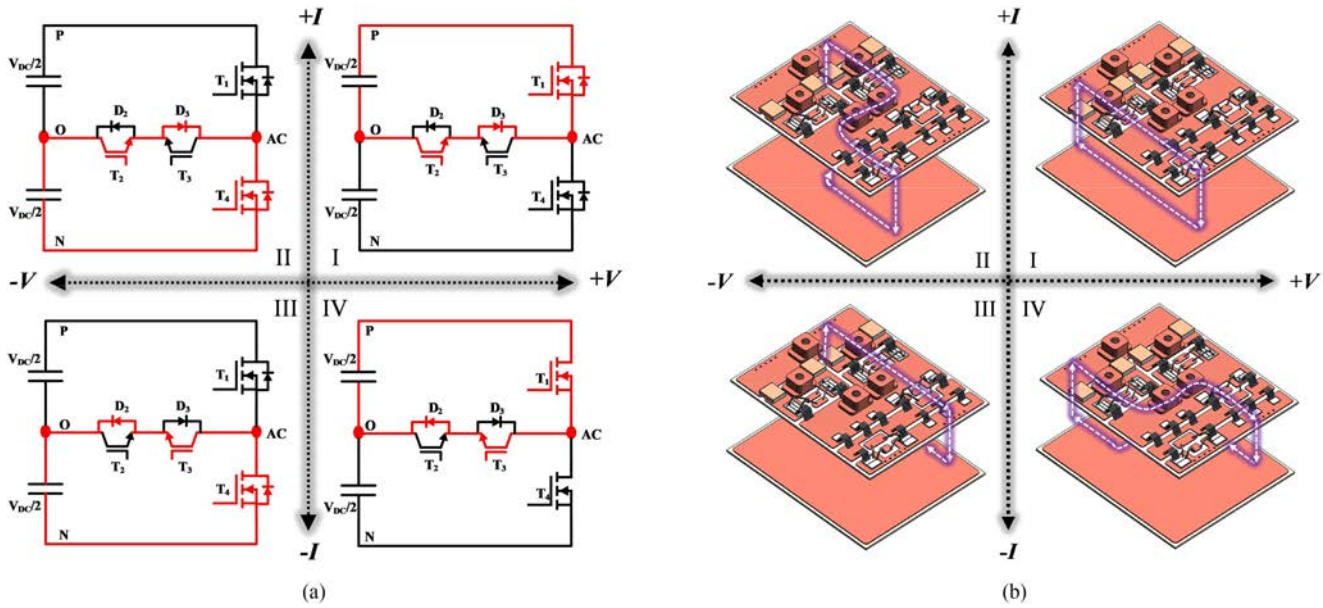

Fig. 8. Commutation loops involved in 3L operation. (a) Commutation loops in 3L operation (marked in red). (b) Physical commutation loops in designed module.

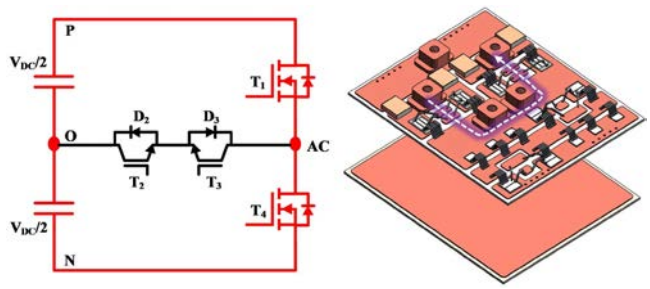

Fig. 9. Commutation loop in 2L operation.

was not possible as the module comes with integrated decoupling capacitors so only load current was monitored. An air core inductor of 131 μH with optimized winding capacitance has been used as clamping load. Off the shelf gate driver from CREE was used to drive the module during testing. Fig. 11 shows the test setup for DPT test.

The test schematics for mentioned three test and their switching waveforms have been shown in Figs. 12 –15. Loop inductance can also be extrapolated from the ringing frequency of $V_{\rm DS}$ during turn OFF transient. If the frequency is measured and the datasheet is available for the die under test, inductance can be calculated using

$$L_{\rm loop} = \frac{1}{4\pi^2 \times f^2 \times C_{\rm OSS}}\,. \tag{4}$$

Here, $L_{\rm loop}$ is the stray inductance, f is the ringing frequency, and $C_{\rm OSS}$ is the output capacitance of the die under test. Placement of decoupling capacitor closer to the device pair helps to reduce the size of power loop as well as the stray inductance, $L_{\rm loop}$, which will eventually bring down the energy associated to this oscillation, hence prevent the capacitor to get over heated [36]–[38]. During the test for capturing the data, 2 GHz oscilloscope from Tektronix has been used. A total of 200 MHz isolated voltage probe has been used for voltage measurement and current was measured using a current probe of 120 MHz bandwidth. During turn-ON, 5 Ω gate resistance and for turn-OFF, 1 Ω resistance was used. For instance, to verify the extracted result 4.6 nH for current commutation loop (CCL3), inductance has calculated from $C_{\rm oss}$ of T_4 switching position at 400 V is around 560 pF as two devices are paralleled at that position. From the 93.2 MHz switching frequency, the inductance can be extrapolated as 5.1 nH, which is very close to the extracted value. Due to the nonideality of manufacturing process, placement of probe and inductance of the measurement point at 0.5 nH deviation is there. Same analysis is done for other CCL as well and no more than 0.5 nH deviation was found from the Q3D extracted value.

When SiC switch position is switching, a turn OFF dv/dt is achieved around 30.1 and 51.5 V/ns for 400 V (3L) and 800 V (2L) blocking voltage, respectively. For IGBT due to the long tail current of the device during turn OFF, turn OFF dv/dt is 15.6 V/ns. Highest overshoot of 133 V is seen for 2L operation, which is 16.6% of the applied dc link voltage.

V. CM Noise Current Reduction

A. Modeling of CM EMI Network

When a voltage gradient is applied across a capacitor, a displacement current passes through it, which is governed by (5)

$$i_C = C\frac{{\rm d}v}{{\rm d}t} \tag{5}$$

$$C = \frac{A\varepsilon}{d}\,. \tag{6}$$

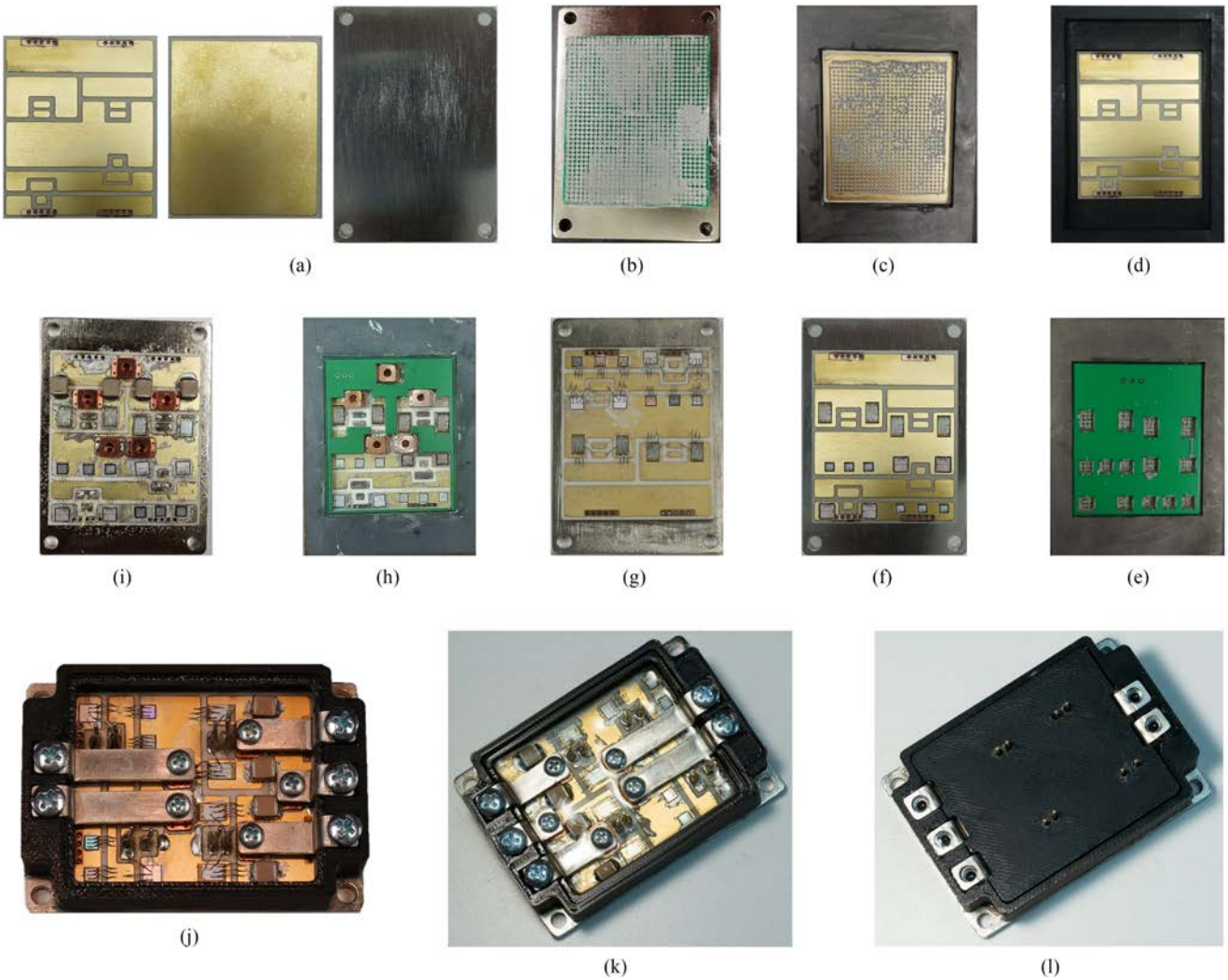

Fig. 10. Fabrication steps of the module. (a) Top DBC, bottom DBC, and baseplate. (b) Screen printing on baseplate. (c) Screen printing on bottom DBC. (d) Alignment using fixture. (i) Module after second reflow. (h) Preparation of second reflow to attach screw terminals. (f) Attached die, DBC, and substrate after first reflow. (e) Screen printing for die attachment. (j) Module after attachment of housing and connectors. (k) Encapsulation of module using silicone gel. (l) Finished module after fabrication.

This displacement current is the primary source of CM EMI in power modules. The parasitic capacitance between switching node to ground provides the path for the noise current to be injected in the ground through the baseplate, as the baseplates are grounded in most of the systems. As decreasing the dv/dt is not a desirable solution to control the noise current by sacrificing the switching speed, one of the popular solutions is to minimize the value of parasitic capacitance itself, which can be achieved either by increasing the thickness of ceramic substrates (d) or by reducing the area of the switching node (A) as shown in (6).

Increasing the thickness of the ceramic substrate will offer higher thermal resistance and hinder the thermal performance of the module. Moreover, the parasitic inductance cancellation will be hampered too, as the coupling will go down with the increase of the distance between two conducting layers. The number of die the switching node is accommodating, die footprint, and number of interconnects landing on that island also limits the reduction of the area of the switching node. Hence, in most of the cases, there is a very small room to play with the value of this capacitance. The proposed approach in this article is different from the conventional one and similar to embedding Y capacitor in module proposed in [39] where noise is routed back to the source. Drawback of embedding Y capacitor is its value is limited by the safety standard and it increases fabrication complexity.

In the proposed approach, instead of embedding a passive capacitor, the noise is routed back to the noise source by using the parasitic capacitance of the module itself. In Fig. 16(a) and (b), the parasitic network of conventional module and the proposed module is presented.

Due to the introduction of the additional DBC, whose entire conducting plane is fixed to DCM potential, it acts as an EMI shield and provides a bypass path for noise. To evaluate the performance of the designed module and have an apple-to-apple comparison, one more module with same pattern but with single DBC is manufactured. Top and bottom copper of this DBC is isolated, as it does not have any via. Associated parasitic capacitance for both modules from individual nodes has been presented as C_1–C_5 in Fig. 16(c) and (d). The values of all

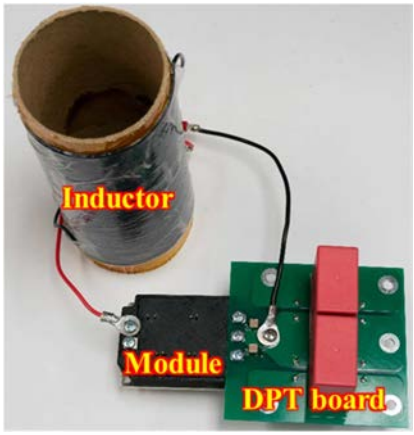

Fig. 11. Test setup.

TABLE IV
EXTRACTED PARASITIC CAPACITANCES

	C_1	C_2	C_3	C_4	C_5
Single DBC (pF)	29.68	18.2	96	27.8	52
Stacked DBC (pF)	29.68	18.2	96	27.8	340

the parasitic capacitances are extracted using Q3D and listed in Table IV.

To model the equivalent circuit of EMI propagation path, we have considered all the associated commutation loops and modeled them separately. For modeling the noise circuit, according to the substitution theorem, a MOSFET can be replaced by a voltage source including all the parasitics at its branch, keeping the circuit behavior the same. Similarly, a diode can be replaced by a current source [40]. After replacing all the switches and decoupling capacitors with voltage and current source, we can apply superposition theorem to see the resultant EMI voltage on LISN. In our analysis, MOSFET is replaced by voltage source $V_{\rm ac}$ and diode is replaced by current source I_D. Apart from the stray capacitance of the module shown in Table IV, one additional capacitance has been considered. Here, the additional capacitance C_8 represents the additional CM noise path such as the stray capacitance of load to ground, barrier capacitance of the isolated gate driver, and power supply. Its value is estimated to be 10 pF.

Primarily, a CM noise equivalent circuit is developed from the parasitic capacitance network of single DBC module shown in Fig. 16(c) and the simplified equivalent model is shown in Fig. 17. Similarly, the CM equivalent is drawn for the 2L operation of stacked DBC module and shown in Fig. 18. Though there are four separate loops associated with 3-L operation, it is shown previously that CCL1 is mirror of CCL3. Same is true for CCL2 and CCL4. Primarily, CM equivalent network for CCL3 out of four associated loops is drawn in Fig. 19. The noise voltage across LISN for single DBC module is given as follows:

$$V_{\rm LISN\ (Single\ DBC)} = \frac{\frac{Z_{\rm LISN}}{2} \| Z_{C1+C2+C5}}{Z_{C3+C8} + \frac{Z_{\rm LISN}}{2} \| Z_{C1+C2+C5}} V_{\rm ac} \tag{7}$$

$$V_{\rm LISN\ (Stacked\ DBC)} = \frac{\frac{Z_{\rm LISN}}{2} \| Z_{C5}}{Z_{C8} + \frac{Z_{\rm LISN}}{2} \| Z_{C5}} V_{\rm ac}. \tag{8}$$

For stacked DBC solution, CM EMI noise equivalent circuit of all the commutation loops are very similar to the model shown in Figs. 18 and 19. CM noise voltage measured for stacked DBC can be presented by (8) for all the associated loops. In (7) and (8), if the value of denominator increases, the noise measured at LISN terminal will go down. That is exactly happening at the case of stacked DBC module. Due to the EMI shielding provided by the bottom DBC, the C_3 capacitance is routed back to the middle point of the dc link whose voltage is ideally zero. Now, C_8 capacitance is the only path for the CM noise to be injected in the ground. Hence, value of the denominator will be higher for stacked DBC solution and the noise voltage will go down accordingly. The ratio between Z_{C3} and Z_{C3+C8} is 9.6 using values from Table IV, and noise voltage of stacked DBC module should be around 20 dB lower according to the developed equivalent model.

B. Experimental Validation

Standard EMI test setup was utilized to measure conducted CM EMI noise from the modules to be compared [46], [47]. Baseplate of the modules are placed on top of a grounded copper plane, which is representing the grounded chassis of motor. Switching test has been done in external loop dedicated for 2L operation for single DBC and stacked DBC module as the schematic shown in Fig. 12(c). The noise has been measured using well-grounded LISN (COMPOWER LI-4100) pair. As the highest voltage rating of the LISN was 780 V dc, test was performed using 400 V dc link. The output from both of the LISN is passed through a noise combiner to get the CM voltage reading according to (9):

$$V_{\rm CM} = \frac{V_{N1} + V_{N2}}{2}. \tag{9}$$

Here, V_{N1} and V_{N2} are the voltage measured across the output of each LISN. The output of the noise combiner is terminated across an external 50 Ω resistance and time domain CM noise data is captured in the oscilloscope by probing voltage across that resistor. Standard EMI test bench used in experiment is shown in Fig. 20.

Gate resistance, load current, and the value of inductive load were kept the same for both the modules during testing. As the layout is kept same for both the modules, the parasitic inductance and area of the switching node remained unaltered. Time domain noise and switching waveform for stacked DBC module are shown in Fig. 21.

For comparison, measured time domain CM noise for both the case is plotted one top of other in Fig. 19(a) using two different colors. Subsequently, fast Fourier transform is performed and the results are shown in Fig. 22 (b). It shows a reduction of CM noise as much as 21 dB is achieved using the proposed shielding approach. The experiment results verify the self-containment capability of EMI noise of the designed module. Within the considered frequency range of conducted EMI (150 kHz–30

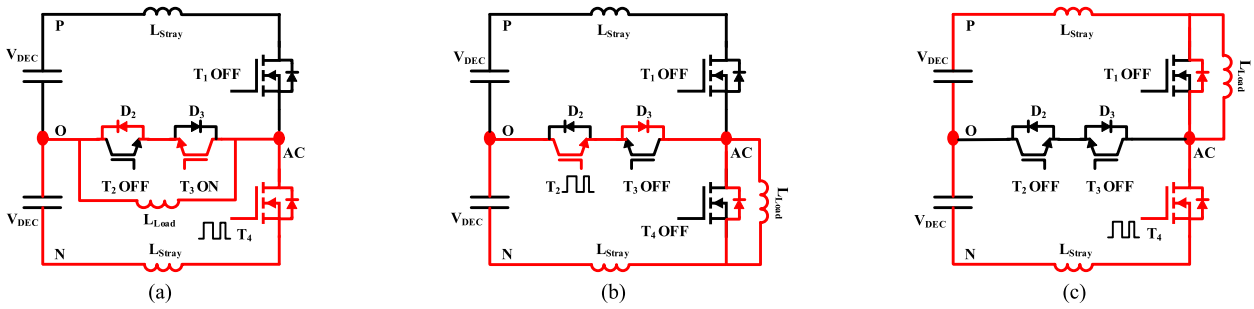

Fig. 12. Schematics of performed double pulse test (DPT). (a) Schematic for DPT of CCL3. (b) Schematic for DPT of CCL2. (c) Schematic for DPT of 2L operation.

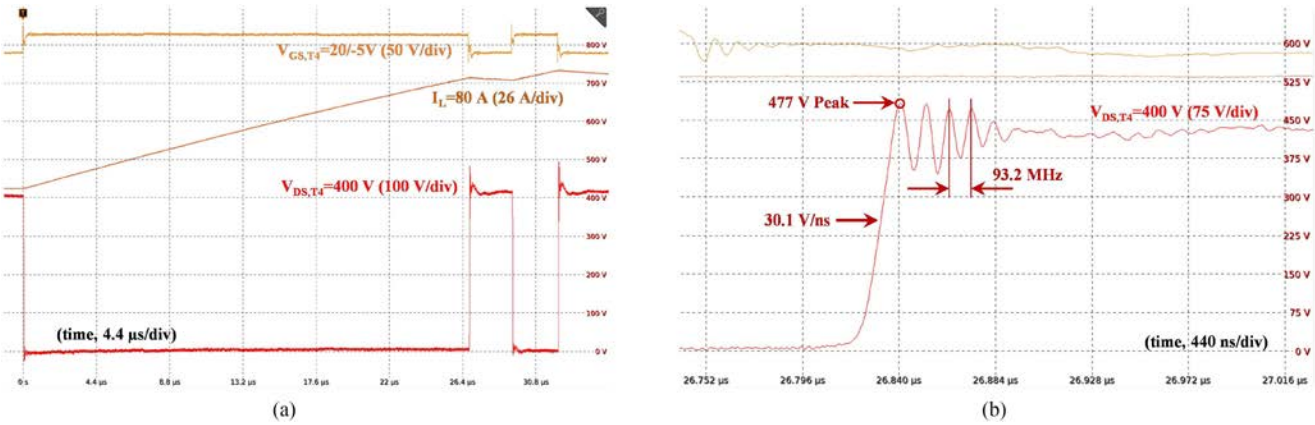

Fig. 13. Switching performance of CCL3. (a) Switching waveform from DPT of CCL3. (b) Zoomed view of turn OFF from DPT of CCL3.

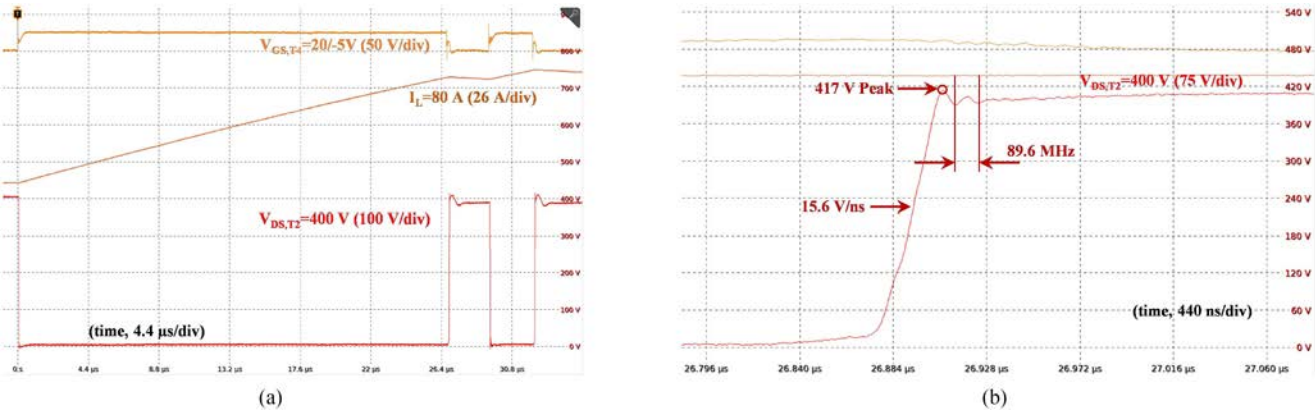

Fig. 14. Switching performance of CCL2. (a) Switching waveform from DPT of CCL2. (b) Zoomed view of turn OFF from DPT of CCL2.

MHz), our designed module shows a consistent performance to reduce CM EMI emission. We believe that the same approach that we have proposed should work for even higher frequency given refined modeling and tailoring to extended frequencies.

VI. Thermal Simulation

To evaluate the thermal performance of the module, an FEA simulation has been done from where the maximum junction temperature and overall thermal resistance (junction to case) of the module can be evaluated. Before starting the thermal simulation, loss calculation was done using MATLAB-based program by utilizing datasheet provided value. The analytical model for loss calculation is according to the literature [41], [42] and modified for hybrid structure as shown in (10)–(15), where $i(k)$ is the transient current, f_0 is the line frequency, f_{sw} is switching frequency, φ is power factor angle, M is modulation index, R represents channel resistance, and V_{fw} is forward voltage drop. As schottky diodes are used in the layout, only conduction loss of the diodes is considered.

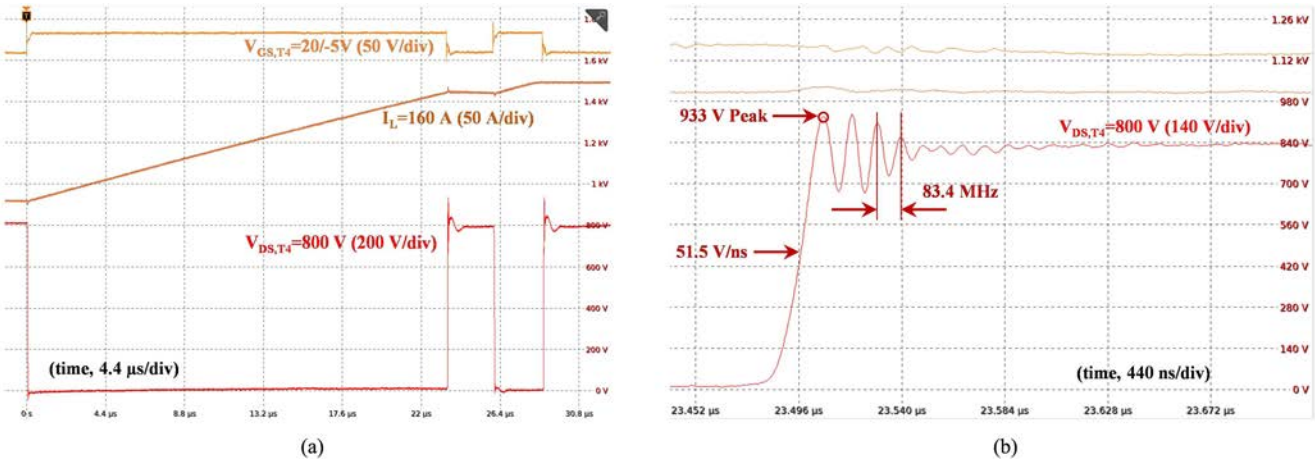

Fig. 15. Switching performance of 2-L operation. (a) Switching waveform from DPT of 2L operation. (b) Zoomed view of turn OFF from DPT of 2L operation.

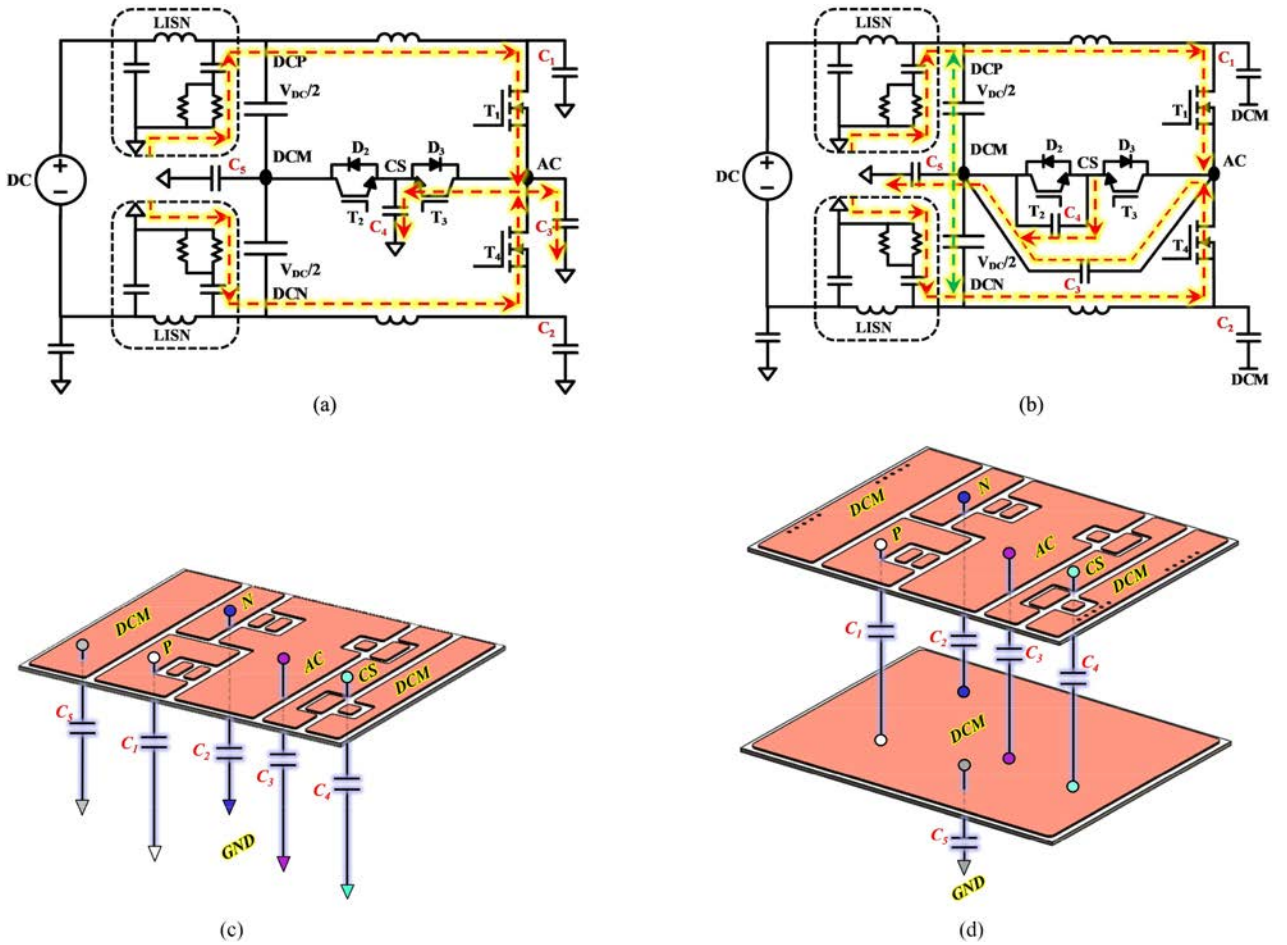

Fig. 16. Representation of CM EMI network. (a) CM noise path for single DBC conventional module. (b) CM noise path for stacked-DBC-based proposed module. (c) Physical location of parasitic capacitance in single DBC module. (d) Physical location of parasitic capacitance in stacked DBC module.

Considering rated current and voltage at 0.95 power factor, 0.8 modulation index, and 70 kHz switching frequency, loss at individual has been calculated. The loss at each die for switching position T_1 and T_4 was found to be 130 W. For clamping leg, the loss was 80 W per IGBT and 53 W per Schottky diode. Simulation was performed in Solidworks at ambient temperature with a convection coefficient *(h)* at the baseplate equal to 5000 W/m^{2}K. The maximum junction temperature 126°C was found in SiC

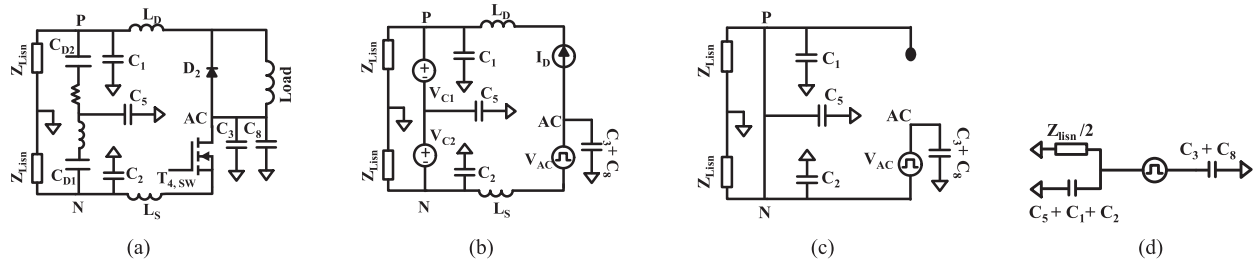

Fig. 17. Equivalent CM EMI circuit of conventional single DBC module. (a) DPT setup: 2L operation. (b) Substitution applied. (c) Superposition applied. (d) Equivalent circuit.

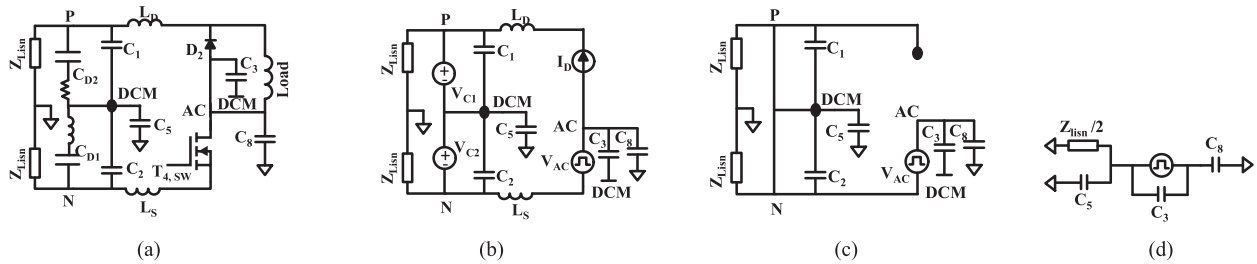

Fig. 18. Equivalent CM EMI circuit of stacked DBC module (loop analyzed: 2-L operation). (a) DPT setup: 2L operation. (b) Substitution applied. (c) Superposition applied. (d) Equivalent circuit.

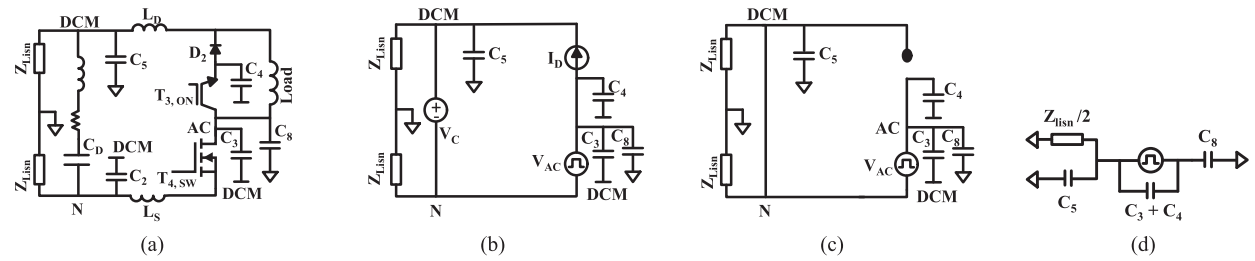

Fig. 19. Equivalent CM EMI circuit of proposed module (loop analyzed: CCL3). (a) DPT setup: CCL3 loop (3L). (b) Substitution applied. (c) Superposition applied. (d) Equivalent circuit.

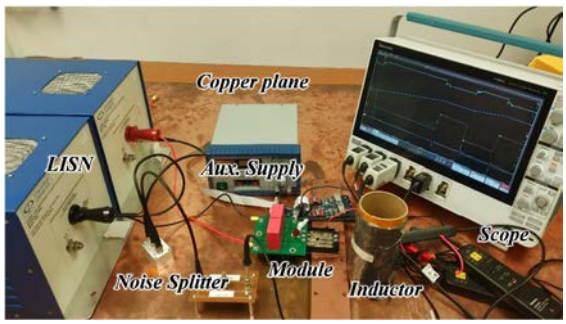

Fig. 20. EMI test bench for CM noise measurement.

MOSFET at T_4 position. Junction to case resistance for the module was calculated to be 0.217°C/W from simulation result. Similar analysis is done for the single DBC-based conventional module and it was found that the thermal resistance for this solution is 0.168°C/W.

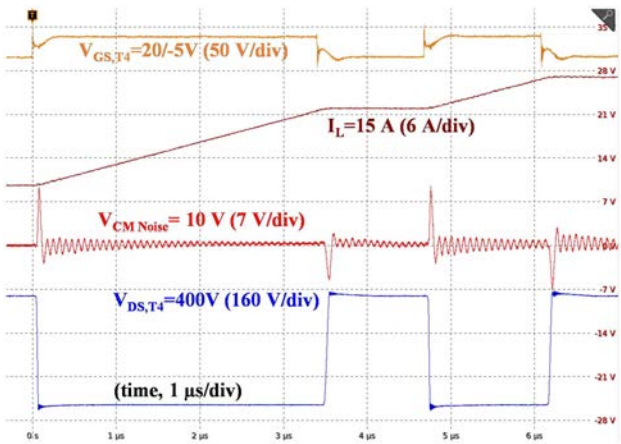

Fig. 21. EMI measurement of stacked DBC module.

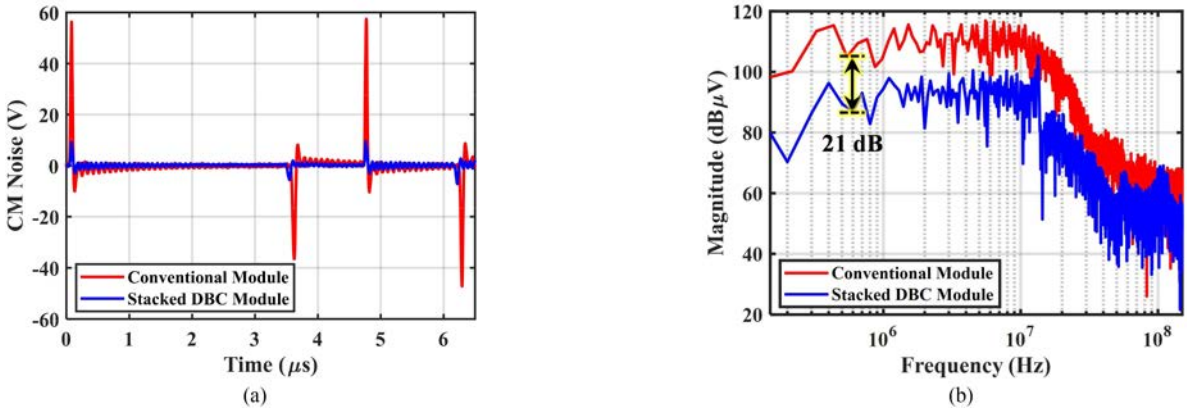

Fig. 22. Comparison of CM noise between stacked DBC and single DBC module. (a) Time domain noise waveform comparison. (b) FFT of CM EMI for stacked and single DBC module.

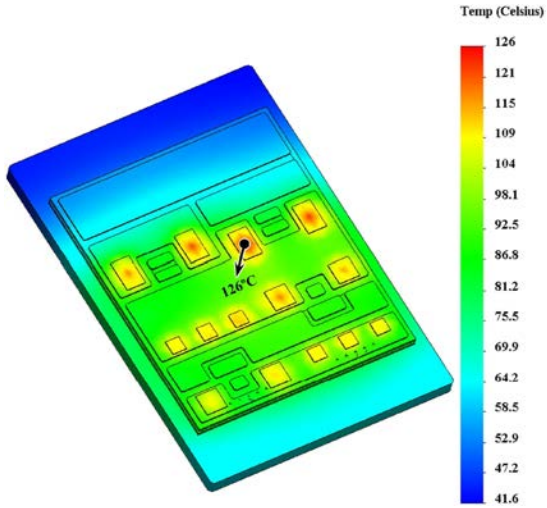

Fig. 23. Thermal simulation result at rated condition.

In the proposed design, we did a co-optimization where by stacking two DBC's the stray inductance and CM EMI goes down by 3.5 times and 10 times, respectively, but the thermal resistance increases by 1.29 times. From a global optimization point of view, benefit in EMI and stray inductance reduction overwhelms the sacrifice of thermal resistance.

Temperature rise of the embedded decoupling capacitor is primarily related to the equivalent series resistance (ESR) and current (I_{decap}) flowing through it. An experiment is performed to measure the current between main dc bus capacitor and module (I_{Supply}), by putting the module in DPT setup. Waveforms are shown in Fig. 24. Waveform of I_{decap} is obtained from the current supplied to the load inductor (I_L) and the current between main dc bus capacitor and module (I_{Supply}). Based on the waveform, we can see that, there is charging and discharging current flowing through the embedded ceramic decoupling capacitor (I_{decap}) in every switching instants, and it resonates with the busbar inductance and embedded decoupling capacitor. Estimation of the I_{decap} helps to select the appropriate ceramic decoupling capacitor. The ESR of the selected capacitor is 40 mΩ at the frequency of oscillation. The estimated loss per

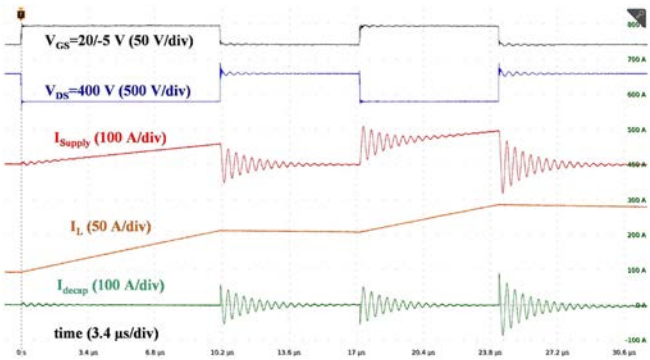

Fig. 24. Test waveform showing current in decoupling capacitor.

capacitor is 4.52 W at rated condition due to I_{decap}, assuming 70 kHz switching frequency.

$$P_{\mathrm{Loss}\ (x)} = P_{\mathrm{Cond}\ (x)} + P_{\mathrm{sw}(x)} \tag{10}$$

$$P_{\mathrm{Cond}\ (\mathrm{MOSFET})} = \frac{1}{\pi}\int_0^{\pi} i^2\,(k)\,R_{\mathrm{DS(on)}} M\,|\mathrm{Sin}\theta|\,\mathrm{d}\theta \tag{11}$$

$$P_{\mathrm{sw(MOSFET)}} = 2f_0 \sum_{k=\frac{\varphi f_{\mathrm{sw}}}{2\pi f_0}}^{k=\frac{\pi f_{\mathrm{sw}}}{2\pi f_0}} \left(E_{\mathrm{MOSFET(on)}} + E_{\mathrm{MOSFET(off)}}\right) \tag{12}$$

$$P_{\mathrm{Cond\ (IGBT)}} = \frac{1}{\pi}\int_0^{\pi} \left(|i\,(k)|\,V_{\mathrm{fw(IGBT)}} + i^2\,(k)\,R_{\mathrm{(IGBT)}}\right) \times (1 - M\,|\mathrm{Sin}\theta|)\,\mathrm{d}\theta \tag{13}$$

$$P_{\mathrm{sw(IGBT)}} = 2f_0 \sum_{k=\frac{0*f_{\mathrm{sw}}}{2\pi f_0}}^{k=\frac{\varphi f_{\mathrm{sw}}}{2\pi f_0}} \left(E_{\mathrm{MOSFET(on)}} + E_{\mathrm{MOSFET(off)}}\right) \tag{14}$$

$$P_{\mathrm{Cond\ (Diode)}} = \frac{1}{\pi}\int_0^{\pi} \left(|i\,(k)|\,V_{\mathrm{fw(Diode)}} + i^2\,(k)\,R_{\mathrm{(Diode)}}\right) \times (1 - M\,|\mathrm{Sin}\theta|)\,\mathrm{d}\theta. \tag{15}$$

Decoupling capacitors of module are located in a way that the chance of thermal coupling with the die is minimal. From the simulation, the location of the decoupling capacitor has a temperature of 66.8°C. Moreover, the capacitors are attached on the same DBC substrate with the semiconductor die; hence, share the same thermal management. So overheating issue of capacitors are duly considered during the design process. In our design, the chosen decoupling capacitor is X7R graded which can operate safely until 125°C. The X7R graded multilevel ceramic capacitor is mainly constructed by BaTiO3. The heat capacity, thermal conductivity, and thermal diffusivity of BaTiO3 is discussed and verified in previous literatures [43], [44]. Considering CTE mismatch between AlN and BaTiO3, literatures [38], [45] show that the strain due to thermal expansion in rated operating condition inside power module package is considerably low. It is concluded that this strain will not pose any reliability concerns which holds for our case as well.

VII. Conclusion

A 3L T-type NPC module has been designed, analyzed, fabricated, and tested which has the same DBC size as Infineon's Easy 2B press fit package. Stacking of two DBCs has been proposed to achieve a vertical power loop to reduce commutation loop inductance. A detailed fabrication steps process has been developed. The electrical switching test has been performed to the rated voltage and current. The fabricated module shows the coherent result of the simulated one. CM EMI has been reduced substantially and verified using experimental result. Thermal simulations have been done to evaluate the thermal performance of the module, which has helped to determine maximum power that can be pushed through the module without overheating and degrading the performance of the die.

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