

Noise Immune Cascaded Gate Driver Solution for Driving High Speed GaN Power Devices

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Abstract— GaN HEMTs permit fast switching, leading to high dV/dt being generated across them. The Common Mode (CM) noise associated with the dV/dt propagates through the gate drivers' isolation barrier capacitance. Due to impedance mismatch between the PWM signal line and return, CM to Differential Mode (DM) noise transformation occurs and distorts the PWM signal at the input of gate driver. This paper investigates the impact of high dV/dt induced noise on gate drive performance in GaN systems. Firstly, noise propagation paths and CM to DM noise transformation are analyzed, followed by simulation and Double Pulse Test (DPT) on hardware. The results show that noise distortion causes mis-triggering of the switches. Further, it is proposed that a cascaded stage comprising power supply and gate driver can suppress the noise by increasing the noise path impedance. The proposed method is verified on hardware with turn-off and turn-on dV/dt equal to 88 V/ns and 62 V/ns respectively at 400 V without mis-triggering.

Keywords—GaN HEMT, gate driver, noise induced mis-triggering, impedance mismatch, CM to DM conversion, cascaded gate driver.

I. INTRODUCTION

Recently, power electronics have undergone a revolution with the introduction of Wide Band Gap (WBG) semiconductor devices such as Gallium Nitride (GaN). Compared with Silicon, GaN HEMTs permit high switching frequencies, which results in a smaller size of the reactive components such as inductors and capacitors. Utilizing these capabilities, significant energy savings could be achieved in various applications ranging from industrial processing and consumer appliances to electric vehicles [1]-[2].

High switching in GaN power devices implies high dV/dt being generated across the drain and source terminal of the device. According to results reported in [3] and [5], the dV/dt can go beyond 150 V/ns. The high dV/dt results in displacement current being generated, which propagates to the control circuitry through the isolation barrier capacitances of the gate driver and the power supply. The displacement current is CM in nature and as it propagates towards the control circuitry it passes through the parasitics, generating noise which disrupts the control signals particularly the PWM signal from the DSP/microcontroller. The displacement CM current can cause sufficient voltage to build up at the gate terminal of the device and cause mis-triggering. A displacement current in μA range is enough to cause mis-triggering [4]. GaN HEMTs are more susceptible to this high dV/dt induced mis-triggering due to lower gate threshold voltage about 2 V [5]. This implies that in a GaN-based half bridge configuration, in addition to the parasitics self-turn on caused by the miller capacitance, the high dV/dt mis-triggering also poses a threat for current shoot through.

Several methods have been proposed to counter high dV/dt induced mis-triggering in GaN-based power converters. The approaches are either based on tuning the gate drive circuit parameters to control switching performance or on diverting the CM displacement current from the signal or control circuitry path. A comparison of CM noise on performance of GaN and Si based power converters for Electric Vehicles (EV) is presented in [8]. Based on the test results, increasing the ON-gate resistance is effective in lowering the CM noise emissions by limiting the switching speed. However, this is achieved at expense of reduced efficiency due to increase in switching loss, which sacrifices the high-speed switching capability of GaN power devices.

Further, modeling and analysis of CM current propagation path for the half-bridge configuration is presented in detail in [4], [5], and [9]. It is shown that gate driver noise immunity can be increased by magnifying isolation capacitance of the power supply, resulting in more CM current finding its way through the isolation capacitance of the power supply. However, the control circuitry is still susceptible to the distortion through the isolation barrier of the power supply. Similarly, a noise containment method is proposed in [8]. By placing C_V capacitors between signal ground and the chassis and power ground the chassis, the noise can be diverted from the DSP/microcontroller. Although, this approach is effective, it can result in considerable near-field Electromagnetic Interference (EMI) emission. Cascading gate driver power supply is shown to be an effective method in increasing noise immunity [12]. By cascading the gate driver power supplies, the noise path impedance can be increased substantially to lower the amplitude of the CM current.

Impedance mismatch between the General-Purpose Input Output (GPIO) pin or PWM signal and return line of the DSP and impact of the RC filters in the signal path in the gate driver primary side is also an unreviewed contributing factor for high dV/dt induced mis-triggering. The impedance mismatch causes CM noise to convert into DM noise and that distorts the PWM from the DSP. This distortion gets reflected and amplified in the gate driver output seen by the GaN HEMT, which can lead to spurious mis-triggering event. This paper investigates the effect of impedance mismatch on the performance of gate driver for GaN-based half-bridge and proposes a cascaded gate driver stage comprising power supply and gate driver. At first, the noise propagation paths are analyzed, and a noise equivalent circuit is developed. This is followed by discussion on noise induced mis-triggering based on the experimental results. Further, the effect of impedance mismatch is analyzed through simulation and a noise immune cascaded gate driver stage is proposed. Lastly, the effectiveness of the proposed gate driver is validated on a hardware prototype.

II. NOISE GENERATION AND PROPAGATION

For GaN transistors, gate drivers composed of an isolated DC-DC converter and a digital isolator are preferred than gate drivers utilizing bootstrap capacitors (Fig. 1). This structure permits high switching frequencies and duty cycles, which is not achievable using a bootstrap capacitor due to the capacitor charging time that hampers the performance at high frequencies [13]. Also, the combination of the isolated DC-DC converter and digital isolator provides higher Common Mode Transient Immunity (CMTI) to suppress noise coupling.

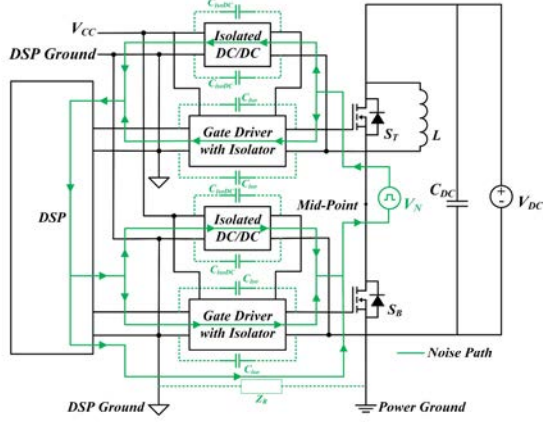


Fig. 1. GaN half-bridge with noise path.

The block diagram of a GaN half-bridge, overlaid with noise path, is shown in Fig. 1. The dV/dt noise source is represented by a pulse source V_N [5]. C_{iso} and C_{isoDC} are the isolation capacitances of the isolated buffer and isolated DC-DC power supply and are the main noise propagation path. The noise current flows from top side gate driver's isolation barrier capacitances towards the DSP. From DSP, there are the following two paths for noise to flow: bottom-side gate driver towards the mid-point and DSP ground to power ground through impedance Z_R . Fig. 2 shows the equivalent noise path for a half-bridge configured for Double Pulse Test (DPT) [14]. As the top device remains off during DPT, the signal pin for top gate driver is shorted directly to the signal ground. Assuming that the major impedance from the noise path is offered from parallel combination of C_{iso} and C_{isoDC} , the displacement current can be approximated as:

$$I_{Displacement} = (C_{iso} + C_{isoDC}) \frac{dV_N}{dt} \quad (1)$$

A RC low-pass filter is usually placed before isolated buffer to damp the noise (ringing), generated due to parasitics. Due to this filter and series output resistance of DSP, there is impedance mismatch between the PWM signal and return line. This impedance mismatch causes noise to transform from CM to DM as reported in [14],[15]. As a result, the PWM signal at the primary side of the gate driver is distorted. This can lead to mis-triggering if the logic at the input of the primary side of the gate driver is not able to maintain its designated level.

III. NOISE INDUCED MIS-TRIGGERING

To investigate the effect of dV/dt induced noise and CM to DM noise transformation, a half-bridge is built using two GaN Systems GS66516T 650 V 60 A transistors in the top and bottom position (Fig. 3). The top and bottom switch gate

drivers consist of a Silicon Lab's Si8271 isolated gate driver, which has 0.5 pf isolation capacitance [17] and isolated power supply from RECOM with maximum isolation capacitance of 10 pf [18]. This combination provides the least isolation capacitance available. The output voltage from the gate driver is -3 V in OFF state and +6 V in ON state. The DSP used for generating DPT pulses is Texas Instrument LAUNCHXL-F28379D [21].

A DPT is performed to test the device near rated current of 60 A at 400 V. However, at 200 V and 9 A, a mis-triggering is observed after turn OFF transient of both pulses (Fig. 4). The switch mis-triggers as the noise amplitude at gate driver input exceeds the threshold and leads to false turn ON of the bottom switch. Further, the effect of dV/dt on DSP signal is also visible at turn ON and OFF transients of both pulses. The switching dV/dt at mid-point generates displacement current that flows through the noise equivalent circuit in Fig. 2.

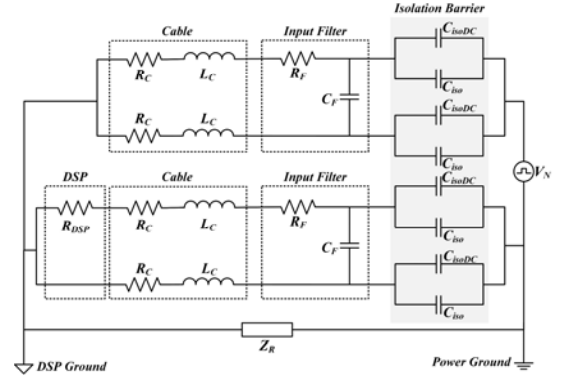


Fig. 2. Noise equivalent circuit.

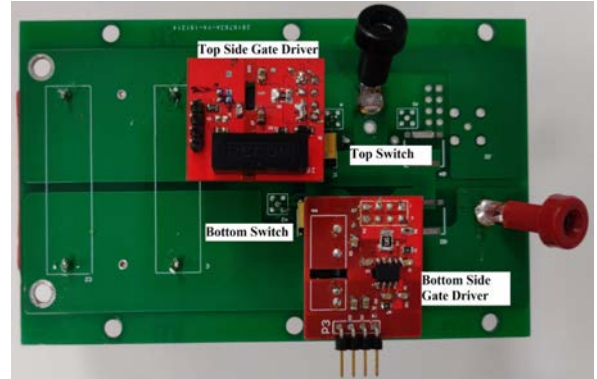


Fig. 3. GaN half-bridge with gate drivers.

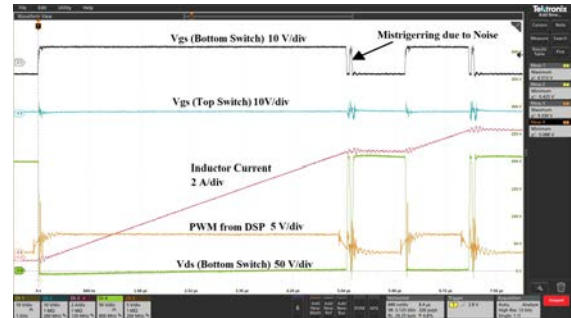


Fig. 4. Mis-triggering at 200 V.

IV. IMPEDANCE MISMATCH

The GPIO pins on a DSP have a series output resistance. The signal or DSP ground does not have series resistance. Similarly, the RC filter is also connected differentially with resistance connected in series in the positive line in the circuit. As both lines are not balanced for both DSP GPIO pin and RC filter, impedance mismatch results. The impedance mismatch causes CM noise, flowing from the mid-point through isolation barrier capacitances towards the DSP, to transform into DM noise. The DM noise adds on the gate drive signal appearing at the input of the gate driver.

To validate CM to DM noise transformation due to impedance mismatch, a simulation is performed in LTspice using the noise equivalent circuit of Fig. 2. The component values are set equal to that of the experimental setup. The amplitude of the noise source (which is equivalent to voltage across the top switch) is set to 200 V as mis-triggering is observed at this value (Fig. 4). The following two cases are considered for simulation:

A. Variation of R_{DSP}

Fig. 5 shows the simulation results of the noise waveform at the end of first DPT pulse for two different values of R_{DSP} . The values of RC low-pass filter are kept constant. The noise voltage is measured at the input terminals of the gate driver after the RC filter. The DSP GPIO pin is driven through a FET based push-pull circuitry. Hence, the output resistance is dynamic as it depends on the output state as well as the current flowing through the FETs driving the pin. From Fig. 3, it is evident that mis triggering occurs when GPIO is in low state. Based on the datasheet of the DSP [21], the conservative estimate of output resistance is taken to be around 20 Ω . The value is approximated by using the low-level output voltage of 0.4 V and maximum allowable GPIO current of 20 mA.

From the figure, it is evident that for the value R_{DSP} equal to 20 Ω , the noise amplitude is around 4.0 V, which exceeds the 2.0 V threshold of the Si 8271. With R_{DSP} reduced to 10 Ω the noise amplitude falls to 3.6 V. This results from the fact that lower value of R_{DSP} reduces the extent of impedance mismatch. Further, the effect of adding R_{DSP} in the DSP ground path is also shown in Fig. 5 for R_{DSP} equal to 20 Ω . For this symmetrical case, the noise is contributed solely from the RC filter; the amplitude observed is 1.9V, which significantly less than 4.0 V as observed for the unsymmetrical case.

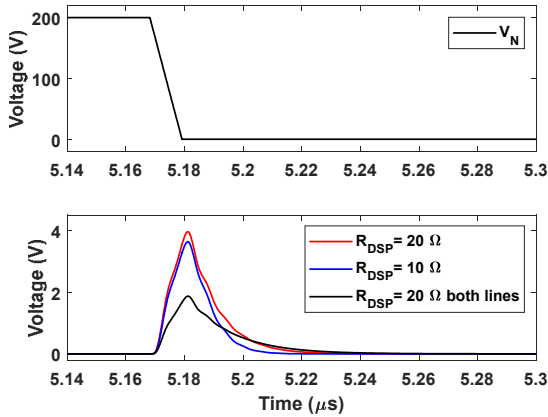


Fig. 5. Noise amplitude variation with R_{DSP} .

B. Variation of RC Filter Parameters

The resistor R_F and capacitance C_F of the RC low-pass filter also contributes to CM to DM noise transformation. To observe this effect, a simulation is performed different values of R_F and C_F with other parameters being constant.

Fig. 6 compares the noise amplitude at end of first DPT pulse for three different values of R_F . For the base value of R_F equal to 30 Ω , the noise peaks at around 4.0, exceeding the gate driver threshold. For values of R_F equal to 20 Ω and 10 Ω , the noise amplitudes measured are 3.48 V and 3.20 V respectively. This shows that decreasing R_F does help in reducing the noise peak, but the reduction is not significant compared with decreasing the value of R_{DSP} .

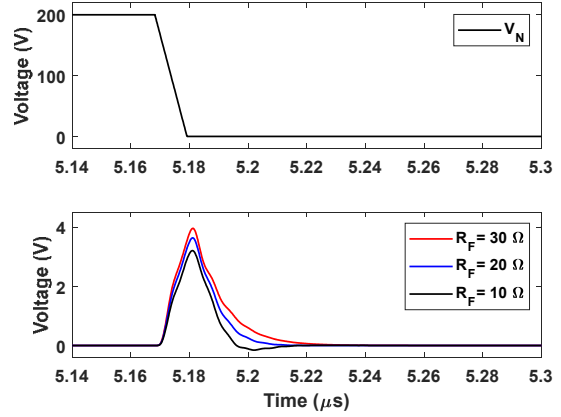


Fig. 6. Noise amplitude variation with R_F .

Similarly, Fig. 7 presents the variation in noise amplitude at end of first DPT pulse for three different values of C_F . From the results it can be concluded that compared with decreasing R_{DSP} and R_F , increasing C_F helps significantly in countering the impedance mismatch between the signal and return path. However, high value of C_F deteriorates the dynamic response of the filter, resulting in PWM signal with considerable rise and fall times. Current shoot through can also result if the rise and fall time intervals of PWM signal of top and bottom switches overlap.

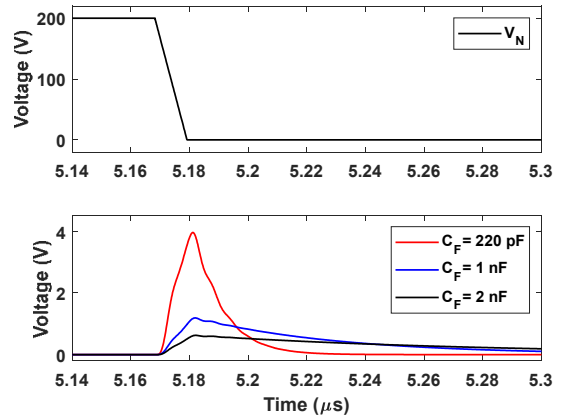


Fig. 7. Noise amplitude variation with C_F .

V. NOISE SUPPRESSION THROUGH CASCADED GATE DRIVER

Several methods have been proposed in the literatures to suppress the dV/dt induced mis-triggering. Noise suppression through fiber optic transmission of both PWM and power signals for gate drivers is proposed in [11]. Although the fiber optic is effective in suppressing the noise, the component count and cost associated with fiber optic transmitter and receiver make it unviable. Further, a noise containment method, proposed in [12] diverts the noise from DSP by using additional filter capacitors, which provides the low impedance path for noise to flow without attenuating the noise.

One approach for noise suppression is to tweak the RC low-pass filter. By increasing the capacitance C_F and decreasing the resistance R_F , the impedance mis-match between two lines can be reduced as evident in Fig. 5, 6 and 7. This in turn reduces the CM to DM noise transformation. Several other methods to reduce CM noise from the switching cell, that is the root cause of the mis-triggering is reported in literatures [19], [20]. However, this sacrifices the initial purpose of using an RC low-pass filter, which is to damp the ringing caused by parasitics and to prevent false turn on with little impact on the rise and fall times. Further, tweaking the value of DSP output series resistance is also not plausible as it depends on operating state and current through the FET push-pull circuitry.

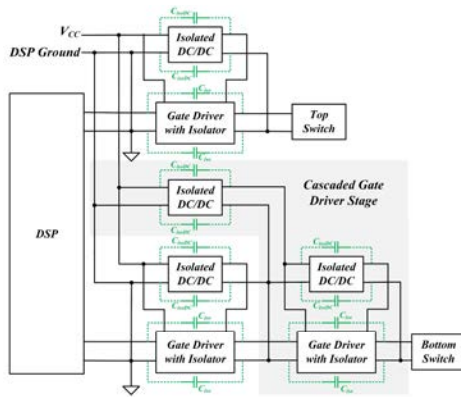


Fig. 8. Gate Drive circuitry with cascaded stage for DPT setup.

Owing to these limitations on tweaking RC low-pass filter and DSP output resistance, noise suppression can be achieved by cascading another gate driver stage to reduce noise amplitude. The proposed concept is shown in Fig. 8, where the cascaded stage comprising power supply and gate driver is provided for the bottom switch only as this switch is only turned ON and OFF during DPT. The cascaded stage is powered from another isolated DC-DC power supply to isolate DSP ground and the cascaded stage DSP ground. Also, compared with cascading power supplies technique [12], the proposed concept has the advantage of having same rating power supplies as each supply drives its associated gate driver stage. The isolated power supply also provides an alternative path for noise to flow. By adding the cascaded stage, the overall impedance of the noise circuit is increased, and the noise amplitude is reduced. This reduces the noise voltage at the input terminal of the gate driver. Further, inclusion of cascaded stage adds an additional propagation delay for the bottom switch. To mitigate this delay, cascaded driver can also be connected for the top switch to synchronize the gate drive signals of the top and bottom switches.

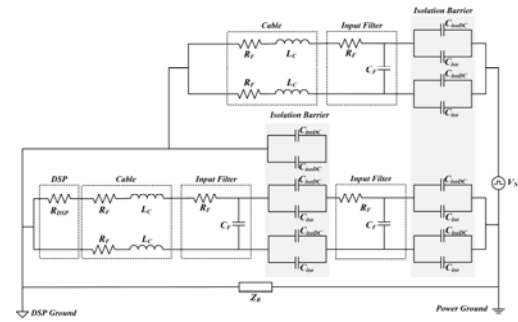


Fig. 9. Noise equivalent circuit for the proposed cascaded stage.

To validate the proposed concept, a simulation is performed using the noise equivalent circuit in Fig. 9. The parameters of the cascaded stage are kept same as that of the original gate drive. The amplitude of noise source is also set to the mis-triggering value of 200 V (Fig. 4). The noise is measured after the RC low-pass filter. The comparison of noise amplitude of proposed cascaded stage structure with the original gate driver structure is presented in Fig. 10. With the cascaded stage, the noise amplitude is reduced considerably (in mV range) and is below the threshold of the gate driver.

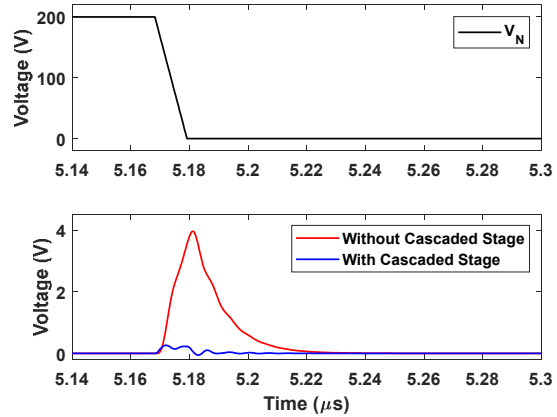


Fig. 10. Comparison of noise amplitude, with and without cascaded stage.

The simulation results in Fig. 10 are further substantiated by performing DPT on the GaN half-bridge in Fig. 3 using the proposed gate driver. Fig. 12 shows the results. At 200 V and 9 A, no mis-triggering is observed. The DPT is continued till 400 V and 55A without any noise induced mis-triggering. The turn OFF and ON dV/dt achieved are 88 V/ns and 62 V/ns as shown in Fig. 13 and 14, respectively.

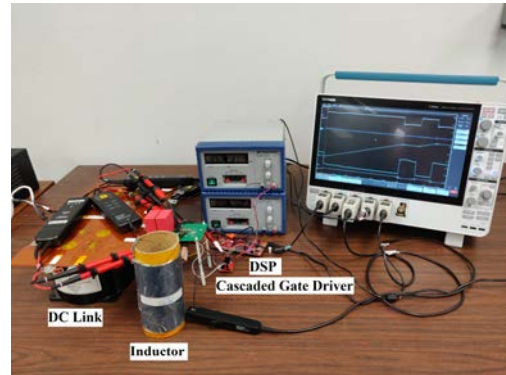


Fig. 11. Experimental setup with cascaded gate driver.

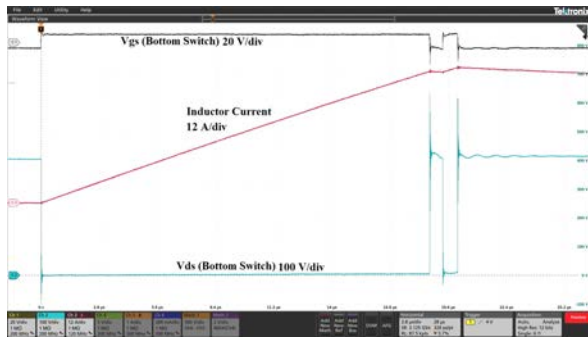


Fig. 12. DPT at 400 V with cascaded gate driver.



Fig. 13. Turn OFF dV/dt for DPT at 400 V 55 A.

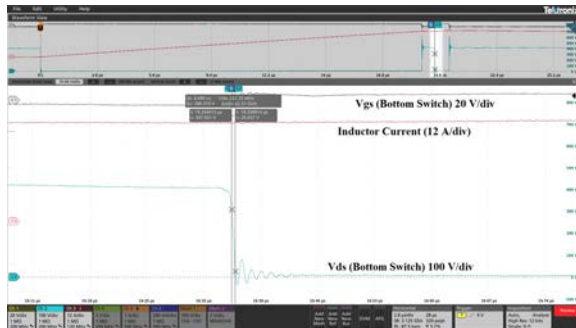


Fig. 14. Turn ON dV/dt for DPT at 400 V 55 A.

VI. CONCLUSION

Fast switching GaN HEMT can achieve slew rate as fast as hundreds of V/ns, which opens the door of advantages for numerous design objectives such as reduced switching loss. However, this high switching speed brings the concern of high CM noise current that hinders the gate drive signal integrity as well as reliability of the entire system. In GaN-based half-bridge, propagation of high dV/dt CM noise at mid-point towards the DSP and its transformation to DM can distort the PWM signal at gate driver input. A technique for mitigating this dV/dt induced turn ON through cascaded gate drive is proposed in this paper. The simulation and hardware DPT results show that this technique is effective in suppressing the noise. Also, the proposed method can be used for both top and bottom switches to synchronize the gate signals.

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REFERENCES

- [1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, May 2014.
- [2] E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, Sept. 2016.
- [3] E. A. Jones, Z. Zhang and F. Wang, "Analysis of the dV/dt transient of enhancement-mode GaN FETs," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 2692-2699, doi: 10.1109/APEC.2017.7931079.
- [4] W. Meng, Z. Fu, F. Zhang and G. Dong, "Common Mode Modeling and Reduction of GaN-based Full Bridge Inverters," *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2018, pp. 60-65.
- [5] W. Meng, F. Zhang, Z. Fu and G. Dong, "High dv/dt Noise Modeling and Reduction on Control Circuits of GaN-Based Full Bridge Inverters," in *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12246-12261, Dec. 2019.
- [6] A.I. Emon et al., "A 650V/60A Gate Driver Integrated Wire-bondless Multichip GaN Module," *2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021.
- [7] A.I. Emon et al., "Design and Optimization of 650V/60A Double-Sided Cooled Multichip GaN Module," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021.
- [8] D. Han, C. T. Morris, W. Lee and B. Sarlioglu, "A Case Study on Common Mode Electromagnetic Interference Characteristics of GaN HEMT and Si MOSFET Power Converters for EV/HEVs," in *IEEE Transactions on Transportation Electrification*, vol. 3, no. 1, pp. 168-179, March 2017.
- [9] Characterization and Analysis of an Innovative Gate Driver and Power Supplies Architecture for HF Power Devices With High dv/dt," in *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6079-6090, Aug. 2017.
- [10] L. Xue, D. Boroyevich and P. Mattavelli, "Driving and sensing design of an enhancement-mode-GaN phaseleg as a building block," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 34-40.
- [11] X. Zhang et al., "A Gate Drive With Power Over Fiber-Based Isolated Power Supply and Comprehensive Protection Functions for 15-kV SiC MOSFET," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 946-955, Sept. 2016.
- [12] V. Nguyen, P. Lefranc and J. Crebier, "Gate Driver Supply Architectures for Common Mode Conducted EMI Reduction in Series Connection of Multiple Power Devices," in *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10265-10276, Dec. 2018.
- [13] W. Zhang, X. Huang, F. C. Lee and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 1484-1489.
- [14] J. Xue, F. Wang and B. Guo, "EMI noise mode transformation due to propagation path unbalance in three-phase motor drive system and its implication to EMI filter design," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014.
- [15] S. Wang and F. C. Lee, "Investigation of the Transformation Between Differential-Mode and Common-Mode Noises in an EMI Filter Due to Unbalance," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 3, pp. 578-587, Aug. 2010.

- [16] Z. Zhang et al., "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 2534-2541.
- [17] Silicon Labs. 2020. Si827x Data Sheet. [online] Available at: <https://www.silabs.com/documents/public/data-sheets/Si827x.pdf>.
- [18] RECOM. 2020. *Rxxpxxs_D Series DC/DC Converters Datasheet*. [online] Available at: <https://recom-power.com/pdf/Econoline/RxxPxx.pdf>.
- [19] A. I. Emon, B. Narayansamy, H. Peng, Mustafeez-ul-Hassan, Z. Yuan and F. Luo, "Investigation of Power Converter's Near Field EMI Containment Using Passive Filters," *2020 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, 2020, pp. 398-403.
- [20] A. I. Emon, Z. Yuan, A. Mirza, A. Deshpande, M. u. Hassan and F. Luo, "1200V/650V/160A SiC+Si IGBT 3L Hybrid T-Type NPC Power Module with Enhanced EMI Shielding," in *IEEE Transactions on Power Electronics*.
- [21] Ti.com. 2021. *TMS320F2837xD Dual-Core Microcontrollers*. [online] Available at: <https://www.ti.com/lit/ds/symlink/tms320f28378d.pdf>.