A Comprehensive Analysis of Current Spikes in a Split-Phase Inverter

Abdul Basit Mirza, Asif Imran Emon, Sama Salehi Vala and Fang Luo
Department of Electrical and Computer Engineering
Stony Brook University
Stony Brook, NY, United States
abdulbasit.mirza@stonybrook.edu

2022 IEEE Applied Power Electronics Conference and Exposition (APEC) | 978-1-6654-0688-8/22/$31.00 ©2022 IEEE | DOI: 10.1109/APEC43599.2022.9773407

***Abstract*—Compared with a conventional two-level inverter, split-phase inverter decouples the top and bottom switches and antiparallel diodes in a phase leg through addition of split inductors. These split inductors prevent current shoot-through with zero deadtime operation, which lowers the distortion in the output waveforms and makes this topology ideal for fast-switching devices such as SiC or GaN. Further, decoupling between top and bottom device's output capacitance also results in lower overall switching loss and improves Electromagnetic Interference (EMI) performance. However, the split inductors experience current spikes during switching transition, which can lead to significant core loss. This paper presents a comprehensive analysis of current spikes in a split phase inverter with SPWM, characterized by the load power factor (PF). The proposed model can be used to optimize the size of split inductor. At first, the circuit of a single phase-leg with split inductors, is analyzed and a mathematical model for spike current estimation is proposed. The proposed model is verified on a SiC-based hardware prototype switching at 72 kHz. It is shown that the spike amplitude depends on the load PF as well as on the values of the split inductors and parasitic capacitances of the power semiconductors. Lastly, the proposed model is extended to the three-phase configuration.**

Keywords— Split-Phase Inverters, Current Spikes, Split Inductors, SiC and GaN, Load Power Factor, Zero Deadtime Operation.

I. Introduction

Adoption of Wide Band Gap (WBG) devices in a standard three-phase two-level inverter promises increase in power density and efficiency through reduction in the size of the output filter and switching loss compared with Silicon [1]-[3]. However, high switching frequency operation makes the two-level inverter more susceptible to the parasitic elements in the circuit such as stray inductances in the PCB circuit board. Moreover, high dV/dt and di/dt capability of WBG devices can aggravate the interaction between the top and bottom switches, leading to spurious/Miller turn-ON, which can eventually lead to current shoot through [1]-[2]. Further, the intrinsic body diode voltage drop of WBG devices is relatively higher compared with the purpose designed diodes, reducing the overall efficiency. Although, anti-paralleling a WBG based diode can help to alleviate body diode loss, but addition of an antiparallel diode increases the total output capacitance across the MOSFET, increasing the turn-ON switching loss. Lastly, from the topology perspective, the three-phase two-level inverter also requires deadtime between the top and bottom complementary switches to prevent crosstalk and current shoot through. However, current shoot-through can still happen with deadtime in some fault conditions [5].

The above-mentioned performance limitations of WBG devices in a standard three-phase two-level inverter are shown to be overcome through split-phase inverter topology, which comprises dissection version of phase-legs of a traditional two-level inverter [4]-[5]. The phase-legs are split to form P-Cell and N-cell with split inductors connected to mid-point of each of these cells on one side and shorted together on the other as shown in Fig. 1. The split-inductor isolates the top switch from its antiparallel diode and the bottom switch and vice versa. This arrangement offers various advantages. Firstly, it allows the inverter to operate with zero deadtime, which maximizes the energy transfer and improves the quality of the output waveforms. Secondly, the top and bottom switches need not to be placed near to each other as the stray inductance between the switches is the leakage inductance, which also serves as the split-inductance. Thirdly, the split arrangement results in reduced turn-on; slightly high turn-off but reduced overall switching loss in the power device as concluded in [6], increasing the overall efficiency of the inverter. Lastly, the EMI emissions of a split-phase inverter are lower compared with a standard two-level inverter leading to small size of the EMI filter [6]-[7].

However, decoupling between the top and bottom devices (Fig. 1) due to split inductors causes the mid-point voltages of P and N cells to rise and fall with a delay. This delay causes a transient voltage pulse to appear across the split inductors, inducing current spikes through the inductors during switching transition either from top to bottom or bottom to top switch. Intense current spikes can cause excessive core loss, reducing the overall efficiency of the inverter [11]-[12]. Further, the magnitude of the current spike depends on the value of split-inductors, output capacitances of the power devices and the type of load, which can be characterized by the Power Factor (PF).

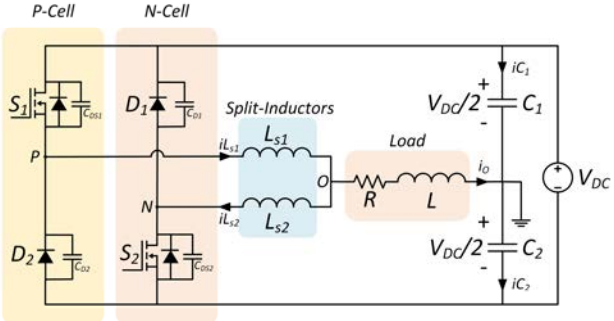


Fig. 1. Split-Phase Leg feeding an RL load.

This paper investigates the spike current phenomenon in split-phase inverters. Firstly, a base case of a single phase-leg is analyzed for zero and unity PF load and equivalent model is derived. The efficacy of the proposed model is then verified on a low voltage hardware prototype. Lastly, the model is extended to the full three-phase split-phase inverter.

II. Current Spikes in Phase-Leg

A. 0 PF (Inductive Load)

Fig. 2 shows the waveforms, divided into four intervals, at S_1 OFF → ON and S_2 ON → OFF switching transition for the phase-leg in Fig. 1, feeding a pure inductive load (0 PF) with positive i_O. The sign conventions of Fig. 1 are followed. The first subplot contains the voltages of node *P*, *O* and *N*. The voltages across the split inductors L_{s1} and L_{s2} are $v_P(t) - v_O(t)$ and $v_O(t) - v_N(t)$.

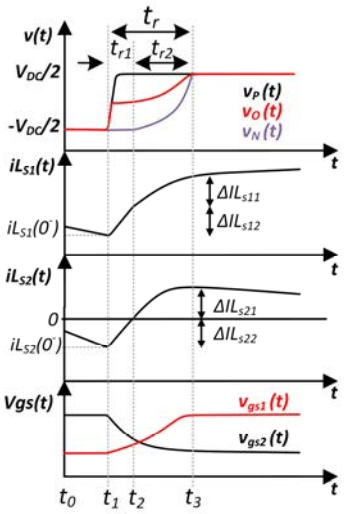
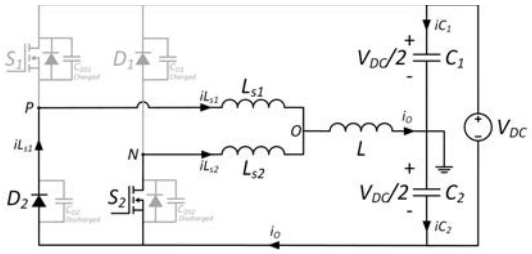
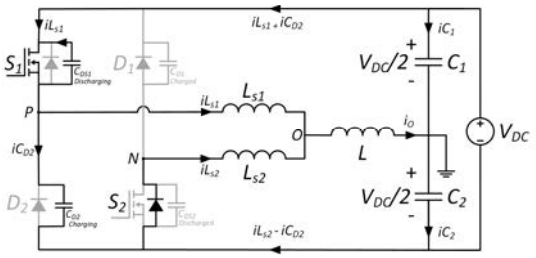


Fig. 2. Waveforms for S_1 OFF → ON and S_2 ON → OFF switching transition with 0 PF load.

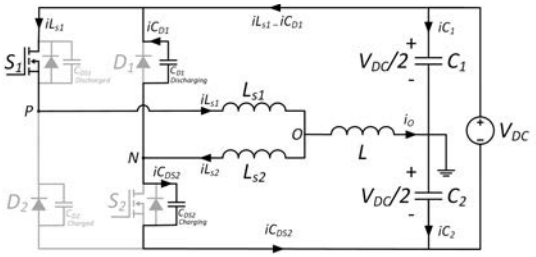
Fig. 3 illustrates the state of power semiconductor devices and direction of split inductor currents for each interval. As S_1 turns ON, the voltage of node *P* rises quickly to $+V_{DC}/2$ with dV/dt of S_1. However, the voltage of node N rises to $+V_{DC}/2$ with a delay t_r. The delay t_r is composed of two intervals $t_{r1} = t_2 - t_1$, and $t_{r2} = t_3 - t_2$. In both intervals a positive voltage pulse appears across L_{s1} and L_{s2} and the inductors experience a spike in current $\Delta iL_{S1} = \Delta iL_{S11} + \Delta iL_{S12}$ and $\Delta iL_{S2} = \Delta iL_{S21} + \Delta iL_{S22}$. The ΔiL_{S11} and ΔiL_{S21} spikes occur during the $t_1 \le t < t_2$ interval and ΔiL_{S12} and ΔiL_{S22} spikes occur during the $t_2 \le t < t_3$ interval according to Fig. 3.



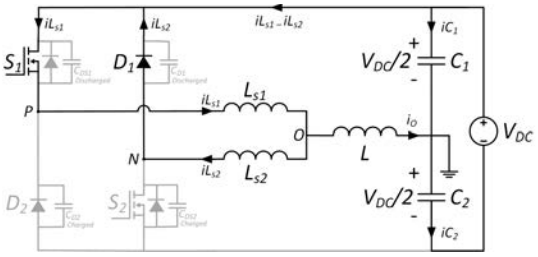
a) $t_0 \le t < t_1$



b) $t_1 \le t < t_2$ (ΔiL_{S11} & ΔiL_{S12})



c) $t_2 \le t < t_3$ (ΔiL_{S21} & ΔiL_{S22})



d)$t_3 \le t$

Fig. 3. Analysis of S_1 OFF → ON and S_2 ON → OFF switching transition.

1) ΔiL_{S11} and ΔiL_{S21} spikes during $t_1 \le t < t_2$

The occurrence of this interval entirely depends on the value of current $iL_{S2} = iL_{S2}(0^-)$ flowing through inductor L_{s2} at the start of the switching transition. If $iL_{S2}(0^-) < 0$ then as S_1 turns ON and S_2 turns OFF, iL_{S2} commutates from channel of S_2 to body diode of S_2 at $t = t_1$, clamping node *N* to $-V_{DC}/2$ while node *P* is clamped to $+V_{DC}/2$. This results in quick freewheeling that lasts till $t = t_2$ when iL_{S2} becomes zero. The freewheeling time t_{r1} can be estimated using (1), which depends on the initial condition $iL_{S2}(0^-)$, split inductance and the DC link voltage. With SPWM the value of $iL_{S2}(0^-)$ varies. No freewheeling occurs for $iL_{S2}(0^-) > 0$. The condition for $iL_{S2}(0^-) < 0$ can be derived from the equivalent circuit for the prior interval ($t_0 \le t < t_1$) as shown in Fig. 4. $iL_{S2}(0^-) < 0$ if the voltage $V_{Ls2} < 0$. For $V_{Ls2} > 0$, $iL_{S2}(0^-) > 0$ and no freewheeling occurs. The criteria for V_{Ls2} is summarized in (2).

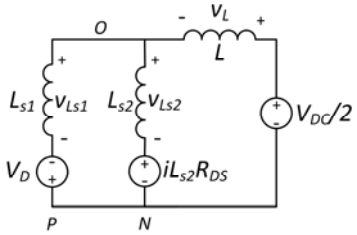


Fig. 4. Equivalent circuit for $t_0 \le t < t_1$ interval.

$$t_{r1} = \frac{L_{S2} iL_{S2}(0^-)}{V_{DC}/2} \quad (1)$$

$$V_{Ls2} = \frac{\left(\frac{V_{DC}}{2} - iL_{S2}R_{DS}\right)L_S^2 - (iL_{S2}R_{DS} + V_D)L_S L}{L_S^2 + 2L_S L}$$

$$iL_{S2}(0^-) > 0 \rightarrow V_{Ls2} > 0 \text{ if } L_s > \frac{(iL_{s2}R_{DS} + V_D)L}{\left(\frac{V_{DC}}{2} - iL_{s2}R_{DS}\right)} \quad (2)$$

$$iL_{S2}(0^-) < 0 \rightarrow V_{Ls2} < 0 \text{ if } L_s < \frac{(iL_{s2}R_{DS} + V_D)L}{\left(\frac{V_{DC}}{2} - iL_{s2}R_{DS}\right)}$$

2) ΔiL_{S12} and ΔiL_{S22} spikes during $t_2 \le t < t_3$

In this interval, the split inductors L_{s1} and L_{s2} interact with the output capacitances C_{D1} and C_{DS2} of D_1 and S_2 respectively. Fig. 5 shows the equivalent circuit. The voltage source $v_s(t)$ represents a $+V_{DC}/2$ step source, mimicking dV/dt of S_1. This interval lasts for time t_{r2} till the voltage of node *N* rises from the initial value of $v_N(0^-) = -V_{DC}/2$ to $+V_{DC}/2$. The rise time t_{r2} mainly depends on the initial value of $iL_{S2} = iL_{S2}(0^-)'$ at start of $t_2 \le t < t_3$ interval. $iL_{S2}(0^-)' = 0$ if freewheeling happens in the prior interval other wise $iL_{S2}(0^-)' > 0$. The spike current magnitudes ΔiL_{S12} and ΔiL_{S22} and t_{r2} decreases as $iL_{S2}(0^-)'$ increases from zero to a positive value. For $iL_{S1}(0^-)' = iL_{S2}(0^-)' = 0$, ΔiL_{S12}, ΔiL_{S22} and t_{r2} can be approximated using (3), (4) and (5) with $L_{s1} = L_{s2} = L_s$.

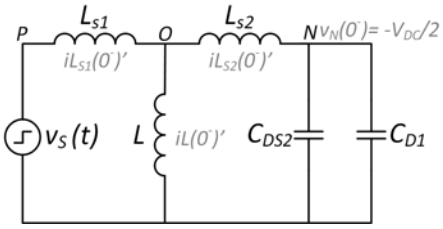


Fig. 5. Equivalent circuit for $t_2 \le t < t_3$ interval.

$$\Delta iL_{s22} = \frac{(C_{DS2}+C_{D1})V_{DC}}{2}\left(\frac{2L+L_s}{L_s+L}\right)\sqrt{\frac{L_s+L}{(L_s^2+2L_sL)}}\, sin\left(\left(\sqrt{\frac{L_s+L}{(L_s^2+2L_sL)}}\right)t_r\right) \quad (3)$$

$$\Delta IL_{s12} = \frac{1}{L_s}\int_0^{t_{r2}} v_s(t) - v_{o(t)}.dt \quad (4)$$

$$t_{r2} = cos^{-1}\frac{\left(-\frac{L_S}{L_S+L}\right)}{\sqrt{\frac{L_S+L}{(L_S^2+2L_SL)(C_{DS2}+C_{D1})}}} \quad (5)$$

The current spike analysis also applies to S_2 OFF → ON and S_1 ON → OFF switching transition with negative i_O by interchanging the roles of L_{s1} and L_{s2} in (1) till (7) with $-V_{DC}/2$ step source and $v_N(0^{-1}) = V_{DC}/2$ in Fig. 5. Further the derived model is also applicable for RL load, with load *L* in Fig. 4 replaced with *RL*.

B. 1 PF (Resistive Load)

With resistive load *R*, the equivalent circuit becomes an RL circuit (Fig. 6). For S_1 OFF → ON and S_2 ON → OFF switching transition, the voltage across the load v_L is given by (6) where $iL_{S1}(0^-)$ and $iL_{S2}(0^-)$ are the initial values of inductor currents with $L_{s1} = L_{s2} = L_s$. Further, like the inductive load case (Fig. 2), the voltage of node *N* rises with a short delay t_r, which can be computed by finding the time it takes for node voltage N, v_N in (7) to rise from $v_N(0^-) = -V_{DC}/2$ to $+V_{DC}/2$ for the equivalent circuit in Fig. 5 with R replaced with L. Contrary to the inductive load, the current through split inductors during time interval t_r does not spikes up. The current rises (L_{s1}) and falls (L_{s2}) with a time constant $2R/L_s$ of the equivalent RL circuit in Fig. 6 with small ΔiL_{S1} and ΔiL_{S2} as shown in (8) and (9). This concept can also be extended to S_2 OFF → ON and S_1 ON → OFF switching transition by interchanging the roles of L_{s1} and L_{s2} in (6) through (9) and inverting the sign of $V_{DC}/2$ source and $v_N(0^-)$ in (7).

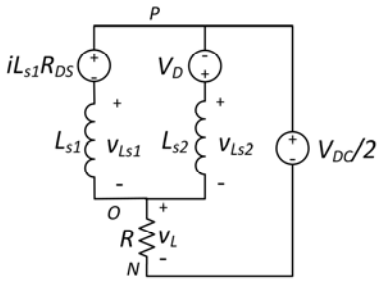


Fig. 6. Equivalent circuit with R load for S_1 OFF → ON and S_2 ON → OFF transition.

III. HARDWARE PROTOTYPE VALIDATION

A hardware prototype for split-phase leg is built and tested using two CREE's KIT-CRD-8FF65P SiC modules [13] to validate the proposed model, shown in Fig. 7. The fundamental and switching frequencies f and f_s are set to 600 Hz and 72 kHz respectively with 0.7 modulation index. The DC link voltage is set to 200 V. Two cases of split inductances $L_{s1} = L_{s2} = 10\ \mu H$ and $L_{s1} = L_{s2} = 220\ \mu H$ are considered for testing. Continuous tests are performed for both purely resistive ($R = 50\Omega$) and inductive ($L = 4.58$ mH) loads. The experimental and proposed model results for L_{s2} current spike ΔiL_{S2} at S_1 OFF → ON and S_2 ON → OFF switching transition with positive i_O are summarized in Fig. 8. The theoretical results match with the experimental results, justifying the efficacy of the model.

For inductive load (Fig. 8 a and b), the current spike ΔiL_{S2} during switching transition includes both t_{r1} and t_{r2} intervals (Fig. 2) for $L_{s1} = L_{s2} = 10\ \mu H$. However, for $L_{s1} = L_{s2} = 220\ \mu H$, the freewheeling interval t_{r1} in Fig. 3 b) is absent as the initial inductor current $iL_{S2}(0^-) > 0$ at the start of the switching transition according to (2). Further, the spike amplitude for $L_{s1} = L_{s2} = 220\ \mu H$ is considerably small and around 28 times lower than for $L_{s1} = L_{s2} = 10\ \mu H$. For resistive load, the L_{s2} falls slightly with time constant $2R/L_s$.

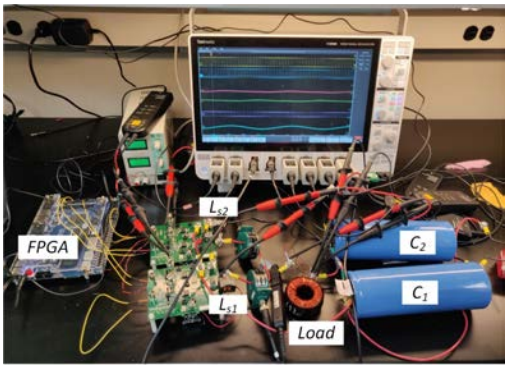


Fig. 7. Experimental Setup.

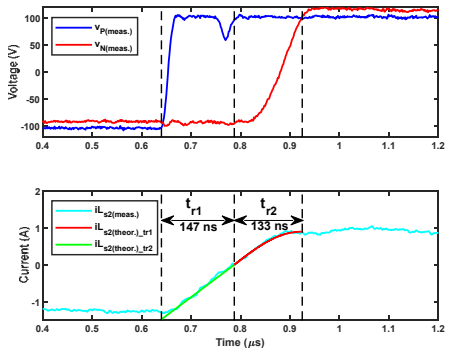
$$v_L(t) = \left(\frac{V_{DC}}{2} - 0.5(iL_{S1}R_{DS} - V_D)\right)\left(1 - e^{-\frac{2R}{L_S}t}\right) + R\left(iL_{S1}(0^-) + iL_{S2}(0^-)\right)e^{-\frac{2R}{L_S}t} \tag{6}$$

$$v_N(t) = \mathcal{L}^{-1}\left\{\frac{\frac{RV_{DC}}{2s} + RL_S iL_{S1}(0^-) + \left(sL_S^2 + RL_S\right)iL_{S2}(0^-) + (C_{DS2}+C_{D1})L_S\left(s^2L_S + 2Rs\right)v_N(0^-)}{s^3L_S^2(C_{DS2}+C_{D1}) + 2s^2RL_S(C_{DS2}+C_{D1}) + sL_S + R}\right\} \tag{7}$$

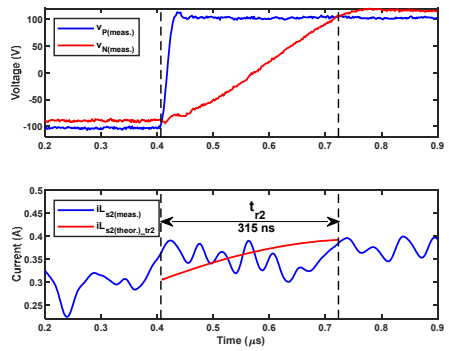
$$v_N(0^-) = -\frac{V_{DC}}{2}$$
$$v_N(t_r) = +\frac{V_{DC}}{2}$$

$$\Delta iL_{S1} = \left(\frac{V_{DC}}{2R} - iL_{S1}(0^-)\right)\left(1 - e^{-\frac{2R}{L_S}t_r}\right) \tag{8}$$

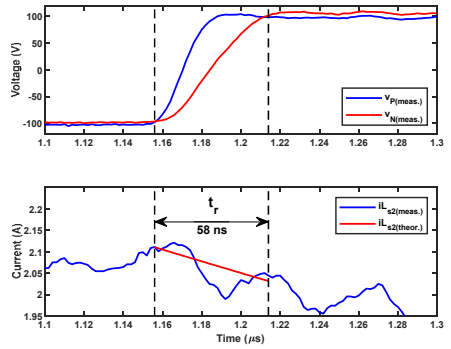
$$\Delta iL_{S2} = iL_{S2}(0^-)\left(1 - e^{-\frac{2R}{L_S}t_r}\right) \approx \frac{V_{DC}}{2R}\left(1 - e^{-\frac{2R}{L_S}t_r}\right) \tag{9}$$



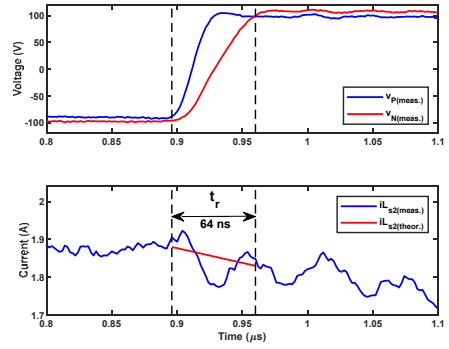
a) $L_{s1} = L_{s2} = 10\ \mu H$ for L load with $\Delta iL_{S2} = 2.10\ A$.



b) $L_{s1} = L_{s2} = 220\ \mu H$ for L load with $\Delta iL_{S2} = 76\ mA$.



c) $L_{s1} = L_{s2} = 10\ \mu H$ for R load with $\Delta iL_{S2} = 63\ mA$.



d) $L_{s1} = L_{s2} = 220\ \mu H$ for R load with $\Delta iL_{S2} = 45\ mA$.

Fig. 8. Experimental results for L_{s2} current spikes ΔiL_{S2} at S_1 OFF → ON and S_2 ON → OFF switching transition.

IV. Extension to Three-Phase

The spike model derived for the phase-leg can be extended to three-phase configuration, shown in Fig. 9, by transforming the circuit at switching transition into the equivalent circuits for the phase-leg in Fig. 4 and 5.

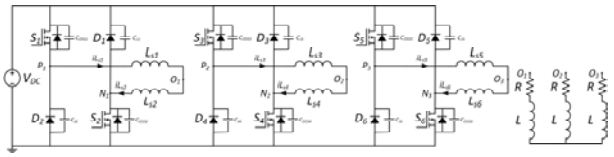


Fig. 9 Three-phase split-phase inverter feeding an RL load.

For SPWM, switching transition happens in one phase-leg at a time. The other phases are either clamped to V_{DC} + or V_{DC} – (power ground). Hence, for deriving the equivalent circuits for spike current estimation for three-phase configuration, the S_1 OFF → ON and S_2 ON → OFF switching transition for the single phase-leg (Fig. 2) can be extended to each phase in Fig. 9 for both inductive and resistive loads. The proceeding analysis focuses on S_1 OFF → ON and S_2 ON → OFF transition in phase A of the inverter.

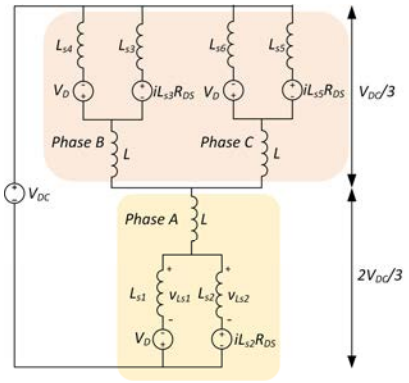
A. 0 PF (Inductive Load)

For inductive three-phase load, the split inductors L_{s1} and L_{s2} in phase A experience a spike in current $\Delta iL_{S1} = \Delta iL_{S11} + \Delta iL_{S12}$ and $\Delta iL_{S2} = \Delta iL_{S21} + \Delta iL_{S22}$. The ΔiL_{S11} and ΔiL_{S21} spikes occur during the $t_1 \le t < t_2$ interval (freewheeling) and ΔiL_{S12} and ΔiL_{S22} spikes occur during the $t_2 \le t < t_3$ interval, like for single phase-leg in Fig. 3.

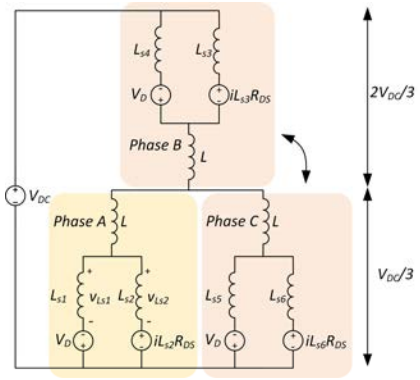
1) ΔiL_{S11} and ΔiL_{S21} spikes during $t_1 \le t < t_2$

In this interval, the current through L_{s2} freewheels through the body diode of S2 if $iL_{S2}(0^-) < 0$. Depending upon the states of the switches S3 and S4 in phase B and S5

and S6 in phase C, two configurations (Fig. 10) for $t_0 \le t < t_1$ prior to $t_1 \le t < t_2$ interval are possible for determining $iL_{S2}(0^-)$. The expressions (1) and (2) can be modified to cater these cases by replacing $V_{DC}/2$ with $2V_{DC}/3$ for Fig. 10 a) and with $V_{DC}/3$ for Fig. 10 b).



a) Equivalent circuit with phase B and C clamped to V_{DC} +.



b) Equivalent circuit with phase B clamped to V_{DC} + and phase C clamped to V_{DC} − and vice versa.

Fig. 10. Possible equivalent circuits for $t_0 \le t < t_1$ interval.

2) ΔiL_{S12} and ΔiL_{S22} spikes during $t_2 \le t < t_3$

In this interval, similar to single phase-leg, the split inductors L_{s1} and L_{s2} interact with the output capacitances C_{D1} and C_{DS2} of D_1 and S_2 respectively. The equivalent circuit is shown in Fig. 11, which is simplified and matched to the circuit in Fig. 5, assuming equal split inductance L_s in all phases. The expressions (3) to (5) can be modified to cater this interval by replacing L and $V_{DC}/2$ in (3) till (5) with L_{eq} and V_{DC} respectively.

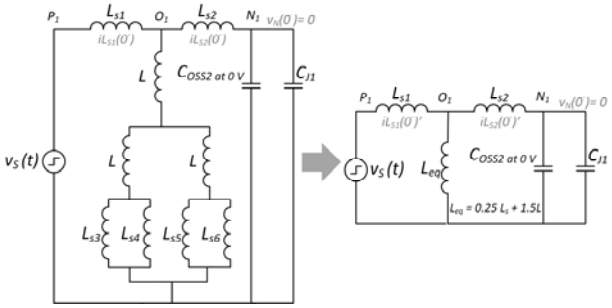


Fig. 11. Equivalent circuit for $t_2 \le t < t_3$ interval.

C. 1 PF (Resistive Load)

The circuits in Fig. 10 also apply to resistive load with L replaced with R, forming an RL circuit with time constant $2R/L_s$ for each phase. The equivalent circuit for phase A after switching transition, derived from Fig. 10, is shown in Fig. 12. Depending upon the states of the switches S3 and S4 in phase B and S5 and S6 in phase C the DC source in Fig. 12 is either $V_{DC}/3$ or $2V_{DC}/3$. The circuit response can be modelled using expressions (6) till (9) with $V_{DC}/2$ replaced by $V_{DC}/3$ or $2V_{DC}/3$ and $v_N(0^-)$ set to 0.

Lastly, this concept is also applicable to S_2 OFF → ON and S_1 ON → OFF switching transition by interchanging the roles of L_{s1} and L_{s2} in (6) through (9) and inverting the sign of source ($V_{DC}/3$ or $2V_{DC}/3$) in (7).

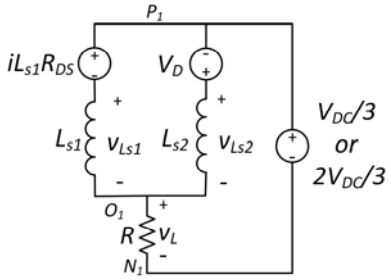


Fig. 12. Equivalent circuit for phase A with R load.

V. Conclusion

Decoupling between top and bottom devices in a split-phase inverter during switching transition leads to current spike in split inductors. Depending upon inverter parameters, the magnitude of the spikes can be exorbitant leading to excessive core loss. An analysis of current spikes in split-phase inverters is presented in this paper for phase-leg and three-phase configuration. It is concluded that the spike magnitude depends on the values of split inductors, device parasitic capacitance and the type of load. It is highest for inductive load and negligible for resistive load. Further, increasing split inductance is effective in lowering the magnitude of the spikes as the model and experimental results show. However, the overall size of the magnetics is increased, lowering the power density of the inverter, and raising concerns for near-field magnetic emission, which induces noise and affects the control circuitry.

Acknowledgment

This work was supported by Oak Ridge National Laboratory (ORNL) funded through the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira. The authors would also like to acknowledge the National Science Foundation (NSF Award No. 1846917) for lending financial support for this work.

References

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, May 2014.

[2] A. B. Mirza, A. I. Emon, S. S. Vala and F. Luo, "Noise Immune Cascaded Gate Driver Solution for Driving High Speed GaN Power Devices," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 5366-5371.

[3] A. I. Emon *et al*., "Design and Optimization of 650V/60A Double-Sided Cooled Multichip GaN Module," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2313-2317

[4] S, Li., "Packaging Design of IGBT Power Module Using Novel Switching Cells. " PhD dissertation, University of Tennessee, 2011.J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

[5] P. Sun, C. Liu, J. Lai, C. Chen and N. Kees, "Three-Phase Dual-Buck Inverter With Unified Pulsewidth Modulation," in *IEEE Transactions on Power Electronics,* vol. 27, no. 3, pp. 1159-1167, March 2012.

[6] Q. Yan, X. Yuan, Y. Geng, A. Charalambous and X. Wu, "Performance Evaluation of Split Output Converters With SiC MOSFETs and SiC Schottky Diodes," in *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 406-422, Jan. 2017.

[7] H. Li, S. Munk-Nielsen, S. Bęczkowski and X. Wang, "SiC MOSFETs based split output half bridge inverter: Current commutation mechanism and efficiency analysis," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 1581-1588.

[8] S. Bęczkowski, H. Li, C. Uhrenfeldt, E. Eni and S. Munk-Nielsen, "10kV SiC MOSFET split output power module," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-7.

[9] B. Chen, P. Sun, C. Liu, C. Chen, J. Lai and W. Yu, "High efficiency transformerless photovoltaic inverter with wide-range power factor capability," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 575-582.

[10] A. I. Emon, Z. Yuan, A. B. Mirza, A. Deshpande, M. U. Hassan and F. Luo, "1200 V/650 V/160 A SiC+Si IGBT 3L Hybrid T-Type NPC Power Module With Enhanced EMI Shielding," in *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13660-13673, Dec. 2021.

[11] H. Matsumori, T. Shimizu, K. Takano and H. Ishii, "Evaluation of Iron Loss of AC Filter Inductor Used in Three-Phase PWM Inverters Based on an Iron Loss Analyzer," in *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3080-3095, April 2016.

[12] T. Shimizu and S. Iyasu, "A Practical Iron Loss Calculation for AC Filter Inductors Used in PWM Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2600-2609, July 2009.

[13] "KIT-CRD-8FF65P Application Note", Wolfspeed, 2020. [Online]. Available: https://cms.wolfspeed.com/app/uploads/2020/12/kit_crd_8ff65p_application_note.pdf.