

Exploring Multiple Pathways to Low TDD GaP/Si for III-V/Si Photovoltaics

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Abstract— Threading dislocation density (TDD) is a key parameter that commonly limits the performance of epitaxially integrated III-V/Si photovoltaics. The GaP/Si epitaxial bridge is a widely studied III-V on Si integration pathway, and recent advances have realized low- 10^6 cm^{-2} TDD in *n*-GaP/Si templates that can be integrated in III-V/Si PV designs amenable to efficiencies well beyond single-junction Si. However, continued development and scaling of III-V/Si PV will ultimately rely on a deeper understanding of dislocation evolution in GaP/Si and will require more process flexibility than has heretofore been demonstrated. Thus, this work demonstrates multiple pathways toward achieving-low 10^6 cm^{-2} TDD, through which we can gain both substantial fundamental understanding of GaP/Si integration and can achieve the needed process flexibility to enable scalable production.

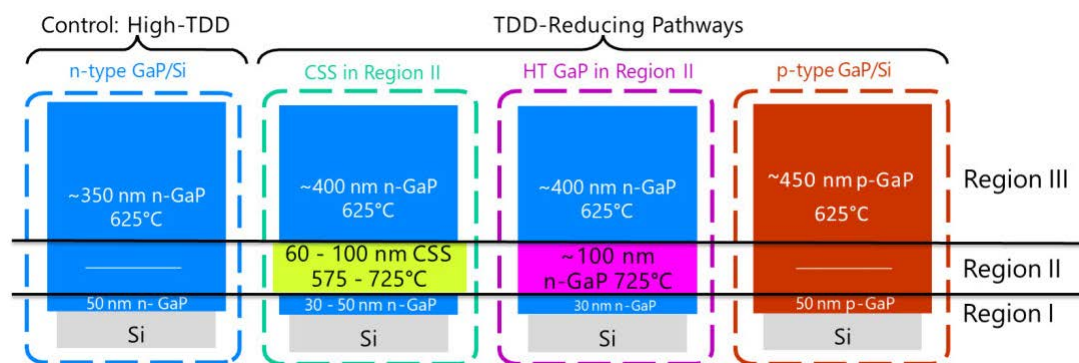
I. SUMMARY

Monolithically integrated III-V/Si tandem photovoltaics are a promising avenue for high-efficiency, low-cost PV cells. Up to this point, monolithic, epitaxial III-V/Si PV development has yielded impressive rates of efficiency improvement, as demonstrated by the authors [1], and others [2], [3]. The next critical step in this development requires reduction of the threading dislocation density (TDD) in the III-V material layers [4]. Much of the TDD stems from the often problematic GaP/Si integration, wherein the heterovalency, $\sim 0.5\%$ lattice mismatch at growth temperature, and poor GaP dislocation dynamics all contribute to high TD introduction rates and thus sub-par metamorphic III-V upper junction performance [5], [6].

The work briefly described herein encompasses various epitaxial pathways in an MOCVD growth environment that we have thus far demonstrated to enable relaxed GaP/Si with TDD $< 5 \times 10^6 \text{ cm}^{-2}$. The parameters explored in these MOCVD

growth studies include growth temperature at either 575°C (low temperature or ‘LT’), 625°C (MT), or 725°C (HT) and dopant polarity as the primary dependent variables. The TDD reduction pathways are summarized in Fig. 1, highlighting 3 thickness regions over which dislocation evolution behavior is distinct. Within this effort, we have explored in detail the impact of compressively strained superlattice (CSS) structures, as described in our previous work [7], and high temperature growth within Region II, as well as effect of the fermi level (dopant polarity) on dislocation evolution in GaP films on Si. Post-growth characterization of dislocations was conducted via electron channeling contrast imaging (ECCI) similar to prior reports [8]. This effort has identified critical aspects of dislocation evolution in the distinct regions of the GaP relaxation process to realize new pathways toward low-TDD GaP/Si that may be applicable to a wider array of GaP/Si integration strategies [9], [10].

The TDD of selected samples at a few thickness points are plotted in Fig. 2. While TDD at the onset of dislocation introduction in 50 nm GaP films is essentially equivalent, each pathway has a unique TDD evolution throughout the growth. For example, by growing Region II using HT-GaP, the TDD is initially very low around $1 \times 10^5 \text{ cm}^{-2}$, though growth throughout Region III introduces TDD at a similar rate as the control in this latter stage. Both the CSS and *p*-GaP strategies reduce TDD introduction in Region III primarily, though the dislocation introduction in early stages of growth is not as low, suggesting that increasing TD glide is more important in this latter growth stage as the film relaxes fully.



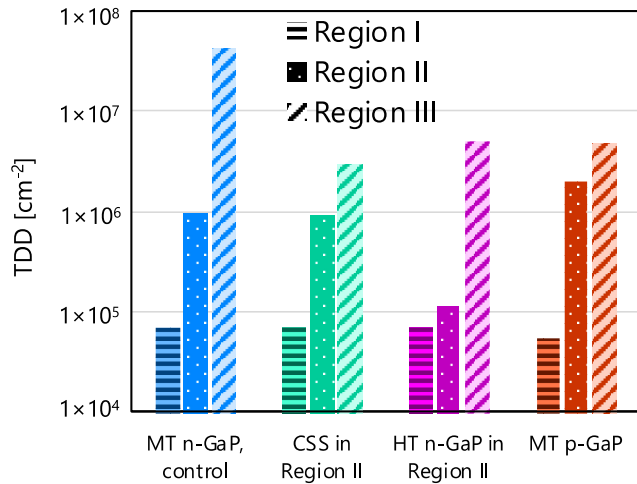


Fig. 2. Resultant TDD in each pathway after growth of the indicated region.

II. CONCLUSIONS

Multiple pathways demonstrating low TDD GaP/Si have been demonstrated. Key regions of the GaP/Si growth were identified and the disparate dislocation behavior in each were studied via comparison between each general strategy. Further optimization within each pathway could likely yield lower TDD in each, providing a variety of options for III-V/Si PV growth. This flexibility, in turn, may help to address technoeconomic

issues (such as thermal budget, Si bottom cell architecture, growth on non-planar Si, etc.) related to low-cost III-V/Si PV growth and design.

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