Development of Low-TDD $GaAs_yP_{1-y}$/GaP/Si Metamorphic Materials for High-Efficiency III-V/Si Photovoltaics

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Abstract*— *Metamorphic III-V/Si materials with low threading dislocation density (TDD) are critical to realizing high-efficiency III-V/Si multijunction photovoltaics. In pursuit of a dual junction III-V/Si design with a $GaAs_{0.75}P_{0.25}$ top junction epitaxially integrated on a Si bottom junction, we report on progress made in the development of GaP/Si and $GaAs_yP_{1-y}$/Si materials with significantly reduced TDD. Using a tightly integrated study of fundamental dislocation dynamics, rapid electron microscopy based feedback on dislocation populations, and MOCVD process development, we have fully re-engineered the GaP on Si growth process. Our new approach results in a TDD of 7×10^4 cm^{-2} for 50 nm thick films. Implementation of a novel dislocation glide enhancing heterostructure then enabled subsequent growth of fully-relaxed, 500 nm total thickness n-GaP with a TDD of 2.4×10^6 cm^{-2}. When applied to the production of full $GaAs_{0.75}P_{0.25}$/Si tandem solar cell structures, but without any significant optimization thus far, this low TDD is effectively maintained, yielding a terminal TDD of only 3.0×10^6 cm^{-2}, sufficient to support high photovoltaic performance.

I. Introduction

Monolithic III-V/Si photovoltaics offer an attractive combination of tunable, high-performance III-V alloys with inexpensive and processible Si platforms. Non-monolithic III-V//Si technologies have thus far achieved high AM1.5G efficiencies of up to 35.9% for mechanically-stacked [1] and 34.1% for wafer-bonded devices [2]. However, the ultimate costs and scalability may be limited by the additional processing and costs required for fabrication. Conversely, monolithic, fully-epitaxial III-V/Si tandem devices have been demonstrated at 23.4% AM1.5G for GaAsP/Si two-junction (2J) [3] and 24.3% for GaInP/GaAs/Si three-junction architectures [2], [4].

At present, the performance of monolithic III-V/Si tandems are limited by excess threading dislocation density (TDD), which generally serves as a distribution of spatially-localized recombination centers that reduce diffusion length in the III-V absorber. The relationship between TDD and minority carrier lifetime has, for example, been studied in GaAs across a range of TDD [5]. High TDD leads to reduced current collection, voltage, and fill factor of the top cell, greatly limiting the overall photovoltaic efficiency. For the GaAsP/Si architecture of interest herein, a TDD of 2×10^6 cm^{-2} is projected to enable high-efficiency 1.72 eV top cells with V_{OC} of ~1.3 V and J_{SC} of >18 mA/cm^{-2}, sufficient for the production of ≥30% tandems [6].

Prior work by the authors and other researchers have found that the excess TDD within the monolithic structures that utilize a $GaAs_yP_{1-y}$/GaP/Si nucleation and compositionally graded buffer (GB) approach, such as the present GaAsP/Si 2J structure, is found to originate at the GaP/Si nucleation interface. The strong potential for the formation of nucleation related defects (e.g. antiphase disorder, stacking faults, etc.), non-negligible (~0.5% at growth temperature) lattice misfit, and low GaP dislocation glide velocity all complicate the production of low TDD GaP/Si virtual substrates. Furthermore, while growth of $GaAs_yP_{1-y}$ GBs with $<2\times10^6$ TDD on bulk GaP substrates is well-demonstrated [7], GBs produced on GaP/Si tend to exhibit higher TDD. Much work has been conducted to develop high-quality GaP/Si virtual substrates [8]–[10], yet the connection between growth conditions/processes and dislocation evolution in $GaAs_yP_{1-y}$/Si is not yet well understood.

To this end, we are investigating GaP/Si and $GaAs_yP_{1-y}$/Si heteroepitaxial structures using electron channeling contrast imaging (ECCI, [11]) to provide rapid feedback on dislocation populations and dynamics, with the ultimate goal of developing scientifically-informed, low-TDD MOCVD growth processes. ECCI is an SEM-based technique that provides large-scale imaging with selective defect contrast similar to plan-view TEM, without the arduous sample preparation. We have developed techniques for acquisition and analysis of large-scale (over 10,000 μm^2) ECCI micrographs to enable accurate quantification of dislocation glide and nucleation dynamics versus a wide variety of growth conditions [12]. These correlative efforts have enabled targeted TDD reduction throughout the $GaAs_yP_{1-y}$/GaP/Si structure, ultimately resulting in a TDD of $3.0 \pm 0.6 \times10^6$ cm^{-2} measured in $GaAs_{0.75}P_{0.25}$ solar cell layers of a full 2J device structure grown on Si.

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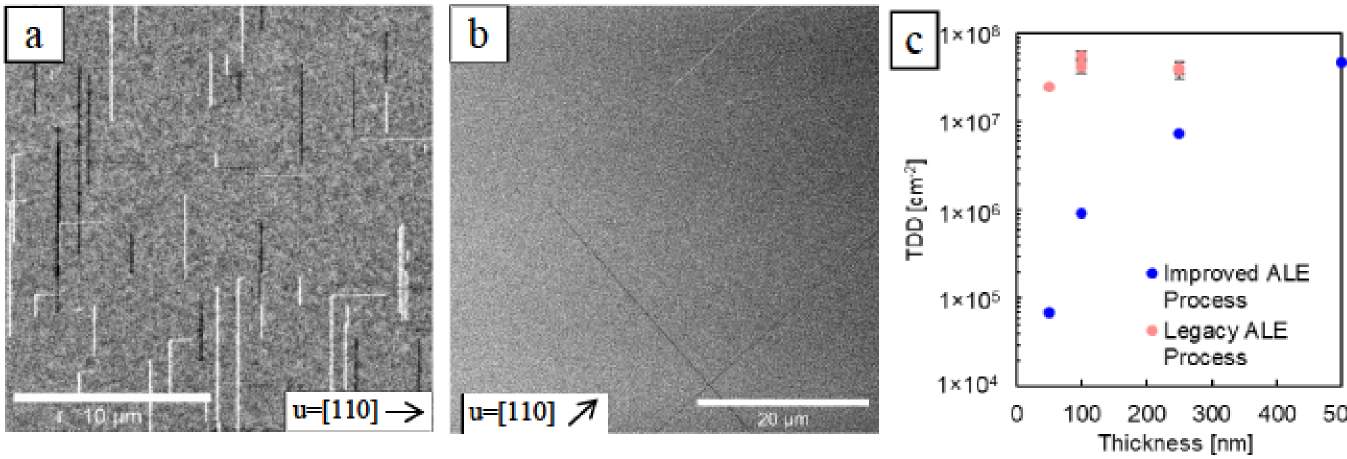

Fig. 1. ECCI micrographs using g = (400) depicting interfacial misfit dislocations under a) 50 nm GaP film with non-optimized nucleation conditions showing high nucleation and poor glide, b) 50 nm and c) 100 nm GaP film with improved nucleation conditions showing low initial nucleation and rapid glide. A histogram of misfit lengths extracted from ECCI montages verifies misfit lengths approaching >1 mm.

II. Approach

Epitaxial $GaAs_yP_{1-y}$ and GaP samples were produced in an Aixtron 3×2" close-coupled showerhead MOCVD reactor on either Si(100) offcut 2° toward [011]. *In-situ* reflectance/pyrometry was utilized for growth rate and temperature monitoring. Precusors employed were trimethylgallium (TMGa), triethylgallium (TEGa), phosphine (PH_3), tert-butylphosphine (TBP), and arsine (AsH_3). Silane (SiH_4) and diethylzinc (DEZn) were used for *n*- and *p*-type doping, respectively.

Si wafers were wet chemically cleaned and oxide etched prior to loading into the MOCVD. Si surface pretreatment was conducted via high-temperature annealing under dilute SiH_4. The substrates were then cooled and atomic layer epitaxy (ALE) based GaP nucleation commenced, similar to prior reports [8]. To investigate the impact of nucleation process on dislocation formation and evolution, several ALE process parameters were varied, including (but not limited to) the number of ALE cycles, purge time between ALE pulses, and the initiating precursor. After depositing 5-15 ALE layers, the substrate temperature was ramped up for "bulk" *n*-GaP growth to a total thickness of typically 50 – 100 nm. Depending on the target structure, *n*-GaP and/or *n*-$GaAs_yP_{1-y}$ layers were then grown on the GaP/Si templates. Compositionally-stepped $GaAs_yP_{1-y}$ GBs were also grown with an average misfit introduction rate of 0.5 – 1.0 %/µm and ~3% As per step. Photovoltaic device structures, including tunneling diodes [13], were grown thereafter according to details found in prior reports [14], [15].

Post-growth ECCI characterization was performed in a Thermo Scientific Apreo SEM with parameters similar to prior reports [11]. Additional work included atomic force microscopy (AFM) and high-resolution X-ray diffractometry (XRD).

III. Results and Discussion

A. GaP/Si Nucleation Process Development and Optimization

Fig. 1a shows an ECCI micrograph of a 50 nm thick GaP/Si sample produced with the legacy ALE process conditions, originally ported from MBE [8]. Here, **g** = (400) diffraction conditions are used to image the misfit dislocation segments along both [110] and $[\bar{1}10]$ line directions; at this thickness, the threading segments bounding each misfit are typically difficult to differentiate from the strong contrast of interfacial misfit segments. At 50 nm, just above the critical thickness for dislocation glide, the misfit dislocation segments using the legacy nucleation process are found to be short and numerous, a highly non-ideal result leading to an effective TDD of ~2×10^7 cm^{-2}, despite being far from fully relaxed.

Films produced using the new ALE nucleation process, based on optimization of the parameters noted in Section II, exhibited substantially more ideal dislocation evolution. ECCI imaging (Fig. 1b) of samples produced by the improved ALE shows sparse, long misfits at the same 50 nm film thickness. Here, the TDD is ~7×10^4 cm^{-2}, which is over 2 orders of magnitude reduced from the legacy process. The mechanism behind this drastic impact on the dislocation nucleation and evolution is still under investigation.

B. Fundamental Dislocation Evolution Investigation

Thicker growths (from 50 – 500 nm) of GaP/Si using each ALE process were then studied. Fig. 1c details the TDD measured via ECCI as a function of growth thickness for these samples. For the legacy process, the majority of the dislocations appear to nucleate all at 50 nm, just at the onset of critical thickness, possibly suggesting a reduced energy barrier to nucleation or an increased barrier to glide. Interestingly, in the improved ALE case nucleation occurs more gradually, but eventually catches up to the TDD of the legacy process at around 500 nm total thickness. While it appears that excess dislocation nucleation is eliminated at the onset of critical thickness for the new process, the continual nucleation throughout the growth suggests that glide (which is already predicted to be slow, especially in *n*-GaP [16]) is unable to effectively relax the increasing epilayer strain, thus nucleation gradually proceeds.

To increase the effective glide velocity, thereby mitigating excess nucleation, a glide-enhancing heterostructure was developed and implemented within the thick (500 nm) *n*-GaP/Si

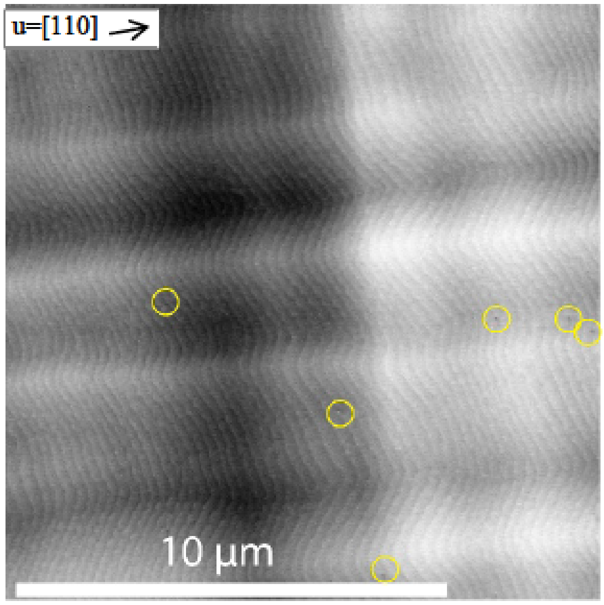

Fig. 2. ECCI micrographs using g = (400) depicting threading dislocations at a density of around 3 $\times 10^6$ cm^{-2} in $GaAs_{0.75}P_{0.25}$ top cell layers.

growth structure. As a result, fully relaxed *n*-GaP/Si samples with TDD as low as $2.4 \pm 0.4 \times 10^6$ cm^{-2} were realized. Details on this structure will be provided in a forthcoming publication.

C. Low-TDD $GaAs_{0.75}P_{0.25}$ Materials on Si

Full 2J device structures (including $GaAs_{0.75}P_{0.25}$ top cell, tunnel diode, and GB) were produced on the improved GaP/Si virtual substrates to investigate further TDD evolution. No significant change in TDD was observed via ECCI counting when varying the misfit rate of the GB from 0.5% μm^{-1} to 1.0% μm^{-1}, thus no other effort toward GB optimization has yet been made. With this new structure, TDD values of $3.0 \pm 0.6 \times 10^6$ cm^{-2} in $GaAs_{0.75}P_{0.25}$ top cell layers have been demonstrated. Fig. 2 presents a representative ECCI image from this structure, showing the low density of threading dislocations and the smooth surface that typically results. The aforementioned $\lesssim 2 \times 10^6$ cm^{-2} is now within reach with, and optimization of the grading structure is underway to achieve this goal.

Conclusions

To date we have demonstrated remarkable progress toward understanding and controlling dislocation evolution at nearly every point within the GaAsP/GaP/Si heteroepitaxial system. At the initial interface, low-TDD GaP/Si (reduced by >100×) was realized via careful changes to the ALE process. During further growth of *n*-GaP, regions of excess nucleation were identified and TDD introduction was mitigated through a glide-enhancing structure. Further growth of a full $GaAs_yP_{1-y}$ photovoltaic structure with TDD values of $3.0 \pm 0.6 \times 10^6$ cm^{-2} was realized by incorporation on low-TDD GaP/Si.

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