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# Nonvolatile Reconfigurable 2D Schottky Barrier Transistors

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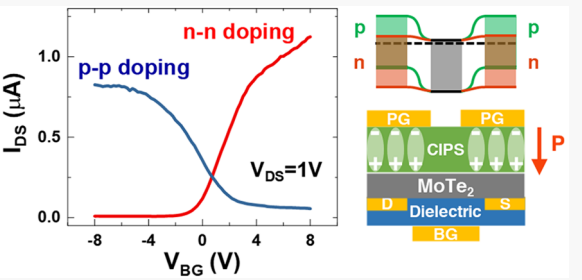
**ABSTRACT:** Nonvolatile reconfigurable transistors can be used to implement highly flexible and compact logic circuits with low power consumption in maintaining the configuration. In this paper, we build nonvolatile reconfigurable transistors based on 2D $CuInP_2S_6/MoTe_2$ heterostructures. The ferroelectric polarization-induced electron and hole doping in the heterostructure are investigated. By introducing the ferroelectric doping into the source/drain contacts, we demonstrate reconfigurable Schottky barrier transistors, whose polarity (n-type or p-type) can be dynamically programmed, where the configuration is nonvolatile in nature. These transistors exhibit a tunable photoresponse, where the n−n doping state leads to negative photocurrent, whereas the p−p doping state gives rise to a positive photocurrent. The transistor with asymmetric (n−p or p−n) contacts exhibits a strong photovoltaic effect. These reconfigurable logic and optoelectronic transistors will enable a new type of device fabric for future computing systems and sensing networks.




**KEYWORDS:** *Reconfigurable logic transistor, 2D ferroelectric heterostructure, copper indium thiophosphate ($CuInP_2S_6$), molybdenum ditelluride ($MoTe_2$)*



## INTRODUCTION

A key challenge of modern computing systems is the "memory bottleneck", where system performance is limited by the time and power required to access memory rather than the computation itself. New devices, circuits, and architectures are needed to reduce the energy and latency related to the data transportation between the memories and logic units. In this regard, reconfigurable transistors are a promising technology, where the polarity (n-type or p-type) of the transistors can be programmed during run-time. This device-level reconfiguration will also allow the functionality of the logic circuit to be dynamically modified during operation. Thus, compared to conventional computing approaches, electronic circuits built with reconfigurable transistors provide higher flexibility and efficient information processing for various applications.[1−4] The nonvolatile states can also be used for data storage, which enables in-memory computing.[5−7] Moreover, different reconfigurable states share the same circuit layout, so that the exact functions of circuit units are immune to hardware hacking.[8−11]

In traditional CMOS technology, the polarity of a transistor is determined by the nature of physical doping in the source/drain regions; thus, it is impossible to change the polarity of a CMOS transistor after fabrication. In contrast, transistors with Schottky contacts allow the injection of both electrons and holes into the channel without requiring heavy doping in the source/drain regions. These Schottky-barrier transistors are inherently ambipolar with tunable polarity of charge carriers in the channel. Reconfigurable Schottky-barrier transistors utilizing 2D materials and Si nanowires have been demonstrated recently.[11−17] These transistors feature Schottky contacts for the source and drain, and small bandgap semiconductors as the channel with a bandgap between 0.3 and 1.3 eV. Electrostatic gating is adopted to tune the Fermi level in the semiconductor and the Schottky barrier height of the contact, thus promoting the injection of both electrons and holes at the Schottky contacts. The doping from electrostatic gating is introduced after fabrication, which enables runtime reconfigurability. However, these devices rely on a constant supply of external voltage to provide electrostatic doping, which raises energy consumption and reliability concerns. Therefore, nonvolatile reconfiguration is necessary to simultaneously achieve run-time reconfiguration and low power consumption while maintaining the configuration during the off-state. Ferroelectric materials can induce different interfacial doping on adjacent layers depending on their polarization states. The stable polarization in ferroelectric material enables applications such as ferroelectric memory and ferroelectric tunneling junction, as well as reconfigurable logic and memory devices.[18−22] In the ferroelectric/semiconductor stack, the ferroelectric doping exerted on the semiconductor can alter the semiconductor's Fermi level in the selected area, and create

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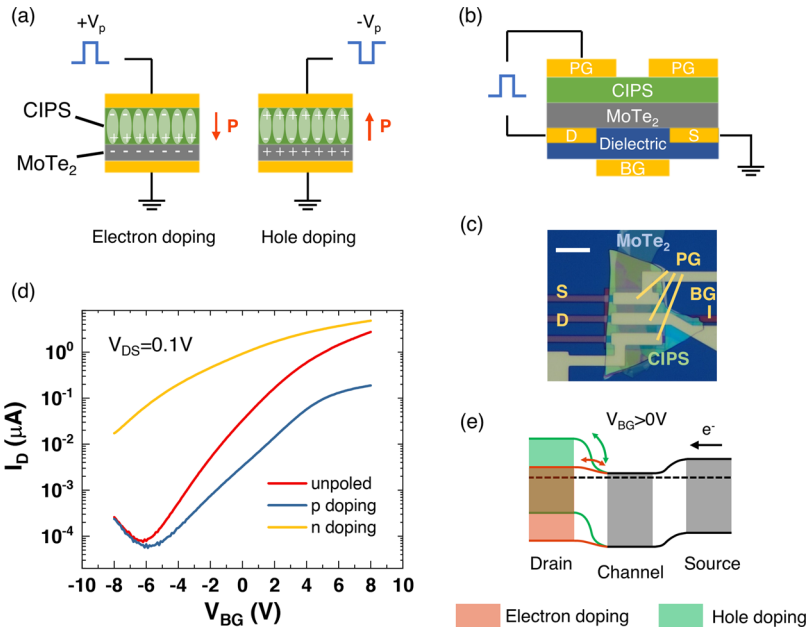


**Figure 1.** Reconfigurable contact based on the CIPS/$MoTe_2$ heterostructure. (a) Schematics of ferroelectric-induced doping in CIPS/$MoTe_2$ heterostructures. (b) Schematic of a $MoTe_2$ transistor with reconfigurable contact as the drain. The dielectric used here is 30 nm $SiN_x$. (c) An optical image of the $MoTe_2$ transistor. The scale bar is 10 $\mu$m. (d) The transfer curves of the transistor under different doping conditions on the drain contact. (e) Band diagrams of $MoTe_2$ at equilibrium with channel electron-doped. The dashed line represents the Fermi level in the $MoTe_2$. Red and green fill colors are used to represent electron doping and hole doping, respectively.

artificial junctions,[22−25] which constitutes a novel scheme for nonvolatile reconfigurable transistors.

Compared with Si nanowires, 2D materials with an atomically thin body provide better immunity to short-channel effects and allow more effective electrostatic or proximity doping.[26−29] In addition, small bandgap 2D semiconductors show both electron and hole conduction depending on the height of the Schottky barrier at the contacts.[30−33] In the context of reconfigurable devices, 2D materials are advantageous in that a steep junction profile can be achieved with atomic thickness. Nonvolatile reconfigurable transistors have been demonstrated based on organic ferroelectric P(VDF-TrFE) and solid-state ionic conductor in $MoS_2$ and $WSe_2$ transistors.[23,34,35] However, the programming of these devices uses scanning probes and high temperatures, which are not scalable for large device arrays and incompatible with electrical reconfiguration. The 2D ferroelectric $CuInP_2S_6$ (CIPS) shows high scalability with stable ferroelectricity in few layers.[36] Moreover, with the convenient integration technique of transfer stacking, it can be easily integrated with the electrically reconfigurable circuits.[37−41]

In this paper, we demonstrate nonvolatile reconfigurable heterostructures with 2D ferroelectric $CuInP_2S_6$ and semiconductor $MoTe_2$. The ferroelectric dipoles in CIPS introduce electron and hole doping in $MoTe_2$, which can be maintained without an external power supply. Reconfigurable transistors are realized by adding ferroelectric CIPS and local program gates in the source/drain regions. Symmetric electron and hole doping in the source/drain contacts can result in n-type and p-type transistors, respectively. In addition, transistors with asymmetric doping in the source and drain regions behave like p−n junctions. Various photoresponses are observed in different doping combinations, which leads to applications such as reconfigurable photodetectors.

## FERROELECTRIC-INDUCED DOPING IN THE CIPS/$MOTE_2$ HETEROSTRUCTURE

The structure of the CIPS/$MoTe_2$ heterostructure is shown in Figure 1a. The CIPS/$MoTe_2$ stack is sandwiched between two metal electrodes. The top electrode on CIPS is referred to as the program gate, and the bottom electrode below $MoTe_2$ is connected to ground. When a voltage pulse with amplitude $V_p$ is applied on the program gate, the polarization in CIPS is aligned with the direction of the external electric field. This dipole alignment in CIPS and the resulting polarization direction are indicated in Figure 1a. After a pulse with positive voltage ($+V_p$) is applied, the positive polarization charges at the bottom surface of CIPS will attract electrons in the adjacent $MoTe_2$ layer. This charge configuration is referred to as the electron or n-doping state. Similarly, a pulse with negative voltage ($-V_p$) will switch the polarization direction and induce hole or p-doping in $MoTe_2$. The different doping states of $MoTe_2$ are used as reconfigurable contacts in a transistor geometry. Figure 1b shows the schematic of a transistor where the aforementioned heterostructure replaces the drain and source contacts. During the programming operation, the program pulse voltage is applied between the program gate and the drain contact. The source and drain contacts are between the channel flake and the back gate, which can screen the electric field from the back gate to the $MoTe_2$ on top of the source and drain. Therefore, the doping in the contact region is not affected by the electrostatic doping from the back gate. Note that the program gate of the reconfigurable contact is extended further into the channel as compared to the source/drain contact for better electrostatic control. Figure 1c shows the optical image of a typical device. The program gates are labeled as "PG". Six devices were fabricated. The thicknesses of $MoTe_2$ flakes used in these devices are 5.1−13.2 nm, and the thicknesses of CIPS flakes are 138−189 nm. The atomic force microscopy (AFM)


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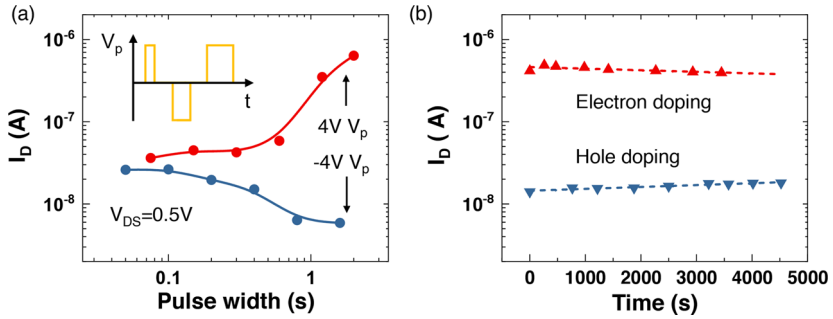


**Figure 2.** Switching time and retention of the reconfigurable contact. (a) Drain current at zero gate voltage with respect to the writing pulse width. The current is used as the indicator of polarization strength. The inset illustrates the measurement scheme of programming pulses. $V_{DS}$ = 0.5 V. (b) The retention behavior of the reconfigurable contact after programming into specific states. The dashed lines represent the linear fitting of the data.

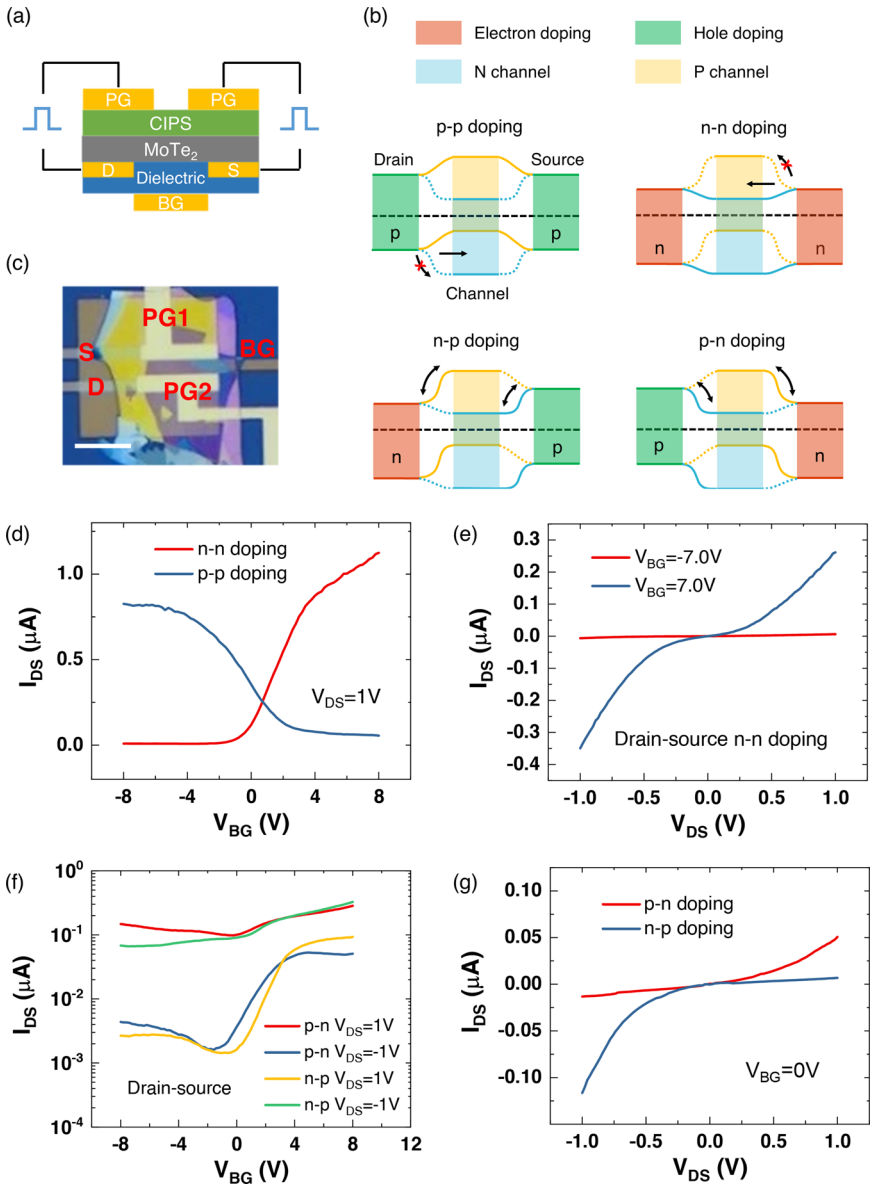


**Figure 3.** Characterization of reconfigurable transistors based on CIPS/$MoTe_2$ heterostructures. (a) The schematic of the reconfigurable transistor. Each contact can be programmed individually. (b) Optical image of the transistor under test. (c) The equilibrium band diagrams of the $MoTe_2$ layer under different combinations of drain-source polarization states. (d) Transfer curves of the transistor under n−n and p−p doping states. The transistor operates as nFET and pFET, respectively. Here, $V_{DS}$ = 1 V. Inset: an optical image of the transistor under test. The scale bar is 10 $\mu$m. (e) Output curves of a transistor in n−n doping state. (f) The transfer curves of the transistor with asymmetric contacts. The conductance depends on the current direction. (g) Output curves of the transistor with asymmetric contacts show rectifying behavior. Here, $V_{BG}$ = 0 V.



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mapping of a typical device is shown in Figure S1. We first investigate the transfer characteristics under different doping states in the drain contact. As shown in Figure 1d, a transistor with 8.5 nm $MoTe_2$ and 145 nm CIPS shows n-type behavior before applying any program pulse (i.e., CIPS is unpoled). Thin $MoTe_2$ generally shows p-type behavior and turns to n-type as the thickness increases.[42,43] Moreover, the ambient atmosphere also introduces p-doping in $MoTe_2$ transistors.[44] To investigate the intrinsic doping in our flakes, $MoTe_2$ transistors encapsulated with BN are built and n-type behavior was observed (Figure S2). We note that CIPS also serves as encapsulation and protects the $MoTe_2$ flake from ambient doping. For an n-type transistor, the electrons flow from the source to the drain when a positive bias is applied on the drain. By controlling the doping of $MoTe_2$ at the drain contact, the flow of electrons can be facilitated or suppressed depending on the doping level. This reconfiguration scheme is adopted in several early reports.[15,45]

The transfer curves measured after the program pulses are shown in Figure 1d. The voltage pulses used are −4 and 3 V for 10 s each. When the reconfigurable contacts are programmed as n-doped, the transfer curve shows strong unipolar conduction with a higher electron current. On the contrary, when the contacts are p-doped, the electron current is smaller than that in the unpoled state. The equilibrium band diagram of $MoTe_2$ is shown in Figure 1e. The left and right sides represent the $MoTe_2$ on top of the source and drain, respectively, whereas the channel is in the middle. When the back-gate voltage $V_{BG} > 0$ V, a large density of electrons is induced in the channel. The n-type doping at the drain side will facilitate the electron conduction by reducing the energy barrier for electrons between the channel and the drain. Conversely, the p-type doping will decrease the electron current by creating a barrier for electron conduction. Besides this reconfiguration scheme, transistors with only source-side switching also show large contrast in electron current between the two doping states (Figure S3), where the electron density in the source reservoir is modulated by the ferroelectric polarization. The equilibrium band diagram of $MoTe_2$ under hole doping ($V_{BG} < -6$ V) is shown in Figure S4. The hole current is limited by the barrier between the channel and the source in both configurations. Therefore, the hole currents are similar for the p-type doping state and the unpoled state. As for the n-type doping state, the hole current is masked by the electron conduction, therefore, only the electron branch is observed.

For the unipolar device, the current measured at $V_{BG} = 0$ V is an indicator of the strength of the polarization-induced doping. Figure 2a shows the polarization strength of the reconfigurable contact with various programming pulse widths. Programming voltages of −4 V and +4 V are used for the measurements. Pulses with variable widths are applied alternatively as shown in the inset. The drain current at drain voltage $V_{DS} = 0.5$ V is measured after each programming pulse. We note that a pulse shorter than 100 ms barely polarizes the reconfigurable contact, whereas a pulse width of 2.4 s can introduce sufficient doping approaching the saturation level, as shown in Figure 2a. The saturation polarization of metal/CIPS/metal capacitor is 4.8 $\mu C/cm^2$, which corresponds to a sheet density of $3 \times 10^{13}$ $cm^{-2}$. The switching time is $10^{-2}$ s at an electric field of 25 kV/cm.[41] The measured switching time here is longer due to the insertion of semiconductor layer, which takes a portion of the applied voltage. In addition, an increased depolarization field in the ferroelectric/semiconductor stack requires a higher pulse voltage or longer pulse width to switch the polarization to saturation level. Figure 2b shows the retention behavior of the reconfigurable contact after being programmed with ±4 V pulses with 10 s pulse width. Compared with the metal/ferroelectric/metal structure, the insertion of the semiconducting layer typically degrades the retention performance. The metal/CIPS/metal capacitor is reported to retain polarization for 1 year.[46] With a semiconducting $MoTe_2$ layer, we observe that the polarization strength slowly decreases over time in log scale. Nonetheless, the device still maintains a sizable current ratio after 1 h.

## NONVOLATILE RECONFIGURABLE TRANSISTORS

To switch the polarity of the transistor between n-type and p-type, two reconfigurable contacts are needed in this transistor. Figure 3a shows the schematic of the reconfigurable transistor where the doping in both the source and the drain are programmed individually. Figure 3c shows an optical image of the reconfigurable transistor. The dielectric here is 20 nm-thick $AlO_x$. The estimated channel width and length are 13.5 and 2.5 $\mu$m, respectively. Depending on the polarization states of the source and drain, four combinations can be achieved. The band diagrams under equilibrium for these doping combinations are shown in Figure 3b. When the drain-source contacts are programmed symmetrically, that is, p−p or n−n doping, shown in the upper half of Figure 3b, both contacts act as reservoirs of carriers of the same polarity (i.e., either holes or electrons), which suppresses the injection of carriers of the opposite polarity. When the doping in the channel is opposite to that of the contacts, the transistor is off. When the channel shares the same type of doping as the contacts, the transistor is on. This is depicted by Figure 3d, where the transfer curves of a reconfigurable transistor programmed in symmetric states are shown. The transistor operates as n-type transistor under n−n doping and p-type transistor under p−p doping in the contacts, showing unipolar behavior for both cases. The output characteristics of the transistor in the n−n doping state are shown in Figure 3e. When $V_{BG} = 7$ V, the channel is completely turned on. The nonlinear output curve implies Schottky injection of electrons. When the channel is brought into p-type conduction at $V_{BG} = -7$ V, the electron current is diminished to a very low level on account of the low electron density in the channel. The hole current is also limited due to the low hole density in the contacts. Therefore, unipolar operations are expected in the reconfigurable transistor.

The two reconfigurable contacts can be programmed differently to achieve p−n doping and n−p doping as shown in the lower half of Figure 3b. Here, when the channel is n-doped, the current is mainly controlled by the p−n junction between the channel and the p-type contact. Similarly, when the channel is p-doped, the current is determined by the $V_{DS}$ junction between the channel and the n-type contact. The p−n offsets are labeled on the band diagram, where the offset for hole-doped channel is smaller than that for the electron-doped channel. Figure 3f shows the transfer curves measured with an asymmetrically programmed transistor. The four curves can be categorized into two groups since the transfer curves of a p−n junction measured with a negative $V_{DS}$ matches that of an n−p junction measured with a positive $V_{DS}$. High conductance is observed for current flowing from the p-doping contact to the n-doping contact. This current is insensitive to gate sweep


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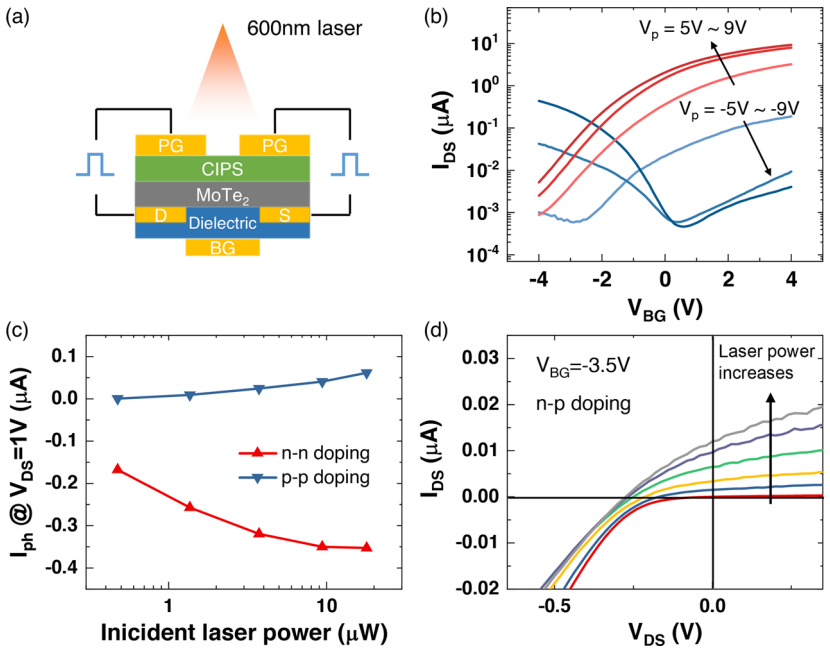


**Figure 4.** Photoresponse of reconfigurable transistors. (a) Schematic of the device under 600 nm laser illumination. (b) Transfer curves of the transistor under test measured after various program pulses. (c) Power-dependent photocurrent of transistor measured at $V_{BG}$ = 0 V with p−p and n−n configuration. The laser power range is in the range of 0.47−18 $\mu$W. (d) Output curves of the transistor with n−p configuration measured with the same laser power range. Here, $V_{BG}$ = −3.5 V.

because the p−n junction is under forward bias. A lower conductance is observed for current along the n−p direction since the p−n junction is reverse biased. The transfer curve of the n−p direction also shows increased current in the n-channel. This is due to a weak p-doping state in these reconfigurable contacts where the hole concentration is relatively small. Consider an n-channel transistor with asymmetric contacts, the current is determined by the p−n junction of the weakly p-doped contact and the n-type channel. The output curves in Figure 3g have rectifying behavior in both n−p and p−n doping conditions due to the asymmetrically programmed contacts.

## PHOTORESPONSE OF RECONFIGURABLE TRANSISTORS

The photoresponse of the reconfigurable transistor also depends on the doping states. Figure 4a shows the schematic of a reconfigurable transistor under laser illumination. A 600 nm laser with tunable power is used for the photocurrent measurements. Note that the bandgap of CIPS is 2.9 eV,[47,48] which is larger than the photon energy and will not affect the light absorption in $MoTe_2$. $SiN_x$ of 20 nm thickness is used as the bottom gate dielectric. The transfer curves of the transistor under symmetric programming are shown in Figure 4b with various pulse amplitudes. The pulse width is 4 s. The CIPS flake in this device is 189 nm thick. A positive program voltage increases the electron current component (nFET state), whereas a negative program voltage increases the hole current component in the drain current (pFET state). As the $MoTe_2$ channel is naturally n-doped, the electron current in the nFET state is stronger than the hole current in the pFET state under the same amplitude of programming voltage. When the contact is programmed symmetrically at ±9 V, the output characteristics measured at $V_{BG}$ = 0 V under laser power series 0.47−18 $\mu$W for n−n doping and p−p doping states are shown in Figure S8a,b. The drain current is zero when the drain voltage is zero (i.e., no photovoltaic effect is observed), which confirms the symmetric doping condition at source/drain contacts. Figure 4c shows the extracted photocurrent at $V_{DS}$ = 1 V for these two states. A negative photocurrent is observed in the n−n doping configuration and gradually saturates at higher incident laser power. The negative photocurrent is presumably due to the photogating effect, where the photogenerated electrons are captured by traps, which reduces the electron density in the channel. For the p−p doping configuration, the transistor is near the minimum conduction point at zero gate voltage, that is, the hole concentration is low. The photocurrent increases as the incident laser power increases. The transistor behaves as a photoconductor and more photogenerated holes lead to an increase in the photocurrent. When the transistor is configured with asymmetric contacts, the photovoltaic effect is observed due to the built-in potential of the p−n junction. Figure 4d shows the output curves of an n−p doped transistor measured under the same laser power series. $V_{BG}$ = −3.5 V is applied to compensate for the channel doping. The dark current crosses the zero point and shows a strong rectifying behavior. As the power increases, the output curve shifts upward. Sizable open-circuit voltage, $V_{oc}$, and short circuit current, $I_{sc}$, are observed, which confirms the built-in potential in the asymmetric contacts. The maximum $V_{oc}$ is ~275 mV, which gives an estimation of the band offset between n-doping and p-doping states of reconfigurable contacts.

## CONCLUSION

In conclusion, we observed nonvolatile doping in $MoTe_2$ induced by the ferroelectric polarization in CIPS. By using this doping technique in the source/drain contacts, a transistor with reconfigurable polarity (n-type or p-type) is demonstrated. The n−n and p−p doping in the source-drain regions


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result in unipolar nFET and pFET, respectively. The transistor under asymmetric doping (n−p or p−n) configuration shows rectifying behavior where a high drain current occurs when the p−n junction is forward biased. The configuration of the transistor based on CIPS/$MoTe_2$ heterostructure is non-volatile, where the polarization in CIPS is nearly unchanged during the 1 h retention test. Distinct photoresponses are observed for the reconfigurable transistor under different configurations. A negative photocurrent is found at an n−n doping state due to the photogating effect. Transistors with p−p doping state show a positive photocurrent due to the photoconductive effect. For asymmetric doping states (n−p or p−n), photovoltaic effect is observed with a maximum open-circuit voltage of 275 mV, which corresponds to the built-in potential between the n- and p-doped regions.

## ■ ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c03557.

Materials and methods, Figures S1−S9, and discussion on programming current in CIPS/$MoTe_2$ heterostructures (PDF)

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### Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

### Notes

The authors declare no competing financial interest.

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## ■ REFERENCES


(1) Gaillardon, P. E.; Tang, X. F.; Kim, G.; De Micheli, G. A Novel FPGA Architecture Based on Ultrafine Grain Reconfigurable Logic Cells. *Ieee T Vlsi Syst* **2015**, *23* (10), 2187−2197.

(2) Pan, C.; Wang, C. Y.; Liang, S. J.; Wang, Y.; Cao, T. J.; Wang, P. F.; Wang, C.; Wang, S.; Cheng, B.; Gao, A. Y.; Liu, E. F.; Watanabe, K.; Taniguchi, T.; Miao, F. Reconfigurable logic and neuromorphic circuits based on electrically tunable two-dimensional homojunctions. *Nat. Electron* **2020**, *3* (7), 383−390.

(3) Raitza, M.; Kumar, A.; Volp, M.; Walter, D.; Trommer, J.; Mikolajick, T.; Weber, W. M. Exploiting Transistor-Level Reconfiguration to Optimize Combinational Circuits. *Proceedings of the 2017 Design, Automation & Test in Europe Conference & Exhibition (Date)* **2017**, 338−343.

(4) Trommer, J.; Heinzig, A.; Baldauf, T.; Slesazeck, S.; Mikolajick, T.; Weber, W. M. Functionality-Enhanced Logic Gate Design Enabled by Symmetrical Reconfigurable Silicon Nanowire Transistors. *IEEE Trans. Nanotechnol.* **2015**, *14* (4), 689−698.

(5) Liu, C. S.; Yan, X.; Song, X. F.; Ding, S. J.; Zhang, D. W.; Zhou, P. A semi-floating gate memory based on van der Waals heterostructures for quasi-non-volatile applications. *Nat. Nanotechnol.* **2018**, *13* (5), 404−410.

(6) Migliato Marega, G.; Zhao, Y.; Avsar, A.; Wang, Z.; Tripathi, M.; Radenovic, A.; Kis, A. Logic-in-memory based on an atomically thin semiconductor. *Nature* **2020**, *587* (7832), 72−77.

(7) Liu, L.; Hou, X.; Zhang, H.; Wang, J. L.; Zhou, P. Ferroelectric field-effect transistors for logic and in-situ memory applications. *Nanotechnology* **2020**, *31* (42), 424007.

(8) Bi, Y.; Hu, X. S.; Jin, Y.; Niemier, M.; Shamsi, K.; Yin, X. Z. Enhancing Hardware Security with Emerging Transistor Technologies. *2016 International Great Lakes Symposium on Vlsi (Glsvlsi)* **2016**, 305−310.

(9) Erbagci, B.; Erbagci, C.; Akkaya, N. E. C.; Mai, K. A Secure Camouflaged Threshold Voltage Defined Logic Family. *Proceedings of the 2016 Ieee International Symposium on Hardware Oriented Security and Trust (Host)* **2016**, 229−235.

(10) Dutta, S.; Grisafe, B.; Frentzel, C.; Enciso, Z.; San Jose, M.; Smith, J.; Ni, K.; Joshi, S.; Datta, S. Experimental Demonstration of Gate-Level Logic Camouflaging and Run-Time Reconfigurability Using Ferroelectric FET for Hardware Security. *IEEE Trans. Electron Devices* **2021**, *68* (2), 516−522.

(11) Wu, P.; Reis, D.; Hu, X. B. S.; Appenzeller, J. Two-dimensional transistors with reconfigurable polarities for secure circuits. *Nat. Electron* **2021**, *4* (1), 45−53.

(12) Resta, G. V.; Balaji, Y.; Lin, D.; Radu, I. P.; Catthoor, F.; Gaillardon, P. E.; De Micheli, G. Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors. *ACS Nano* **2018**, *12* (7), 7039−7047.

(13) Larentis, S.; Fallahazad, B.; Movva, H. C. P.; Kim, K.; Rai, A.; Taniguchi, T.; Watanabe, K.; Banerjee, S. K.; Tutuc, E. Reconfigurable Complementary Monolayer MoTe2 Field-Effect Transistors for Integrated Circuits. *ACS Nano* **2017**, *11* (5), 4832−4839.

(14) Nakaharai, S.; Yamamoto, M.; Ueno, K.; Lin, Y. F.; Li, S. L.; Tsukagoshi, K. Electrostatically Reversible Polarity of Ambipolar alpha-MoTe2 Transistors. *ACS Nano* **2015**, *9* (6), 5976−5983.

(15) Heinzig, A.; Slesazeck, S.; Kreupl, F.; Mikolajick, T.; Weber, W. M. Reconfigurable silicon nanowire transistors. *Nano Lett.* **2012**, *12* (1), 119−124.

(16) Glassner, S.; Zeiner, C.; Periwal, P.; Baron, T.; Bertagnolli, E.; Lugstein, A. Multimode Silicon Nanowire Transistors. *Nano Lett.* **2014**, *14* (11), 6699−6703.

(17) Simon, M.; Liang, B.; Fischer, D.; Knaut, M.; Tahn, A.; Mikolajick, T.; Weber, W. M. Top-Down Fabricated Reconfigurable FET With Two Symmetric and High-Current On-States. *IEEE Electron Device Lett.* **2020**, *41* (7), 1110−1113.

(18) Yap, W. C.; Jiang, H.; Liu, J. L.; Xia, Q. F.; Zhu, W. J. Ferroelectric transistors with monolayer molybdenum disulfide and ultra-thin aluminum-doped hafnium oxide. *Appl. Phys. Lett.* **2017**, *111* (1), 013103.

(19) Chen, L.; Wang, T. Y.; Dai, Y. W.; Cha, M. Y.; Zhu, H.; Sun, Q. Q.; Ding, S. J.; Zhou, P.; Chua, L.; Zhang, D. W. Ultra-low power Hf0.5Zr0.5O2 based ferroelectric tunnel junction synapses for

hardware neural network applications. *Nanoscale* **2018**, *10* (33), 15826−15833.
(20) Shekhawat, A.; Walters, G.; Yang, N.; Guo, J.; Nishida, T.; Moghaddam, S. Data retention and low voltage operation of Al2O3/Hf(0.5)Zr(0.5)O(2)based ferroelectric tunnel junctions. *Nanotechnology* **2020**, *31* (39), 39LT01.
(21) Zhao, R.; Zhao, X.; Liu, H.; Shao, M.; Feng, Q.; Liu, T.; Lu, T.; Wu, X.; Yi, Y.; Ren, T. L. Reconfigurable logic-memory hybrid device based on ferroelectric Hf0.5Zr0.5O2. *IEEE Electron Device Lett.* **2021**, *42* (8), 1164−1167.
(22) Luo, Z. D.; Yang, M. M.; Liu, Y.; Alexe, M. Emerging Opportunities for 2D Semiconductor/Ferroelectric Transistor-Structure Devices. *Adv. Mater.* **2021**, *33* (12), 2005620.
(23) Lv, L.; Zhuge, F. W.; Xie, F. J.; Xiong, X. J.; Zhang, Q. F.; Zhang, N.; Huang, Y.; Zhai, T. Y. Reconfigurable two-dimensional optoelectronic devices enabled by local ferroelectric polarization. *Nat. Commun.* **2019**, *10*, 3331.
(24) Li, D. W.; Xiao, Z. Y.; Mu, S.; Wang, F.; Liu, Y.; Song, J. F.; Huang, X.; Jiang, L. J.; Xiao, J.; Liu, L.; Ducharme, S.; Cui, B.; Hong, X.; Jiang, L.; Silvain, J. F.; Lu, Y. F. A Facile Space-Confined Solid-Phase Sulfurization Strategy for Growth of High-Quality Ultrathin Molybdenum Disulfide Single Crystals. *Nano Lett.* **2018**, *18* (3), 2021−2032.
(25) Xiao, Z. Y.; Song, J. F.; Ferry, D. K.; Ducharme, S.; Hong, X. Ferroelectric-Domain−patterning-Controlled Schottky Junction State in Monolayer MoS2. *Phys. Rev. Lett.* **2017**, *118* (23), 236801.
(26) Liu, H.; Neal, A. T.; Ye, P. D. Channel Length Scaling of MoS2MOSFETs. *ACS Nano* **2012**, *6* (10), 8563−8569.
(27) Desai, S. B.; Madhvapathy, S. R.; Sachid, A. B.; Llinas, J. P.; Wang, Q. X.; Ahn, G. H.; Pitner, G.; Kim, M. J.; Bokor, J.; Hu, C. M.; Wong, H. S. P.; Javey, A. MoS2 transistors with 1-nanometer gate lengths. *Science* **2016**, *354* (6308), 99−102.
(28) Chhowalla, M.; Jena, D.; Zhang, H. Two-dimensional semiconductors for transistors. *Nat. Rev. Mater.* **2016**, *1* (11), 16052.
(29) Cao, W.; Kang, J. H.; Sarkar, D.; Liu, W.; Banerjee, K. 2D Semiconductor FETs-Projections and Design for Sub-10 nm VLSI. *IEEE Trans. Electron Devices* **2015**, *62* (11), 3459−3469.
(30) Hu, W. N.; Sheng, Z.; Hou, X.; Chen, H. W.; Zhang, Z. X.; Zhang, D. W.; Zhou, P. Ambipolar 2D Semiconductors and Emerging Device Applications. *Small Methods* **2021**, *5* (1), 2000837.
(31) Yarmoghaddam, E.; Haratipour, N.; Koester, S. J.; Rakheja, S. A Physics-Based Compact Model for Ultrathin Black Phosphorus FETs-Part I: Effect of Contacts, Temperature, Ambipolarity, and Traps. *IEEE Trans. Electron Devices* **2020**, *67* (1), 389−396.
(32) Yarmoghaddam, E.; Haratipour, N.; Koester, S. J.; Rakheja, S. A Physics-Based Compact Model for Ultrathin Black Phosphorus FETs-Part II: Model Validation Against Numerical and Experimental Data. *IEEE Trans. Electron Devices* **2020**, *67* (1), 397−405.
(33) Lanza, M.; Wong, H. S. P.; Pop, E.; Ielmini, D.; Strukov, D.; Regan, B. C.; Larcher, L.; Villena, M. A.; Yang, J. J.; Goux, L.; Belmonte, A.; Yang, Y. C.; Puglisi, F. M.; Kang, J. F.; Magyari-Kope, B.; Yalon, E.; Kenyon, A.; Buckwell, M.; Mehonic, A.; Shluger, A.; Li, H. T.; Hou, T. H.; Hudec, B.; Akinwande, D.; Ge, R. J.; Ambrogio, S.; Roldan, J. B.; Miranda, E.; Sune, J.; Pey, K. L.; Wu, X.; Raghavan, N.; Wu, E.; Lu, W. D.; Navarro, G.; Zhang, W. D.; Wu, H. Q.; Li, R. W.; Holleitner, A.; Wurstbauer, U.; Lemme, M. C.; Liu, M.; Long, S. B.; Liu, Q.; Lv, H. B.; Padovani, A.; Pavan, P.; Valov, I.; Jing, X.; Han, T. T.; Zhu, K. C.; Chen, S. C.; Hui, F.; Shi, Y. Y. Recommended Methods to Study Resistive Switching Devices. *Adv. Electron Mater.* **2019**, *5* (1), 1800143.
(34) Lee, S. J.; Lin, Z. Y.; Huang, J.; Choi, C. S.; Chen, P.; Liu, Y.; Guo, J.; Jia, C. C.; Wang, Y. L.; Wang, L. Y.; Liao, Q. L.; Shakir, I.; Duan, X. D.; Dunn, B.; Zhang, Y.; Huang, Y.; Duan, X. F. Programmable devices based on reversible solid-state doping of two-dimensional semiconductors with superionic silver iodide. *Nat. Electron* **2020**, *3* (10), 630−637.
(35) Wu, G. J.; Tian, B. B.; Liu, L.; Lv, W.; Wu, S.; Wang, X. D.; Chen, Y.; Li, J. Y.; Wang, Z.; Wu, S. Q.; Shen, H.; Lin, T.; Zhou, P.; Liu, Q.; Duan, C. G.; Zhang, S. T.; Meng, X. J.; Wu, S. W.; Hu, W. D.; Wang, X. R.; Chu, J. H.; Wang, J. L. Programmable transition metal dichalcogenide homojunctions controlled by nonvolatile ferroelectric domains. *Nat. Electron* **2020**, *3* (1), 43−50.
(36) Zhou, S.; You, L.; Zhou, H. L.; Pu, Y.; Gui, Z. G.; Wang, J. L. Van der Waals layered ferroelectric CuInP2S6: Physical properties and device applications. *Front Phys-Beijing* **2021**, *16* (1), 13301.
(37) Wu, J. B.; Chen, H. Y.; Yang, N.; Cao, J.; Yan, X. D.; Liu, F. X.; Sun, Q. B.; Ling, X.; Guo, J.; Wang, H. High tunnelling electroresistance in a ferroelectric van der Waals heterojunction via giant barrier height modulation. *Nat. Electron* **2020**, *3* (8), 466−472.
(38) Huang, W. H.; Wang, F.; Yin, L.; Cheng, R. Q.; Wang, Z. X.; Sendeku, M. G.; Wang, J. J.; Li, N. N.; Yao, Y. Y.; He, J. Gate-Coupling-Enabled Robust Hysteresis for Nonvolatile Memory and Programmable Rectifier in Van der Waals Ferroelectric Heterojunctions. *Adv. Mater.* **2020**, *32*, 1908040.
(39) Si, M.; Liao, P. Y.; Qiu, G.; Duan, Y.; Ye, P. D. Ferroelectric Field-Effect Transistors Based on MoS2 and CuInP2S6 Two-Dimensional van der Waals Heterostructure. *ACS Nano* **2018**, *12* (7), 6700−6705.
(40) Wang, X. W.; Yu, P.; Lei, Z. D.; Zhu, C.; Cao, X.; Liu, F. C.; You, L.; Zeng, Q. S.; Deng, Y.; Zhu, C.; Zhou, J. D.; Fu, Q. D.; Wang, J. L.; Huang, Y. Z.; Liu, Z. Van der Waals negative capacitance transistors. *Nat. Commun.* **2019**, *10*, 3037.
(41) Zhao, Z. J.; Xu, K.; Ryu, H.; Zhu, W. J. Strong Temperature Effect on the Ferroelectric Properties of CuInP2S6 and Its Heterostructures. *ACS Appl. Mater. Interfaces* **2020**, *12* (46), 51820−51826.
(42) Fathipour, S.; Ma, N.; Hwang, W. S.; Protasenko, V.; Vishwanath, S.; Xing, H. G.; Xu, H.; Jena, D.; Appenzeller, J.; Seabaugh, A. Exfoliated multilayer MoTe2 field-effect transistors. *Appl. Phys. Lett.* **2014**, *105* (19), 192101.
(43) Zhu, Y. Q.; Zhang, F.; Appenzeller, J. Thickness Tunable Transport Properties in MoTe2 Field Effect Transistors. *Ieee Device Res. Conf* **2018**, 1−2.
(44) Sirota, B.; Glavin, N.; Krylyuk, S.; Davydov, A. V.; Voevodin, A. A. Hexagonal MoTe2 with Amorphous BN Passivation Layer for Improved Oxidation Resistance and Endurance of 2D Field Effect Transistors. *Sci. Rep.* **2018**, *8*, 8668.
(45) Trommer, J.; Heinzig, A.; Muhle, U.; Loffler, M.; Winzer, A.; Jordan, P. M.; Beister, J.; Baldauf, T.; Geidel, M.; Adolphi, B.; Zschech, E.; Mikolajick, T.; Weber, W. M. Enabling Energy Efficiency and Polarity Control in Germanium Nanowire Transistors by Individually Gated Nanojunctions. *ACS Nano* **2017**, *11* (2), 1704−1711.
(46) Zhou, S.; You, L.; Chaturvedi, A.; Morris, S. A.; Herrin, J. S.; Zhang, N.; Abdelsamie, A.; Hu, Y. Z.; Chen, J. Q.; Zhou, Y.; Dong, S. A.; Wang, J. L. Anomalous polarization switching and permanent retention in a ferroelectric ionic conductor. *Mater. Horiz.* **2020**, *7* (1), 263−274.
(47) Liu, F.; You, L.; Seyler, K. L.; Li, X.; Yu, P.; Lin, J.; Wang, X.; Zhou, J.; Wang, H.; He, H.; Pantelides, S. T.; Zhou, W.; Sharma, P.; Xu, X.; Ajayan, P. M.; Wang, J.; Liu, Z. Room-temperature ferroelectricity in CuInP2S6 ultrathin flakes. *Nat. Commun.* **2016**, *7*, 12357.
(48) Ryu, H.; Xu, K.; Li, D.; Hong, X.; Zhu, W. Empowering 2D nanoelectronics via ferroelectricity. *Appl. Phys. Lett.* **2020**, *117* (8), 080503.


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