Electrical Characterization and Benchmarking of Polylithic Integration Using Fused-Silica Stitch-Chips with Compressible Microinterconnects for RF/mm-Wave Applications

Ting Zheng, *Student Member, IEEE,* Paul K. Jo, *Student Member, IEEE,*
Sreejith Kochupurackal Rajan, *Student Member, IEEE,* and Muhannad S. Bakir, *Senior Member, IEEE*

***Abstract*—A polylithic integration technology is demonstrated for seamless stitching of chiplets of various functions, including RF, analog, and digital chiplets. In this technology, stitch-chips with compressible microinterconnects (CMIs) are used for low-loss, low-parasitic, and dense interconnection between chiplets. The modeling, fabrication, assembly, and characterization of a set of testbeds using fused-silica stitch-chips with integrated CMIs are demonstrated in this paper. A 500 μm-long stitch-chip signal channel is measured to have less than 0.42 dB insertion loss up to 40 GHz with minimal parasitics (4.68 Ω at 28 GHz, 4.99 Ω at 39 GHz, 359 pH up to 40 GHz, and 62 fF up to 40 GHz). Moreover, CMIs' S-parameters are extracted by L-2L de-embedding technique up to 40 GHz. CMIs exhibit less than 0.2 dB insertion loss up to 40 GHz with better than 16.2 dB return loss. Furthermore, benchmarking to other interconnections is presented in terms of the loss and parasitics. Compared with conventional silicon-based interconnection, the data suggest that the fused-silica stitch-chip based interconnection reduces the insertion loss by approximately 3.8 dB at the 28 GHz and 39 GHz frequency bands. The stitch-chip interconnection has a similar insertion loss as glass interposer, organic substrate, and integrated fan-out (InFO) with the benefit of simple rework.**

***Index Terms*—De-embedding, flexible interconnects, RF measurements, RLCG parameters, transmission lines.**

I. Introduction

MONOLITHIC 3D integration is widely investigated for gigascale integrated (GSI) circuits to enable increasing functionality and performance. It has the potential to overcome device and circuit scaling challenges, such as incremental delays and power consumption [1]. However, for RF/mm-wave systems, monolithic 3D integration lacks material and device integration flexibility, which results in high cost, long time-to-market, modeling difficulties, and poor thermal management [2]. In contrast, polylithic integration of chiplets enables seamless heterogeneous integration of RF, analog, and digital chiplets sourced from different materials, processes, and foundries to yield optimized system functionality and electrical performance and achieve better thermal performance potentially [2], [3], [4], [5]. By partitioning system functionality into different components and integrating them, the system integration/performance challenges can be disintegrated into lower-level challenges that could be easier to overcome (e.g., inductors could be integrated on a low-loss substrate for higher quality factor to enhance system performance [3]).

Interconnect losses must be carefully optimized in polylithic integration due to interconnect length. This becomes more critical when RF/mm-wave systems utilize higher-frequency bandwidths, such as fifth-generation (5G) wireless systems (28 GHz and 39 GHz bands) [3]. For these RF/mm-wave systems, any polylithic integration technology should provide low-loss, impedance-matching, and low-parasitic signal interfaces between RF, analog, and digital chiplets with other components, such as antennas and passives [3], [4]. For example, antennas in package feed lines and interconnects between RF beamforming ICs and frequency conversion ICs should route mm-wave signals with insignificant loss to enhance the performance (e.g., the antenna efficiency) [6], [7]. In addition, impedance matching between analog or RF ICs and antenna elements is critical for sufficient power transferring [4], [7]. Small parasitics are also critical not only for signal integrity of digital ICs but also for RF/mm-wave components, such as baseband modules and antenna-integrated modules [4].

While wire bonding is mature and cost-effective to package ICs, the bond wire introduces significant loss and parasitics at high frequencies, impedance discontinuity, and density scaling challenges, which result in a significant degradation of system performance [8]. In this paper, a polylithic integration technology enabled by stitch-chips is proposed. Fig. 1 shows a side view of the envisioned technology for RF/mm-wave systems. Unlike bond wires, very short transmission lines (approaching less than 100 μm) are optimized on a low-loss dielectric substrate to form the stitch-chips for low-loss, low-parasitic, and impedance-matched signal transitions. The fabrication of the stitch-chips is based on mature lithography processes that could enable easy scaling to fulfill future fine-pitch interconnect requirements (e.g., antenna arrays operating beyond 100 GHz may demand much denser interconnect routing between

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T. Zheng, S. Kochupurackal Rajan, and M. S. Bakir are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332, USA (e-mail: ting.zheng@gatech.edu)

P. K. Jo was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332, USA. He is now with the Georgia Tech Research Institute, Atlanta, GA, 30318, USA

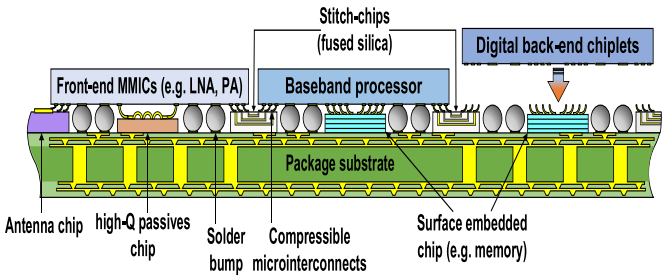


Fig. 1. Envisioned polylithic integration using stitch-chips for RF/mm-wave systems

elements (spacing around 1.5 mm or less) [7]). Furthermore, the stitch-chips' fabrication eliminates the process for through vias, which are necessary in other interposer-like technologies, such as RF-IC and antenna integration using high-resistivity Si interposer [9]. In addition, the stitch-chips can incorporate integrated passive devices (IPD) serving as matching network and filtering circuits.

Compressible microinterconnects (CMIs) [10], as pressure-based mechanically compliant off-chip I/Os, are used to interface chiplets with the stitch-chips. Such I/Os could enable die-level testing and rapid prototyping of system-in-package. Similar compliant off-chip I/Os are currently used in several commercial products. For example, FormFactor's Pyrana RF probe cards utilize compliant I/Os with 80 μm to 106 μm pitch for die-level testing up to 45 GHz [11]. Samtec's Z-RAY compression interposer with larger compliant I/Os serves as a removable interface between the package and board, which enables rapid prototyping for R&D applications [12].

The CMIs have similar dimensions as solder bumps used in flip-chip but could overcome several mechanical and electrical challenges: first, CMIs do not form intermetallic compound (IMC) whose ratio increases with bump-pitch scaling and causes mechanical reliability issues (e.g., cracking) [13]; second, shorting with adjacent interconnects during scaling is not a concern for CMIs. However, shorting is a challenge for fine-pitch solder bumps using thermo-compression bonding. In addition, CMI assembly can be performed at room temperature and does not require large forces, which facilitate the assembly. The stitching technology enabled by the CMIs can achieve the integration of various chiplets irrespective of their coefficient of thermal expansion (CTE) mismatch. CMIs can also enable simple rework, which is key to boost system yield as chiplets can be easily replaced and upgraded.

The RF/mm-wave characterization of stitch-chips and CMIs is necessary to demonstrate the performance of the proposed technology. To this end, the design of de-embedding testbeds and parasitics extraction are performed. For de-embedding, while the thru-reflect-line (TRL) technique is expected to have an error on the measured S-parameters due to the difficulty of determining the reference impedance [14], and the open-short de-embedding technique suffers from frequency band limitation [15], the L-2L technique [16], [17] has been applied widely for the RF/mm-wave characterization of interconnects. For parasitics extraction, distributed models and lumped models have been investigated for interconnects [18], [19]. However, the models are band-limited, which requires validation of their feasibility at the frequency band of interest.

In this paper, a set of testbeds for stitch-chips are modeled, fabricated, and assembled. Probing pads' de-embedding and L-2L de-embedding are studied for these testbeds. While preliminary results (up to 30 GHz) of stitch-chip channels and CMIs, including S-parameters and eye-diagrams, are reported in our previous work [20], this paper, for the first time, demonstrates the characterization of both stitch-chip channels and CMIs up to 40 GHz for emerging 5G systems (28 GHz- and 39 GHz-bands). Moreover, for the first time, parasitics extraction methods are investigated for both stitch-chip channels and CMIs, and their frequency-dependent parasitics are reported in this paper. To further demonstrate the performance of the stitch-chip channels, benchmarking to other signal channels is shown. The electrical performance of CMIs is also compared with other off-chip I/Os and reported in this paper.

The organization of this paper is as follows: Section II describes a testbed that emulates a fully assembled stitch-chip system. The L-2L de-embedding and parasitics extraction methods are also demonstrated. Section III summarizes the fabrication of CMIs and assembly process of the testbed. Sections IV and V report the characterization of stitch-chip channels and the de-embedding results of the CMIs, respectively. Benchmarking discussion is reported in Section VI. Finally, Section VII is the conclusion.

II. De-Embedding and Parasitics Modeling

Fig. 2a shows a testbed designed in ANSYS HFSS and reported in our previous work [20]. The design emulates a fully assembled stitch-chip system in the proposed polylithic

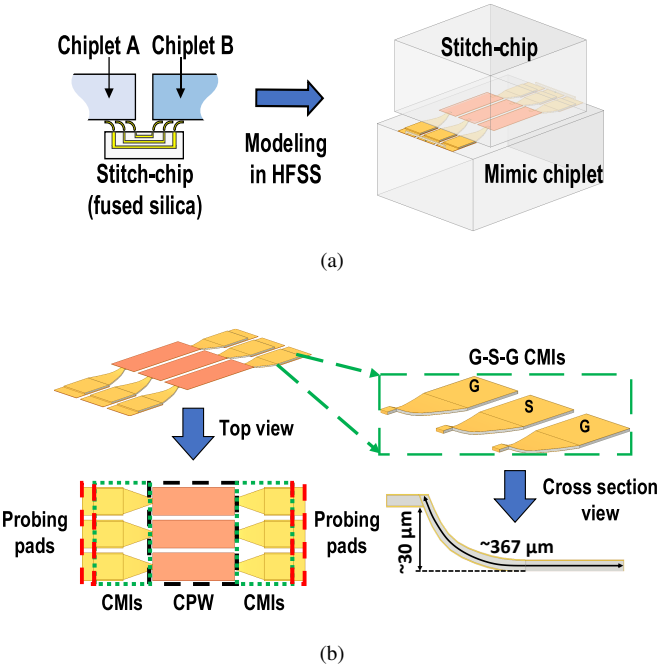


Fig. 2. Testbed HFSS modeling: (a) modeling procedure and (b) schematic of a device under test and G-S-G CMIs

integration technology. Fused-silica substrate is used for both the stitch-chip and the mimic chiplet due to its low-loss properties (low dielectric constant ∼3.9 and low loss tangent ∼0.0002).

Coplanar waveguides (CPWs) are designed on the stitch-chip: center signal conductor has 170 μm width and is 30 μm spaced from adjacent ground (reference) traces; all conductors are 1.5 μm thick copper capped with 0.5 μm thick gold. These dimensions result in CPWs with approximately 50 Ω characteristic impedance up to 40 GHz.

Two ground-signal-ground (G-S-G) sets of gold-coated NiW CMIs (NiW for higher yield strength to prevent plastic deformation) with probing pads are formed on the mimic chiplet. Note that these CMIs can also be formed on the stitch-chip. The CMIs are 30 μm in height and ∼367 μm in length, as shown in Fig. 2b. The size of the probing pads is 170 μm×250 μm. The CMIs are coated with electroless-plated gold to prevent oxidation [21]. Moreover, this electroless-plated gold layer is essential to reduce the loss because of its higher conductivity and larger skin depth at high frequencies. Fig. 2b shows a device under test (DUT) consisting of two probing pads, one CPW and two sets of CMIs. Curved sidewalls enable the out-of-plane mechanical flexibility of the CMIs [10].

A. L-2L De-Embedding Technique

As shown in Fig. 3a, the parasitics of the probing pads should be removed firstly by ABCD-matrix computation as follows:

$$[Thrupads] = [Pad][Pad] \tag{1}$$

$$[DUT] = [Pad][Chan][Pad] \tag{2}$$

$$[Chan] = \sqrt{[Thrupads]}^{-1}[DUT]\sqrt{[Thrupads]}^{-1} \tag{3}$$

where $[Pad]$ represents the probing pads' ABCD-matrix, and $[Chan]$ is the ABCD-matrix of the resulting structure (i.e. stitch-chip channel, CMIs+CPW+CMIs).

A proper L-2L de-embedding of the CMIs requires at least two testbeds, one with L-length CPW and the other with 2L-length CPW on stitch-chips. To meet this requirement, two testbeds are designed. One has 500 μm (L) long CPWs and the other has 1000 μm (2L) long CPWs. The ABCD-matrices of these testbeds after removing the probing pads' parasitics (i.e. stitch-chip channel) are denoted as $[Chan1]$ and $[Chan2]$ in Fig. 3b. As shown in Fig. 3b, $[CMI]$ and $[L]$ are the ABCD-matrices of the CMIs and the L-length CPW, respectively. Next, L-2L de-embedding [16], [17] is performed and described using ABCD-matrix form:

$$[Chan1] = [CMI][L][CMI] \tag{4}$$

$$[Chan2] = [CMI][L][L][CMI] \tag{5}$$

$$[CMI] = \left(\sqrt{[Chan1]^{-1}[Chan2][Chan1]^{-1}}\right)^{-1} \tag{6}$$

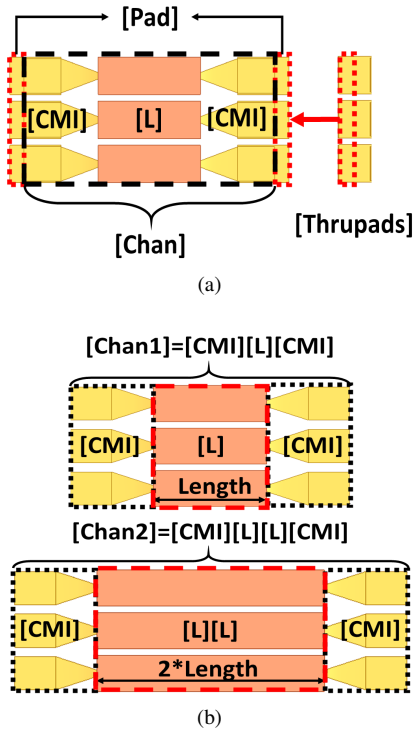


Fig. 3. L-2L de-embedding procedure: (a) pad parasitics removal and (b) L-2L de-embedding

B. Parasitics Extraction

Parasitics extraction models can be categorized into distributed models (using propagation constant γ and frequency-dependent characteristic impedance Z_0) and lumped models [19]. The condition to apply these different models relies on the wavelength, which could be calculated as follows:

$$\lambda = c/(\sqrt{\varepsilon_r} f) \tag{7}$$

where λ is the wavelength, c is the speed of electromagnetic wave in vacuum, ε_r is the relative permittivity of the medium, and f is frequency. If the physical length of a target structure is less than or comparable to λ/10, lumped models can be used. Otherwise, the distributed model should be used.

However, the medium in these testbeds consists of air and fused-silica, which results in an unknown effective permittivity. This complicates the wavelength calculation. One approach is to consider two cases: one assumes that the medium is only air, while the other assumes only fused-silica. The effective permittivity of the actual medium will be between the calculated values from the two cases and as will be the wavelength. Therefore, λ/10 is within the range of ∼380 μm to ∼750 μm at 40 GHz, which implies that the lumped models can be used for the parasitics extraction of the CMIs (typical length less than 380 μm) and the distributed model will be used for the CPWs. A combined parasitics model that includes both the CMIs' lumped model and the CPW's distributed model is proposed for the total stitch-chip channel (i.e. CMIs+CPW+CMIs).

The combined model for the total stitch-chip channel is shown in Fig. 4. The combined model consists of two CMIs'

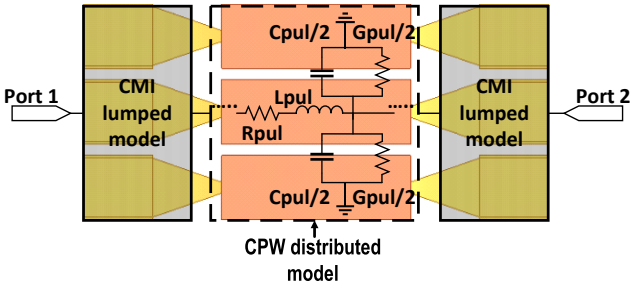


Fig. 4. Combined parasitics model for the total stitch-chip channel (distributed model for CPW and lumped model for CMIs)

lumped model blocks and one CPW's distributed model block. These three blocks are connected to represent the parasitics model of the total stitch-chip channel. For the CMIs' lumped model, a detailed discussion is provided later in this section. For the CPW's distributed model, one per-unit-length (pul) element, which is calculated from an ABCD-matrix of the CPW, is depicted in Fig. 4 and the CPW's distributed model is a cascade of these pul elements. The CPW's propagation constant γ and characteristic impedance Z_0 are calculated from the ABCD-matrix of the CPW firstly [19]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cosh(\gamma l) & Z_0 sinh(\gamma l) \\ \frac{1}{Z_0} sinh(\gamma l) & cosh(\gamma l) \end{bmatrix} \tag{8}$$

$$Z_0 = \sqrt{\frac{B}{C}} \tag{9}$$

$$\gamma = \frac{cosh^{-1}(A)}{l} \tag{10}$$

where l is the physical length of the CPW. Next, the parasitic resistance (R), the parasitic inductance (L), the parasitic conductance (G), and the parasitic capacitance (C) of the CPW can be calculated with the propagation constant γ and the characteristic impedance Z_0 [19]. The parasitics of the total stitch-chip channel (CMIs+CPW+CMIs) are a summation of the parasitics from the CPW's distributed model and from two CMIs' lumped models:

$$R_{tot} = R_{CPW} + 2R_{CMI} = l \times real(\gamma Z_0) + 2R_{Z/Y} \tag{11}$$

$$L_{tot} = L_{CPW} + 2L_{CMI} = l \times \frac{imag(\gamma Z_0)}{2\pi f} + 2L_{Z/Y} \tag{12}$$

$$G_{tot} = G_{CPW} + 2G_{CMI} = l \times real\left(\frac{\gamma}{Z_0}\right) + 2G_{Z/Y} \tag{13}$$

$$C_{tot} = C_{CPW} + 2C_{CMI} = l \times \frac{imag\left(\frac{\gamma}{Z_0}\right)}{2\pi f} + 2C_{Z/Y} \tag{14}$$

where f is the frequency; $R_{Z/Y}$, $L_{Z/Y}$, $G_{Z/Y}$, and $C_{Z/Y}$ are the parasitic RLGC from CMIs' lumped models.

Fig. 5 shows the lumped models (Π-model and T-model) for the CMIs only. These lumped models are part of the combined parasitics model and their values are used in the parasitics extraction of the total stitch-chip channels. These lumped models use Z- or Y-matrices converted from ABCD-matrices of CMI-only structures.

A two-port Y-matrix of a CMI-only structure is used for the Π-lumped model shown in Fig. 5a, and can be expressed as follows:

$$[\mathbf{Y}] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{15}$$

where Y_{11} and Y_{22} are the input admittances seen through these two ports respectively. Y_{12} and Y_{21} are the transfer admittances between these two ports. The parasitic RLGC can be calculated [19]:

$$R_Y = real\left(\frac{-2}{Y_{12} + Y_{21}}\right) \tag{16}$$

$$L_Y = \frac{imag\left(\frac{-2}{Y_{12}+Y_{21}}\right)}{2\pi f} \tag{17}$$

$$G_Y = real(Y_{11} + Y_{22} + (Y_{12} + Y_{21})) \tag{18}$$

$$C_Y = \frac{imag(Y_{11} + Y_{22} + (Y_{12} + Y_{21}))}{2\pi f} \tag{19}$$

where f is the frequency.

A two-port Z-matrix of a CMI-only structure is used for the T-lumped model shown in Fig. 5b, and can be expressed as follows:

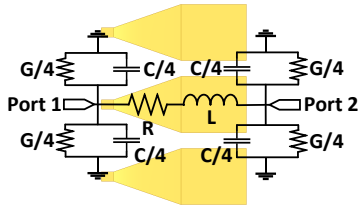
$$[\mathbf{Z}] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{20}$$

where Z_{11} and Z_{22} are the input impedances seen through these two ports respectively. Z_{12} and Z_{21} are the transfer impedances between these two ports. The equations for parasitic RLGC are as follows [19]:

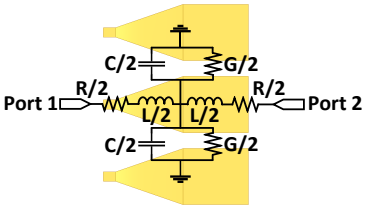
$$R_Z = real(Z_{11} + Z_{22} - (Z_{12} + Z_{21})) \tag{21}$$

$$L_Z = \frac{imag(Z_{11} + Z_{22} - (Z_{12} + Z_{21}))}{2\pi f} \tag{22}$$

$$G_Z = real\left(\frac{2}{Z_{12} + Z_{21}}\right) \tag{23}$$



(a)



(b)

Fig. 5. Lumped parasitics models for CMIs: (a) Π-model and (b) T-model

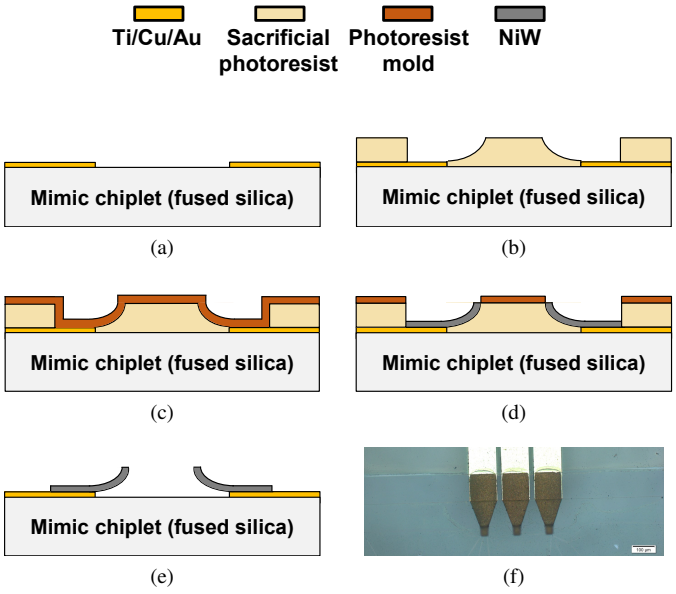


Fig. 6. Mimic chiplet fabrication process: (a) probing pads' lift-off, (b) photoresist patterning after pads' lift-off, (c) photoresist spray coating after seed layer sputtering, (d) photoresist molding and electroplating, (e) CMI releasing, and (f) a top view of CMIs in microscope

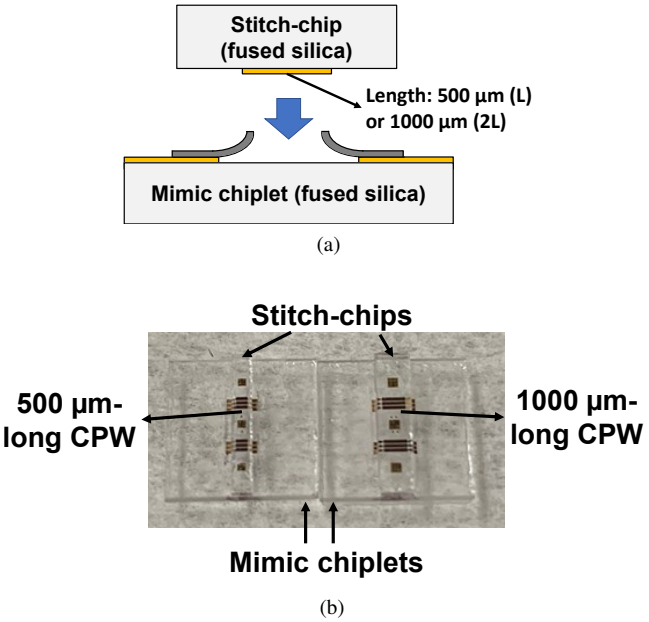


Fig. 7. Assembly: (a) flip-chip bonding of the stitch-chip and the mimic chiplet and (b) samples after assembly

$$C_Z = \frac{imag\left(\frac{2}{Z_{12}+Z_{21}}\right)}{2\pi f} \tag{24}$$

where f is the frequency.

III. Testbed Fabrication and Assembly

The fabrication process is summarized in Fig. 6 and is similar to our previous work [20]. A lift-off process is performed for both the CPWs on the stitch-chips and the probing pads on the mimic chiplets. On the mimic chiplets, a sacrificial photoresist layer is spin-coated. Next, the sacrificial photoresist layer is patterned to obtain a curved sidewall profile through photolithography [10]. After Ti/Cu/Ti seed layer sputtering, another photoresist layer is spray-coated and patterned as a mold for CMI NiW electroplating. Next, the top Ti seed layer is etched away to expose Cu seed layer for electroplating. Following electroplating, the photoresist layers and the seed layer are removed to release the CMIs. Finally, electroless-gold plating is performed to cover all conductive surfaces. Fig. 6f shows a micrograph of fabricated G-S-G CMIs.

As illustrated in Fig. 7a, a flip-chip bonder (Finetech FINEPLACER lambda) is utilized to assemble the stitch-chip and the mimic chiplet. They are held together using epoxy at the edges of the chips (for demonstration purposes). In Fig. 7a, a stitch-chip with 500 μm-long CPWs and a stitch-chip with 1000 μm-long CPWs are assembled separately. The assembled samples are shown in Fig. 7b.

IV. Stitch-Chip Channel Characterization

RF/mm-wave measurements up to 40 GHz were performed using a Keysight N5245A PNA-X network analyzer in a Faraday cage, as shown in Fig. 8. The assembled samples are directly probed by Cascade Microtech 200 μm-pitch G-S-G |Z| probes. Short-open-load-thru (SOLT) calibration (with Cascade Microtech CSR-8 calibration substrate) was used to move the measurement reference plane to the probes' tips. Next, the S-parameters were measured for the assembled samples shown in Fig. 7b and thru-pads structures (500 μm long in G-S-G configuration as shown in Fig. 3a).

A. Measured S-Parameters of Stitch-Chip Channels

The S-parameters measured for the assembled samples and the thru-pads structures are converted to ABCD-matrices firstly and then used to remove probing pads' parasitics using (1) to (3). Next, the resulting ABCD-matrices are converted back to S-parameters, as shown in Fig. 9. Fig. 9 depicts the measured and simulated S-parameters of the stitch-chip channels that represent the actual signal interfaces between

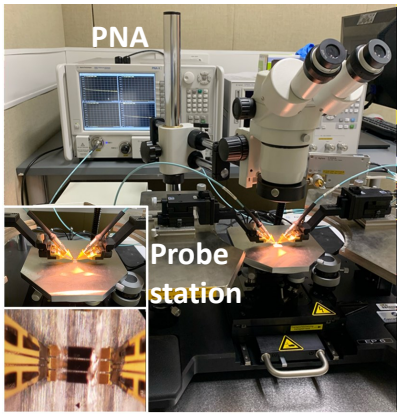


Fig. 8. RF/mm-wave measurements setup (PNA and probe station)

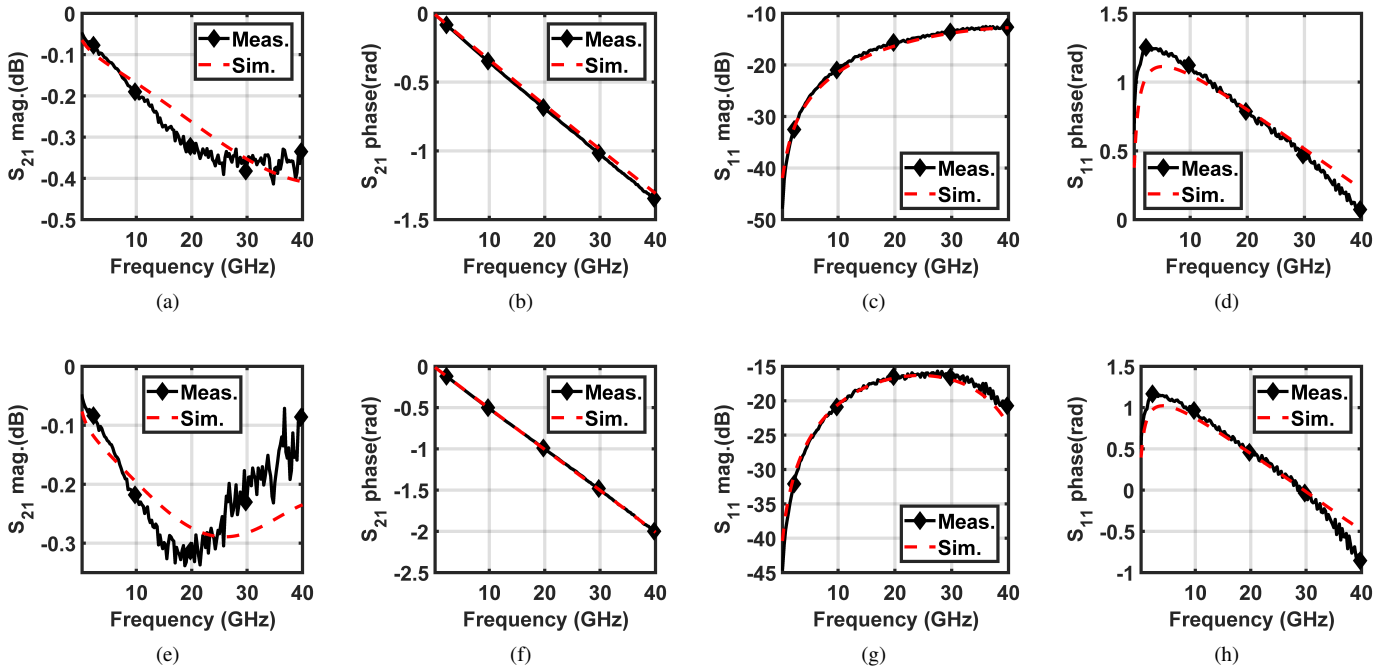


Fig. 9. Measured S-parameters of stitch-chip channels (after removing probing pads, i.e. CPWs with CMIs at both ends): 500 μm-long stitch-chip channel: (a) magnitude of insertion loss, (b) phase of insertion loss, (c) magnitude of return loss, and (d) phase of return loss; 1000 μm-long stitch-chip channel: (e) magnitude of insertion loss, (f) phase of insertion loss, (g) magnitude of return loss, and (h) phase of return loss

chiplets of the proposed polylithic integration technology shown in Fig. 1. In Fig. 9a, the simulated and measured insertion loss magnitude ($|S_{21}|$) at 20 GHz are approximately 0.26 dB (0.971) and 0.33 dB (0.963), respectively, which indicates a difference of 0.82%. The stitch-chip channels exhibit an insertion loss of less than 0.42 dB up to 40 GHz, which suggests their potential to provide ultra low-loss signal interfaces for RF/mm-wave systems. In Fig. 9e, the low-loss sample may be susceptible to background noise, as seen by the ripples at high frequencies. In addition, the stitch-chip channels show acceptable return loss (RL>12.7 dB).

Note that in Fig. 9a and Fig. 9e, after approximately 20 GHz, the 1000 μm long stitch-chip channel shows lower insertion loss than the 500 μm long channel. This could be an outcome of the 1000 μm long channel's lower return loss at high frequencies due to possible resonance around 40 GHz (more L and C from longer channel cause resonance to shift to lower frequency), as shown in Fig. 9g. Generally, lower return loss results in lower reflection coefficient and higher transmission coefficient, which leads to lower insertion loss.

B. Parasitics Extraction of Stitch-Chip Channels

To extract the parasitics of the total stitch channel, 500 μm-long CPWs are measured to obtain S-parameters and then converted to ABCD-matrix. Next, following the de-embedding and parasitics extraction procedure in Section II, the total parasitics of a 500 μm-long stitch-chip channel from the combined parasitics model can be obtained, as shown in Fig. 10.

As shown in Fig. 10b and Fig. 10c, the measured parasitic L and G are in good agreement with the simulations. However,

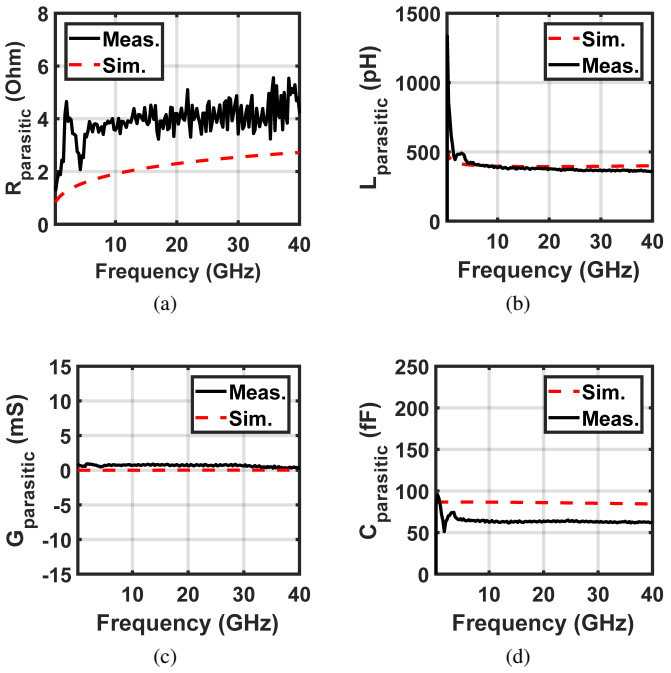


Fig. 10. Parasitics extraction of stitch-chip channels using the combined model: (a) parasitic R, (b) parasitic L, (c) parasitic G, and (d) parasitic C

the contact resistance between the CMI and the CPW on the stitch-chips is not accounted for in the model due to its complexity in the actual assembly. This limitation contributes to most of the discrepancy of the measured parasitic R from the simulation, as shown in Fig. 10a. In addition, the measured parasitic R and C could suffer from SOLT calibration error

resulting from such wide-band calibration [22] and process variations (e.g., fabricated dimensions differ from mask design). The ripples in the measured R is suspected to be an outcome of the high frequency noise during such low-loss measurements.

The total parasitics of the 500 μm-long stitch-chip channel are 4.68 Ω at 28 GHz, 4.99 Ω at 39 GHz, 359 pH up to 40 GHz, and 62 fF up to 40 GHz. The parasitic L and C remain relatively constant across the 40 GHz bandwidth, while the parasitic R increases due to skin depth. With the optimization of chiplet position, the total physical length of a stitch-chip channel could approach 100 μm or less, which implies extreme low-parasitic chiplet-to-chiplet signal propagation in the proposed polylithic integration technology.

V. CMI Characterization

Prior papers have reported the CMI's mechanical characteristics and DC resistance [23], [24]. In [23], a CMI free of plastic deformation is reported; the CMI recovers its original profile after 5000 cycles of 30 μm indentations. This section focuses on the RF/mm-wave characterization of the CMIs.

A. Measured S-Parameters of CMIs

Using the L-2L de-embedding technique in Section II, the resulting ABCD-matrix of G-S-G CMIs (30 μm in height and ~367 μm in length, as shown in Fig. 2b) can be obtained and converted back to S-parameters (up to 40 GHz), as shown in Fig. 11. The magnitude and the phase angle of the measured results match well to the simulations. However, mismatches are observed and suspected to be an outcome of the measurement noise and process variations in the testbeds, such as electroplated metal thickness variation. The return loss of the CMIs is better than 16.2 dB up to 40 GHz, while the insertion loss is below 0.2 dB.

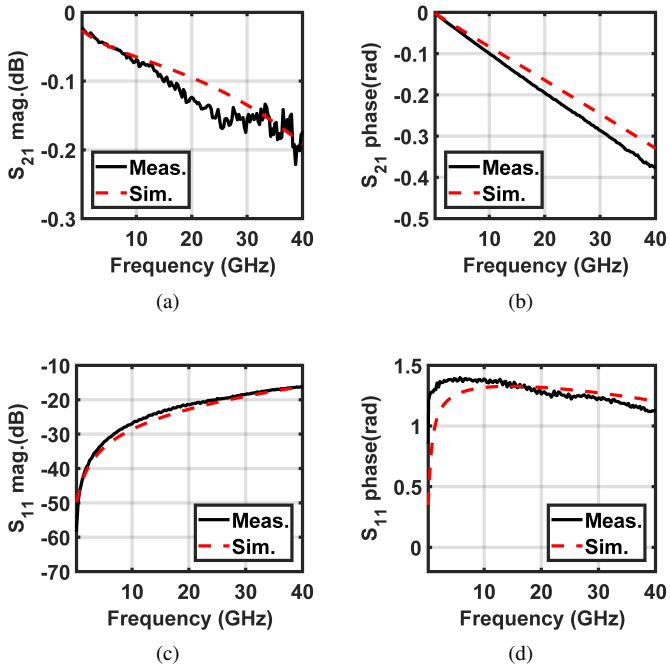


Fig. 11. Measured S-parameters of CMIs using L-2L de-embedding: (a) insertion loss magnitude, (b) insertion loss phase, (c) return loss magnitude, and (d) return loss phase

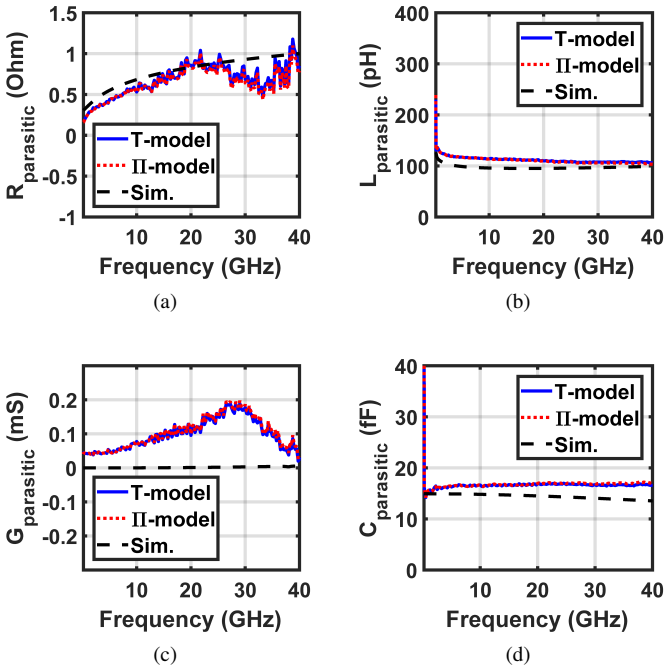


Fig. 12. Parasitics extraction of CMIs using the lumped models: (a) parasitic R, (b) parasitic L, (c) parasitic G, and (d) parasitic C

B. Parasitics Extraction of CMIs

To extract CMIs' parasitics, their measured S-parameters are converted to the Z/Y-parameters for the lumped model extraction, as shown in Section II. The parasitic RLGC of the G-S-G CMIs are depicted in Fig. 12. Because CMIs are electrically short up to 40 GHz, the generated results from these two lumped models are similar. Table I summarizes the measured CMIs' parasitics in this work and the simulated parasitics of CMIs with varied pitch and height. With pitch scaling, parasitics decrease except parasitic R, as DC resistance increases due to smaller cross-sectional area of the conductor.

In Fig. 12a, the measurement shows larger fluctuations at high-frequencies (>~20 GHz), which could be due to the measurement noise. The difference between the simulation and the measurement shown at high-frequencies is suspected to be a result of the calibration error [22] and process variations.

In Fig. 12c, the measurement and the simulation are divergent. Theoretically, each CMI is surrounded by air, which should result in virtually zero parasitic G. However, in the actual fabrication, photoresist residuals could appear between signal-CMI and ground-CMI after sacrificial photoresist layer removal and seed layer etching, which may increase the CMIs' parasitic G. More importantly, the fused silica underneath CMIs' pads could increase the measured parasitic G, which is not fully accounted for in the simulation.

TABLE I
SUMMARY OF CMIS' PARASITICS AT SELECTED RF/MM-WAVE FREQUENCIES.

	28 GHz				39 GHz			
Pitch/ height (μm)	**R (Ω)**	**L (pH)**	**G (μS)**	**C (fF)**	**R (Ω)**	**L (pH)**	**G (μS)**	**C (fF)**
200/30 (meas.)	0.71	106	170	17	0.99	105	70	17.2
200/30 (sim.)	0.91	96.3	2.5	14.2	0.99	98.9	5.2	13.6
200/60 (sim.)	0.92	102	0.7	14	1	106	4.4	13
150/30 (sim.)	0.96	96	3	12.5	1.01	94.5	1.4	12.9
50/30 (sim.)	1.67	71.6	9.9	8.9	1.75	69.1	16	9.4

VI. BENCHMARKING OF SIGNAL CHANNELS AND OFF-CHIP I/OS

A. Benchmarking of Signal Channels

Table II shows the insertion loss of signal channels in different technologies. Technologies using high resistivity (HR) silicon, glass, and organic substrates are commonly implemented for packaging RF/mm-wave chiplets.

The fused-silica stitch-chip channel shows relatively lower insertion loss than HR silicon interposer channel due to its lower dielectric constant and loss tangent. For other Si interposer technologies, an additional simulation is performed as follows: 1) CPWs with 50 Ω characteristic impedance are designed on standard silicon (10 S/m conductivity) with 1 μm-thick silicon dioxide [20]; 2) Solder bumps, instead of CMIs, are implemented as off-chip interconnects at the ends of the CPWs [20]. The fused-silica stitching technology demonstrates approximately 3.8 dB loss improvement to the simulated Si interposer technology.

When comparing glass interposer, organic substrate, and integrated fan-out (InFO) wafer level packaging, the stitching technology shows similar insertion loss with several added benefits: first, the mechanical compliance of the CMIs used in the stitching technology can enable the integration of RF/mm-wave chiplets and components made using different materials (e.g., GaN, GaAs, ceramic, etc.) regardless of their CTE mismatch. In addition, the CMI's mechanical compliance can improve the package-level thermomechanical reliability, such as reducing thermally induced package warpage [34]; second, CMIs can provide temporary interconnections, which can offer a testing solution for known good die (KGD) and improve package yield by facilitating chiplet replacement/rework; third, as CMIs are pressure-based interconnects, they are compatible with any contact pad material; lastly, the stitching technology focuses on localized low-loss signal interfaces that can be applied on any package substrate.

A comparison between EMIB with comparable fine-pitch stitch-chip channels is also included in Table II for reference. After scaling the pitch of the stitch-chip channel to be reasonably comparable with EMIB, the new generated stitch-chip channel model is simulated to obtain S-parameters. Compared with EMIB, stitch-chips with fine-pitch channels reduce the insertion loss by approximately 13 dB. The large loss shown for fine-pitch EMIB channel is partially due to the small cross-sectional area of the traces and lossy Si substrate [29].

The extracted parasitics of the stitch-chip channels are benchmarked to other technologies, as shown in Table III. For RF/mm-wave chiplets, embedded wafer-level ball-grid array (eWLB) has gained attention for its small form factor, improved electrical and thermal performances, etc [35]. The stitch-chip channel shows similar capacitance but higher inductance and resistance than those of eWLB. However, eWLB demands precise die positioning, die shift control, and package warpage control during processing [35].

In Table III, parasitics are also compared among Si-based technologies mainly for digital chiplets. To the authors' best knowledge, only transmission lines' parasitics are reported for Si interposer channels, while the stitch-chip channels' parasitics in this work include both transmission lines and CMIs as off-chip I/Os. Therefore, the data reported for Si interposer channels are underestimated when comparing the total signal link consisting of off-chip I/Os and transmission lines. In this comparison, the parasitics of the stitch-chip channels are lower thanks to shorter channel length and low-loss substrate material: the parasitic L and C are decreased by approximately 66.7% and 89.4% respectively, compared with the results in [31].

B. Benchmarking of Off-Chip I/Os

Table IV compares the loss and frequency-dependent parasitics of bumps and the CMIs in this work. The table also includes the best simulated values of electrically optimized CMIs (lowest insertion loss and return loss while minimizing equivalent stress during assembly). This could be realized by simply shortening the CMIs length but maintaining pitch and height. Comparable or lower insertion loss is observed for CMIs with similar pitch and height to bumps [36], [38] (approximately 150 to 200 μm pitch and 30 to 35 μm height). For example, the CMIs with 150 μm pitch and 30 μm height possess similar insertion loss (approximately 2.45% difference) as solder bumps with the same dimensions [36]. However, CMIs measured in this paper (30 μm in height and $\sim$367 μm in length, as shown in Fig. 2b) may possess relative higher resistance (340 mΩ at 2.5 GHz) and inductance (113.5 pH up to 14.5 GHz); the simulated resistance and a measured inductance of solder bumps (300 μm-pitch and 55 μm-height) are 11.7 mΩ at 2.5 GHz and 66 pH up to 14.5 GHz [37]. In addition, CMIs could overcome solder bumps' shortcomings such as IMC formation, shorting as pitch scales, and enable simple rework. CMIs do not require underfill to assemble, which leads to even lower parasitic G and C. To

TABLE II
COMPARISON OF SIGNAL CHANNELS.

Technology	**Channel length /pitch**	**Off-chip I/O /height**	**Insertion loss**
High resistivity silicon interposer [25]	1 mm/-	-/-	0.94 dB @ 40 GHz
Glass interposer [26]	1.86 mm/188 μm	-/-	$\sim$0.56 dB @ 28 GHz
Organic substrate [27]	1.35 mm/-	Au bumps/50 μm	$\sim$0.3 dB @ 40 GHz
InFO [28]	4 mm/-	-/-	1.12 dB @ 39 GHz
Silicon interposer (sim.)	1 mm/200 μm	Solder bumps/30 μm	$\sim$3.8 dB @ 28 GHz $\sim$4.0 dB @ 39 GHz
EMIB [29], [30] (shown as reference)	1 mm/$\sim$4 μm	Microbumps and vias/-	$\sim$14 dB @ 25 GHz
This work (meas.)	1 mm/200 μm	CMIs/30 μm	$\sim$0.2 dB @ 28 GHz $\sim$0.2 dB @ 39 GHz
This work (sim.)	1 mm/4 μm	CMIs/30 μm	$\sim$1.15 dB @ 25 GHz

TABLE III
PARASITICS COMPARISON OF SIGNAL CHANNELS.

Technology	Silicon interposer [31]	Silicon interposer [32]	EMIB [30] (shown as reference)	eWLB [33]	**This work (meas.)**	**This work (sim.)**
Transmission line typical length/pitch	3 mm/4 to 6 μm (Microstrip)	10 mm/20 μm (CB-CPW)	$<$10 mm/4 μm (Microstrip)	-/107 μm (CPW)	0.5 mm/200 μm (CPW)	0.5 mm/4 μm (CPW)
Off-chip I/O/height	Microbumps/-	-/-	Microbumps and vias/-	-/-	CMI/30 μm	CMI/30 μm
R (Ω)	33.87 to 36.94 (28 and 39 GHz)	15 (3.5 GHz)	-	$\sim$0.78/mm (10 GHz)	4.68 to 4.99 (28 and 39 GHz)	10.12 to 11.03 (28 and 39 GHz)
L (nH)	0.78	2.9	-	$\sim$0.27/mm	0.36	0.26
C (pF)	0.63	1.6	-	$\sim$0.12/mm	0.062	0.067

further optimize the electrical performance, a material having higher conductivity and larger skin depth at high frequencies (e.g., copper) might be selected as the core of CMIs during fabrication.

VII. CONCLUSION

In this paper, a polylithic integration technology is demonstrated with a testbed, which emulates a fully assembled stitch-chip system for RF/mm-wave systems. Modeling, fabrication, assembly, characterization, and benchmarking are reported. The measurements suggest that the 500 μm-long stitch-chip channels are ultra low-loss (less than 0.42 dB insertion loss up to 40 GHz) and with minimal parasitics (4.68 Ω at 28 GHz, 4.99 Ω at 39 GHz, 359 pH up to 40 GHz, and 62 fF up to 40 GHz). The stitching technology shows lower loss than other Si-based technologies: given the same pitch and length, the loss improvement is approximately 3.8 dB up to 40 GHz. Moreover, compared with other technologies, such as glass interposer technology, organic substrate technology, and InFO, the stitching technology has similar loss with a benefit of simple rework.

CMIs' S-parameters are extracted by L-2L de-embedding technique up to 40 GHz. The results show that the CMIs possess less than 0.2 dB insertion loss and better than 16.2 dB return loss. In addition, their parasitics are extracted using

TABLE IV
COMPARISON BETWEEN CMIS AND OTHER OFF-CHIP I/OS (INCLUDING PADS).

Off-chip I/O	Solder bumps [36]	Solder bumps [37]	Au bumps [38]	Flip-chip bumps [39]	Au bumps [40]	**CMIs (meas.)**	**CMIs (sim.)**	**CMIs optimization (best value)**
Pitch/height (μm)	150/30	300/55	$\sim$155 to 180/35	>100/20	100/22	200/30	150/30	200/30
Insertion loss	<0.4 dB up to 40 GHz	-	<0.2 dB up to 35 GHz	<0.4 dB up to 40 GHz	<0.3 dB up to 90 GHz	<0.22 dB up to 40 GHz	<0.18 dB up to 40 GHz	<0.14 dB up to 40 GHz
R (mΩ)	-	11.7 (2.5 GHz)	-	-	-	340 (2.5 GHz)	509.3 (2.5 GHz)	>94.4 (2.5 GHz)
L (pH)	-	66	-	90	-	113.5	98.9	>12.9
C (fF)	-	-	-	86	-	17	12.5	>14.8

lumped circuit models for the first time. The results, compared with bumps, suggest that CMIs could possess comparable loss but higher resistance and inductance, which requires future optimization (e.g., thicker gold coating). In addition, the CMIs could overcome solder bumps' common issues, such as IMC formation, shorting as pitch scales, and enable simple rework, especially for packaging with a large number of chiplets to improve package yield.

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REFERENCES

[1] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[2] K. K. Samanta, "Pushing the envelope for heterogeneity: multilayer and 3-D heterogeneous integrations for next generation millimeter- and submillimeter-wave circuits and systems," *IEEE Microw. Mag.*, vol. 18, no. 2, pp. 28–43, Mar. 2017.

[3] I. Ndip and K. Lang, "Roles and requirements of electronic packaging in 5G," in *Proc. 2018 7th Electron. Syst. Integration Technol. Conf. (ESTC)*, Dresden, Germany, Sep. 2018, pp. 1–5.

[4] A. O. Watanabe, M. Ali, S. Y. B. Sayeed, R. R. Tummala, and M. R. Pulugurtha, "A review of 5G front-end systems package integration," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 11, no. 1, pp. 118–133, Jan. 2021.

[5] S. Shinjo, K. Nakatani, K. Tsutsumi, and H. Nakamizo, "Integrating the front end: a highly integrated RF front end for high-SHF wide-band massive MIMO in 5G," *IEEE Microw. Mag.*, vol. 18, no. 5, pp. 31–40, Jul. 2017.

[6] X. Gu *et al.*, "Development, implementation, and characterization of a 64-element dual-polarized phased-array antenna module for 28-GHz high-speed data communications," *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 7, pp. 2975–2984, Jul. 2019.

[7] X. Gu, D. Liu, and B. Sadhu, "Packaging and antenna integration for silicon-based millimeter-wave phased arrays: 5G and beyond," *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 123–134, Jan. 2021.

[8] Y. P. Zhang and D. Liu, "Antenna-on-chip and antenna-in-package solutions to highly integrated millimeter-wave devices for wireless communications," *IEEE Trans. Antennas Propag.*, vol. 57, no. 10, pp. 2830–2841, Oct. 2009.

[9] O. E. Bouayadi *et al.*, "Silicon interposer: A versatile platform towards full-3D integration of wireless systems at millimeter-wave frequencies," in *Proc. 2015 IEEE 65th Electron. Compon. Technol. Conf. (ECTC)*, San Diego, CA, May 2015, pp. 973–980.

[10] P. K. Jo, M. Zia, J. L. Gonzalez, H. Oh, and M. S. Bakir, "Design, fabrication, and characterization of dense compressible microinterconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 7, no. 7, pp. 1003–1010, Jul. 2017.

[11] Accessed 15 Apr. 2021. [Online]. Available: https://www.formfactor.com/products/probe-cards/?_probe_cards=family-pyrana-rf

[12] Accessed 15 Apr. 2021. [Online]. Available: https://www.samtec.com/connectors/high-speed-board-to-board/compression-interposers/zray

[13] C. Zhan, C. Chuang, J. Juang, S. Lu, and T. Chang, "Assembly and reliability characterization of 3D chip stacking with 30μm pitch lead-free solder micro bump interconnection," in *Proc. 2010 60th Electron. Compon. Technol. Conf. (ECTC)*, Las Vegas, NV, Jun. 2010, pp. 1043–1049.

[14] M. Wojnowski, G. Sommer, A. Klumpp, and W. Weber, "Electrical characterization of 3D interconnection structures up to millimeter wave frequencies," in *Proc. 2008 10th Electron. Packag. Technol. Conf. (EPTC)*, Singapore, Singapore, Dec. 2008, pp. 1393–1402.

[15] Y. Chang, D. Chang, S. S. H. Hsu, J. Lee, S. Lin, and Y. Juang, "A matrix-computation based methodology for extracting the S-parameters of interconnects in advanced packaging technologies," in *Proc. Asia-Pacific Microw. Conf. 2011*, Melbourne, VIC, Dec. 2011, pp. 1909–1912.

[16] Y. Li *et al.*, "Electromagnetic characteristics of multiport TSVs using L-2L de-embedding method and shielding TSVs," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 5, pp. 1541–1548, Oct. 2017.

[17] H. Yen *et al.*, "TSV RF de-embedding method and modeling for 3DIC," in *Proc. 2012 SEMI Adv. Semicond. Manuf. Conf.*, Saratoga Springs, NY, May 2012, pp. 394–397.

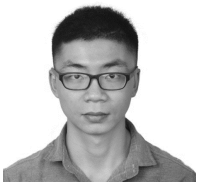
[18] I. Ndip *et al.*, "Analytical, numerical-, and measurement–based methods for extracting the electrical parameters of through silicon vias (TSVs)," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 3, pp. 504–515, Mar. 2014.

[19] Z. Xu, X. Gu, and J. Lu, "Parasitics extraction, wideband modeling and sensitivity analysis of through-strata-via (TSV) in 3D integration/packaging," in *Proc. 2011 IEEE/SEMI Adv. Semicond. Manuf. Conf.*, Saratoga Springs, NY, May 2011, pp. 1–6.

[20] T. Zheng, P. K. Jo, S. Kochupurackal Rajan, and M. S. Bakir, "Polylithic integration for RF/mm-wave chiplets using stitch-chips: modeling, fabrication, and characterization," in *Proc. 2020 IEEE MTT-S Int. Microw. Symp. (IMS)*, Aug. 2020, pp. 1035–1038.

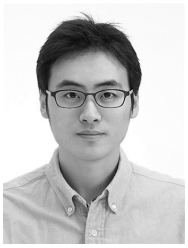
[21] C. Zhang, H. S. Yang, and M. S. Bakir, "Highly elastic gold passivated mechanically flexible interconnects," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 10, pp. 1632–1639, Oct. 2013.

[22] A. Davidson, E. Strid, and K. Jones, "Achieving greater on-wafer S-parameter accuracy with the LRM calibration technique," in *Proc. 34th ARFTG Conf. Dig.*, vol. 16, Ft. Lauderdale, FL, Nov. 1989, pp. 61–66.
[23] P. K. Jo, M. Zia, J. L. Gonzalez, and M. S. Bakir, "Dense and highly elastic compressible microinterconnects (CMIs) for electronic microsystems," in *Proc. 2017 IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, May 2017, pp. 684–689.
[24] P. K. Jo, X. Zhang, J. L. Gonzalez, G. S. May, and M. S. Bakir, "Heterogeneous multi-die stitching enabled by fine-pitch and multi-height compressible microinterconnects (CMIs)," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2957–2963, Jul. 2018.
[25] J. Yan *et al.*, "Fabrication and RF property evaluation of high-resistivity Si interposer for 2.5-D/3-D heterogeneous integration of RF devices," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 11, pp. 2012–2020, Nov. 2018.
[26] A. O. Watanabe *et al.*, "First demonstration of 28 GHz and 39 GHz transmission lines and antennas on glass substrates for 5G modules," in *Proc. 2017 IEEE 67th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, May 2017, pp. 236–241.
[27] W. T. Khan, A. Ulusoy, R. L. Schmid, and J. Papapolymerou, "Characterization of a low-loss and wide-band (DC to 170 GHz) flip-chip interconnect on an organic substrate," in *Proc. 2014 IEEE MTT-S Int. Microw. Symp. (IMS)*, Tampa, FL, Jun. 2014, pp. 1–4.
[28] C.-H. Tsai *et al.*, "High performance passive devices for millimeter wave system integration on integrated fan-out (InFO) wafer level packaging technology," in *Proc. 2015 IEEE Int. Electron Devices Meeting (IEDM)*, Washington, DC, Dec. 2015, pp. 25.2.1–25.2.4.
[29] W. T. Beyene *et al.*, "Signaling analysis and optimal channel data rates for high-performance FPGA interfaces," in *Proc. 2018 IEEE 27th Conf. Elect. Perform. Electron. Packag. Syst. (EPEPS)*, San Jose, CA, Oct. 2018, pp. 17–19.
[30] R. Mahajan *et al.*, "Embedded multi-die interconnect bridge (EMIB) – a high density, high bandwidth packaging interconnect," in *Proc. 2016 IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, Las Vegas, NV, May 2016, pp. 557–565.
[31] K. Cho *et al.*, "Signal integrity design and analysis of silicon interposer for GPU-memory channels in high-bandwidth memory interface," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 9, pp. 1658–1671, Sep. 2018.
[32] R. Weerasekera *et al.*, "High bandwidth interconnect design opportunities in 2.5D through-silicon interposer (TSI)," in *Proc. 2016 IEEE 18th Electron. Packag. Technol. Conf. (EPTC)*, Singapore, Singapore, Nov. 2016, pp. 241–244.
[33] M. Wojnowski, M. Engl, M. Brunnbauer, K. Pressel, G. Sommer, and R. Weigel, "High frequency characterization of thin-film redistribution layers for embedded wafer level BGA," in *Proc. 2007 9th Electron. Packag. Technol. Conf.*, Singapore, Singapore, Dec. 2007, pp. 308–314.
[34] M. O. Hossen, J. L. Gonzalez, and M. S. Bakir, "Thermomechanical analysis and package-level optimization of mechanically flexible interconnects for interposer-on-motherboard assembly," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 12, pp. 2081–2089, Dec. 2018.
[35] M. Brunnbauer, T. Meyer, G. Ofner, K. Mueller, and R. Hagen, "Embedded wafer level ball grid array (eWLB)," in *Proc. 2008 33rd IEEE/CPMT Int. Electron. Manuf. Technol. Conf. (IEMT)*, Penang, Malaysia, Nov. 2008, pp. 1–6.
[36] K. B. Unchwaniwala and M. F. Caggiano, "Electrical analysis of IC packaging with emphasis on different ball grid array packages," in *Proc. 2001 51st Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, May 2001, pp. 1496–1501.
[37] I. N. Ndip, G. Sommer, W. John, and H. Reichl, "Characterization of bump arrays at RF/microwave frequencies," *Microelectronics Reliability*, vol. 45, no. 3, pp. 551–558, Mar. 2005.
[38] C.-L. Wang and R.-B. Wu, "Modeling and design for electrical performance of wideband flip-chip transition," *IEEE Trans. Adv. Packag.*, vol. 26, no. 4, pp. 385–391, Nov. 2003.
[39] D. Staiculescu, A. Sutono, and J. Laskar, "Wideband scalable electrical model for microwave/millimeter wave flip chip interconnects," *IEEE Trans. Adv. Packag.*, vol. 24, no. 3, pp. 255–259, Aug. 2001.
[40] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 5, pp. 871–878, May 2001.



Ting Zheng (S'18) received the B. S. degree (Hons.) in microelectronics from Nanjing University, Nanjing, China, in 2016. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the Georgia Institute of Technology, Atlanta, GA, USA.

His current research interests include 2.5D/3D heterogeneous integration using stitching technology and microfabricated flexible interconnect technology for RF/mm-wave applications.



Paul K. Jo (S'15) received the B.S. degree (Hons.) and the M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2009 and 2011, respectively. He received the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA in 2019.

Sreejith Kochupurackal Rajan (S'18) received the B.Tech. degree in electronics and communication engineering from the Cochin University of Science and Technology, Kochi, India, in 2013, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2016, where he is currently pursuing the Ph.D. degree in electrical and computer engineering.

His current research interests include the study of interconnection and thermal challenges in advanced heterogeneous integration architectures.

Muhannad S. Bakir (SM'12) is a Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA. His current research interests include 3-D electronic system integration, advanced cooling, and power delivery for 3-D systems, biosensors and their integration with CMOS circuitry, and nanofabrication technology.

Dr. Bakir was a recipient of the 2013 Intel Early Career Faculty Honor Award, the 2012 DARPA Young Faculty Award, and the 2011 IEEE CPMT Society Outstanding Young Engineer Award. His research group has received more than 20 conference and student paper awards including six from the IEEE Electronic Components and Technology Conference (ECTC), four from the IEEE International Interconnect Technology Conference (IITC), and one from the IEEE Custom Integrated Circuits Conference (CICC). His group received the 2014 Best Paper of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY in the area of advanced packaging. He is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES and an Associate Editor of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY. In 2015, he was elected by the IEEE CPMT Society to serve as a Distinguished Lecturer for a four-year term.