Comparison of Electrical Characteristics of Schottky Junctions based on CdS Nanowires and Thin Film

Hongmei Dang[1], Esther Ososanya[1] and Nian Zhang[1]

[1]Department of Electrical and Computer Engineering, University of the District of Columbia

Abstract:

CdS nanowires and film Schottky diodes are fabricated and diode properties are compared. Effect of SnO_2 on CdS film diode properties is investigated. CdS film/ Au on 100nm SnO_2 substrate demonstrates like-resistor characteristics and increase in SnO_2 thickness corrects resistor behavior, however the effective reverse saturation current density J_o is significantly high and shunt resistance are considerably low, implying that SnO_2 slightly prevents impurities migration from CdS films into ITO but cause additional issues. Thickness of CdS film on diode properties is further investigated and increasing CdS film thickness improved J_o by one order of magnitude, however shunt resistance is obviously low, suggesting intrinsic issues in CdS film. 100nm CdS nanowire/Au diodes reduce J_o by three orders of magnitude in the dark and two orders of magnitude in the light respectively and their shunt resistance is significantly enhanced by 70 times when comparing with those of the CdS film diodes. The wide difference can be attributed to the fact that CdS nanowires overcome intrinsic issues in CdS film and thus demonstrate significantly well-defined diode behavior. Simulation found that CdS nanowire diodes have low compensating acceptor type traps and interface state density of $5.0*10^9/cm^2$, indicating that interface recombination isn't a dominated current transport mechanism in the nanowire diodes. CdS film diodes are simulated with acceptor traps and interface state density increased by two order of magnitude and shunt resistance reduced by one order of magnitude, indicating that high density of interface states and shunt paths occur in the CdS film diodes.

Keywords *Nanowire Schottky diodes, reverse saturation current, shunt resistance, recombination*

Introduction

Cadmium sulphide (CdS) is one of the most promising II-VI semi-conductor materials because of appropriate band structure [1, 2]. It's film form has a direct, energy gap of 2.4 eV, resulting in an absorption coefficient $>10^4$ cm^{-1} for wavelength less than 500nm [1-3]. Due to high light absorption coefficient, it needs only thin layer to absorb >90% of light above the band gap. CdS can be natively *n*-doped and the carrier density even reaches 1.6×10^{18} cm^{-3} [4]. CdS has been widely used in sensors [5, 6], photodetectors[7], light emitting diodes[8], logic circuits[9], photocatalyst for water splitting [1] as fuel cells which are applied for electrical vehicles. In addition, CdS was recognized to be the most effective heterojunction partner of II-VI solar cells and has been widely applied into these II-VI solar cells such as CdTe [10, 11], CZTS [12] and Sb_2Se_3 solar cells[13]. However, there is a great challenge regarding the application CdS film, because the fast recombination of photo-excited electron hole pairs in CdS film reduce photocatalytic activity, photodetector response and photocurrent in solar cells etc[1, 10]. Considerable efforts have been carried out to exploit feasible approaches to reduce recombination and enhance photo-response of CdS film based devices, including reducing CdS thickness [10], doping strategy [14] and co-catalyst modifying methods [1].

Nanoparticles, nanorods and nanowires have been used to tune optical and electrical properties, improve photon generation and electron-hole combination[1, 2, 15, 16]. Oriented and aligned nanostructures have shown excellent performance in various piezoelectric nanogenerator [17], optoelectronics [15, 18] and electronic devices[19, 20]. Inspired by wide applications of CdS and nanostructures, here we fabricate CdS nanowires and configure the CdS nanowire into Schottky diodes. As comparison, CdS film/Au diodes are fabricated. We further characterize electrical properties of CdS nanowires/Au diodes, develop a simulation model to quantitatively analyze their

I-V characteristics and further compare their properties with CdS film diodes. Investigation in this work gives novel insight into CdS nanowires and can find wide applications such as fuel cells for electrical vehicles[1, 21], various solar cells [11] and photodetectors [7], transistors etc [19, 22].

1. Experimental Procedures

1.1 Formation of Alumina Matrix: CdS nanowires were grown with highly oriented and well aligned arrays by an alumina- matrix-assisted deposition method. Figure 1 shows visual images of fabrication steps for CdS nanowires. Firstly, alumina- matrix was prepared by following procedures. RF sputtering deposited 100nm intrinsic tin oxide SnO_2 and then 5nm titanium on ITO glass substrate. Electron beam evaporation deposited 100nm/200nm thick aluminum on the substrate, as shown Figure 1(a). Next, 0.3M oxalic acid solution was prepared to anodize Al/Ti/SnO_2/ITO glass substrate under 50V DC bias until Al substrate became transparent, indicating that Al layer has become to alumina- matrix. It has been found that there was a barrier layer between alumina-matrix and SnO_2/ITO glass substrate due to insertion of 5nm titanium, which prevents growth of nanowires by alumina- matrix. Therefore, 5% phosphoric acid was used to etch samples for 30 minutes to partially remove the barrier layer. Reactive ion etch (RIE) process was set with RF and ICP power to completely remove the barrier layer. The samples were etched in 5% phosphoric acid for 5 minutes and rinsed by deionized water[11]. The barrier-free transparent alumina- matrix with nanopores were formed on SnO_2/ITO glass substrate, where the visual image is shown in Figure 1(b).

1.2 Growth of CdS Nanowire: An eletrodeposition method was developed to embed CdS into alumina- matrix nanopores. The visual image of CdS nanowires/ SnO2/ ITO/ the glass is shown in Figure 1(c), and the corresponding SEM image for the CdS nanowires is shown in Figure 1(d). Specifically, the CdS nanowires were grown in electrolyte with a mixture of 0.055M cadmium chloride and 0.19M

sulfur in 50mL dimethyl-sulfoxide (DMSO) solution, under dc current density of 7mA/cm^2 and deposition temperature of 120-160°C. It is observed that all of the nanopores with completely removed barrier layer can be filled efficiently with CdS nanowires under dc bias. Therefore, the barrier layer removing procedure is crucial to form uniform and dense CdS nanowires. Following growth, the CdS nanowires were annealed at 400℃ for 30 minutes with 100-sccm Argon purge[11].

1.3 Formation of CdS/Au diode structure: CdS/Au diode structure was formed by following procedures. 0.1M NaOH solution is used to selectively remove alumina-matrix for 1 min and partially expose CdS nanowires. The thermal evaporation is used to deposit 100nm Au on the CdS nanowires, resulting in CdS nanowires/Au Schottky diodes. For comparison, 100nm/200nm/400nm planar CdS thin film was deposited on 100nm/175nm/250nm/325nm SnO_2/ITO glass substrate by well-established chemical bath deposition and 100nm Au was deposited on the top to form CdS film/Au Schottky diode structure.

1.4 Characterization: Material characterization of the CdS nanowires was conducted with a scanning electron microscope (Hitachi S-900 field emission SEM). For diode characterization, electrical properties of CdS nanowire /Au Schottky diodes and CdS film/Au Schottky diodes were characterized as comparison. The current density versus voltage (J–V) were measured at illumination intensity of 100 mW cm^{-2} and at the dark, where gold contact was biased positively with respect to the bottom ITO. Simulations of J-V characteristics of CdS nanowires/Au and CdS film/Au diodes were performed by SCAPS software[23]. By fitting J-V simulations with measured J-V characteristics, we established numerical models to investigate electrical property mechanism of CdS nanowires/Au diodes compared with CdS film/Au diodes. This work focuses on CdS nanowire mechanism, investigation in this work will give insight into other CdS nanowire-based devices and can find wide application in solar cells, fuel cells and photodetectors ect [1].

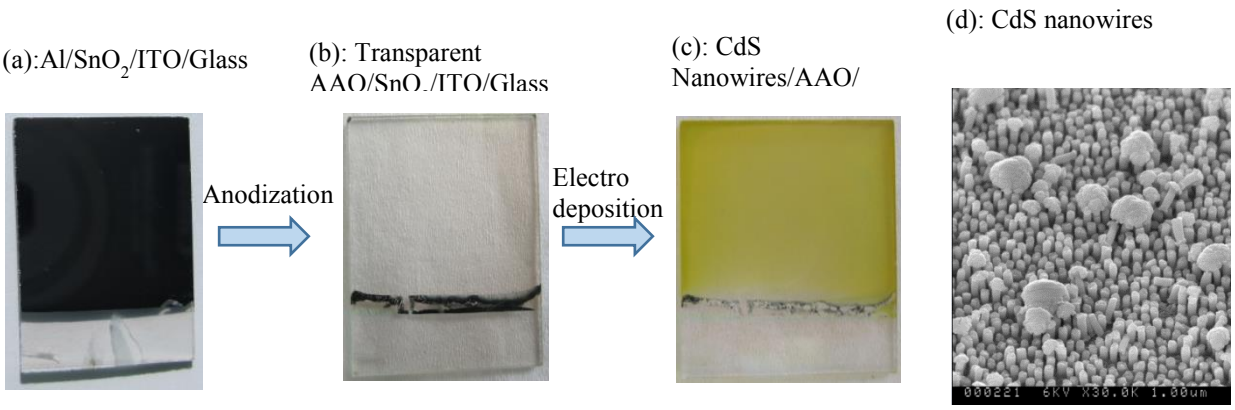

Figure 1. Visual images of fabrication steps for CdS nanowires including (a) aluminum deposited on the top of a substrate,(b) formation of AAO matrix and (c) CdS nanowires filled in the nanopores of AAO matrix; and (d) top view SEM image of CdS nanowires.

2. Results and Discussion

For comparison, J-V characteristics of Au/ CdS film with 100nm thickness on 100nm SnO_2/ITO glass substrate (100nm CdS film diodes on 100nm SnO_2) were measured in dark and under "one sun" illumination, shown in the Figure 2 (a). In order to understand the effect of SnO_2 on CdS film diodes, J-V characteristics of 100nm CdS film/Au diodes on 175nm/225nm/300nm SnO_2 substrate (CdS film diodes on 175nm SnO_2, CdS film diodes on 225nm SnO_2 CdS film diodes on 300nm SnO_2)were characterized, shown in Figure 2 (b) and (c) and (d) respectively.

Furthermore, effect of CdS film thickness on electron transport was investigated, and CdS films with 200nm and 400nm thickness/Au Schottky diodes on 100nm SnO_2/ITO glass substrate (200nm CdS film diodes and 400nm CdS film diodes) were measured in dark and under "one sun" illumination, shown in the Figure 3 (a) and (b) respectively.

For insight about CdS nanowire arrays, CdS nanowires with 100nm and 200nm length were configured into 100nm CdS nanowires/Au Schottky diodes on 100nm SnO_2/ITO glass substrate (100nm CdS nanowire diodes on 100nm SnO_2) and 200nm CdS nanowires/Au Schottky diodes

on 100nm SnO_2/ITO glass substrate (200nm CdS nanowire diodes on 100nm SnO_2). Their Current density (J)-voltage (V) characteristics were measured in dark and under "one sun" illumination, shown in the Figure 4 (a) and (c) respectively.

2.1 Effect of SnO_2 on Current-Voltage Characteristics of CdS film/Au Schottky Diodes

Figure 2 (a), (b) and (c) and (d) show J-V characteristics of 100nm CdS film diodes on 100nm/175nm/225nm/300nm SnO_2 substrate respectively. Figure 2 (e) shows LnJ verse V characteristics of these diodes in order to extract diode ideality factor (n) and reverse saturation current density (J_0). Extracted diode parameters of these CdS film diodes are illustrated in the Table 1.

J-V characteristics of 100nm CdS film diodes on 100nm SnO_2 demonstrate resistor-like behavior, where J is nearly linearly dependent on voltage. Analysis its J-V data yielded series resistance of $0.48\Omega/cm^2$ and $0.3\Omega/cm^2$ respectively, and shunt resistance of $0.4/cm^2$ and shunt resistance $0.2/cm^2$ in the light and dark irrespectively. The very low series and shunt resistance indicate that there are an abundant of shunt paths in 100nm CdS film deposited by CBD and these high density of shunt paths form low resistivity of resistors which are in parallel with diodes. These parallel resistors become dominated factors, forming resistor-like J-V curves.

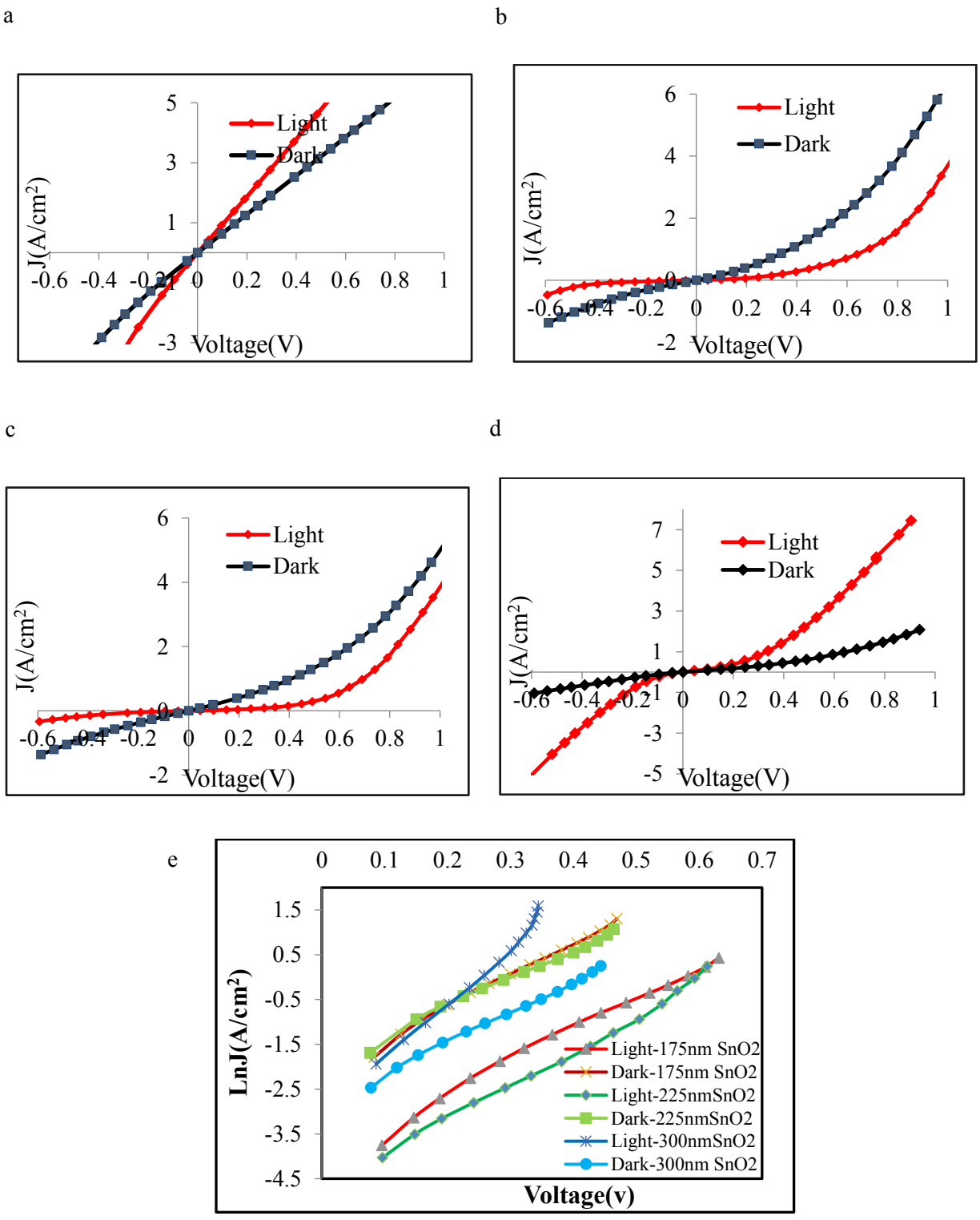

Figure 2, Current density (J) versus voltage V characteristics of 100nm CdS film/Au Schottky diodes on (a): 100nm SnO_2 substrate. (b): 175nm SnO_2 substrate. (c): 225nm SnO_2 substrate. (d): 300nm SnO_2 substrate. (e) LnJ verse V characteristics of 100nm CdS film/Au on 100nm/175nm/225nm/300nm SnO_2 substrate.

In order to solve resistor-like J-V curves, CdS film was maintained 100nm thickness but SnO_2 thickness were increased to 175nm, 225nm and 300nm. As shown in Figure 2 (b), CdS film diodes on 175nm SnO_2 thickness obviously reduce shunt issues and show rectifying diode characteristics. Current density in the light is lower than its dark value, which is thought to be due to additional light generated defects in CdS film. Analysis of J vs. V data in Figure 2 (b) demonstrated the effective reverse saturation current density (J_o), diode ideality factor (n), series and shunt resistance values of $1.1*10^{-2}$ A/cm^2, 3.1, $0.08\Omega/cm^2$ and $0.04\Omega/cm^2$ in the dark and $2.0*10^{-3}$ A/cm^2, 3.6, $0.1\Omega/cm^2$ and 2.2 Ω/cm^2 in light, as illustrated in the Table 1. However, the low J_0 and shunt resistance reveal that shunt and tunneling are the dominant processes for electron transport in these devices.

Further increasing thickness of SnO_2 to 225nm, similar diode behavior was observed. Compared with 100nm CdS film diodes on 175nm SnO_2 substrate, the diodes on 225nm SnO_2 substrate exhibited higher diode ideality factor and reverse saturation current density and similar value of series and shunt resistance, shown in the Table 1. The higher diode ideality factor and reverse saturation current density imply degraded diode performance. When thickness of SnO_2 is increase to 300nm, diode ideality factors are approximately increased by 2 times, reverse saturation current density are further increased by one order of magnitude, series resistance is obviously increased and shunt resistance is further reduced to 0.46 Ω/cm^2 and $0.12\Omega/cm^2$ in the dark and light respectively. Significantly increased diode ideality factor and reduced J_0 and shunt resistance demonstrate that diode behavior has been deteriorated. The reason is thought to be related to our hypothesis that thick SnO_2 increases resistance of the diodes and interface recombination between CdS and SnO_2 becomes more obvious with increasing SnO_2 thickness. As a result, increase of SnO_2 thickness can overcome resistor-like behavior in 100nm CdS film diodes, however high

reverse saturation current density low shunt resistance are main issues in these diodes.

2.2 Effect of CdS film thickness on Current-Voltage Characteristics of Diodes

Thickness of CdS film on J-V characteristics of the CdS film/Au Schottky diodes was investigated. Figure 3 (a) and (b) show J-V characteristics of 200nm CdS film and 400nm CdS film diodes under dark and one-sun illumination. Figure 3 (c) shows their LnJ verse V characteristics under dark and one-sun illumination to extract diode ideality factor and reverse saturation current density, which are demonstrated in the Table 1. When CdS film thickness is increased to 200nm, the J-V curves of CdS film diodes eliminate resistor-like characteristics founded in the 100nm CdS film diodes and exhibit Schottky diode behavior.

J-V data of 200nm CdS film diodes was analyzed and yielded the reverse saturation current density (J_0) and diode ideality factor (n) values of $1.2*10^{-4}$ A/cm^2 and 3.1 in the light and $5.8*10^{-4}$ A/cm^2 and 4 in the dark. Compared with 100nm CdS film diodes, 200nm CdS film diodes reduce J_0 by approximately 19 times in the dark and 16 times in the light, and maintain diode ideality factor, series and shunt resistances in the similar range. It is thought that thicker CdS film alleviates pinholes impact and reduces migration of metal from CdS film into SnO_2 and ITO, hence decreasing interface recombination and generation. Reducing interface recombination and generation lead to improvement of J_o. Measurements of shunt resistance reveal less resistance in the light than dark. It is possible that the additional light generated electron-hole pairs contribute to additional tunneling currents, resulted in lower shunt resistance in the light. It is observed that shunt resistance in the light and dark maintains low values, suggesting poor quality of CdS film.

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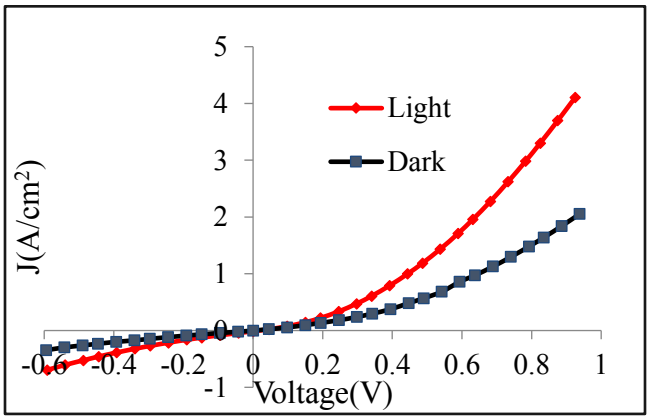

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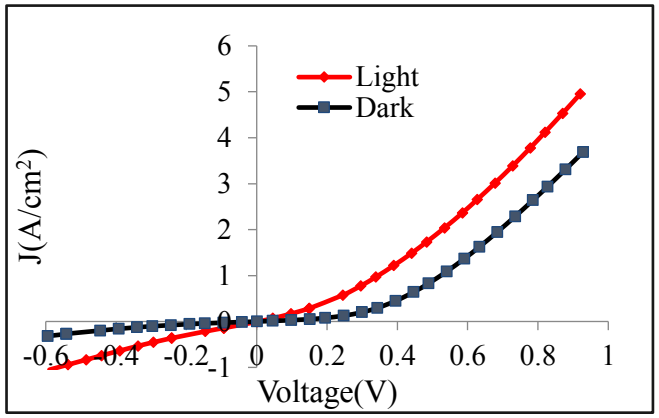

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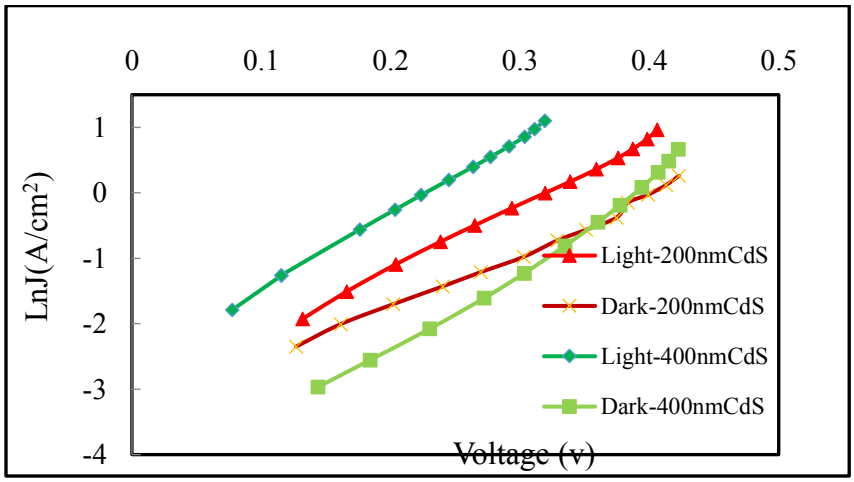

Figure 3, Dark and light current density (J) versus voltage V characteristics of (a): 200nm CdS film/Au Schottky diodes on 175nm SnO_2 substrate. (b): 400nm CdS film/Au Schottky diodes on 175nm SnO_2 substrate. (c): Dark and light LnJ verse V characteristics of these 200nm and 400nm CdS diodes.

As shown in Figure 3 (b), when CdS thickness is further increased to 400nm, the diode demonstrates similar performance as the diode with 200nm CdS film. The main difference between the diodes made from 200nm and 400nm CdS films are reverse saturation current density (J_0) and shunt resistance under illumination. When CdS thickness is increased to 400nm, the J_0 is

significantly increased from $1.2*10^{-4}$ to $3.2*10^{-2}$, increased by approximately two order of magnitude. A significant increase in J_0 value indicates non-ideal generation events become severe in the interface and depletion region. As shown in the Table 1, slightly increased shunt resistance implies that additional light generated electron-holes pairs transport through pinholes or 3D defects in the thicker CdS film to interface and ITO substrate. Thus, it can be concluded that an approach increasing CdS film thickness eliminates like-resistor behavior, however the approach presents significant challenges of its own. Low shunt resistance and relative low J_0 caused by poor quality of CdS film deteriorate diode performance.

Table 1 Extracted diode parameters of CdS nanowires/Au and CdS film/Au diodes

Diode Type	**Test Condition**	**Diode Ideality Factor (A)**	**Reverse Saturation Current Density J_o(A/cm^2)**	**Series Resistance(Ω/cm^2)**	**Shunt Resistance(Ω/cm^2)**
100nm CdS film/Au	Dark	N/A	N/A	0.48/cm^2	0.4/cm^2
	Illumination	N/A	N/A	0.3/cm^2	0.2/cm^2
100nm CdS film/Au on 175nm SnO_2	Dark	3.1	$1.1*10^{-2}$	0.08/cm^2	0.44/cm^2
	Illumination	3.6	$2*10^{-3}$	0.1/cm^2	2.2/cm^2
100nm CdS film /Au on 225nm SnO_2	Dark	6.0	$1.37*10^{-1}$	0.1/cm^2	0.44/cm^2
	Illumination	3.7	$2.3*10^{-3}$	0.09/cm^2	1.9/cm^2

100nm CdS film/Au on 300nm SnO_2	Dark	13	$3.6*10^{-1}$	$0.11/cm^2$	$0.46/cm^2$
	Illumination	12.8	$7.1*10^{-1}$	$0.07/cm^2$	$0.12/cm^2$
200nm CdS film/Au on 175nm SnO_2	Dark	4.06	$5.8*10^{-4}$	$0.24/cm^2$	$1.8/cm^2$
	Illumination	3.14	$1.2*10^{-4}$	$0.12/cm^2$	$0.88/cm^2$
400nm CdS film/Au on 175nm SnO_2	Dark	3.54	$3.1*10^{-4}$	$0.13/cm^2$	$1.9/cm^2$
	Illumination	3.17	$3.2*10^{-2}$	$0.12/cm^2$	$0.56/cm^2$
100nm CdS nanowires/Au on 100nm SnO_2	Dark	3.3	$8.0*10^{-5}$	$1.58/cm^2$	$30.8/cm^2$
	Illumination	3.1	$6.9*10^{-5}$	$1.37/cm^2$	$24.4/cm^2$
200nm CdS nanowires/Au on 100nm SnO_2	Dark	2.2	$1.2*10^{-4}$	$1.16/cm^2$	$13.4/cm^2$
	Illumination	2.6	$2.4*10^{-5}$	$0.64/cm^2$	$10.9/cm^2$

2.3 Characterization of CdS nanowires/Au Schottky Diode

CdS nanowires/Au Shottky diodes are presented to overcome these challenges. Figure 4 (a) illustrates current density J dependence on voltage V, where the junctions were formed by Au

deposited on CdS nanowires with 100nm length on 100nm SnO_2 substrate. The J-V characteristics of the junctions show rectification behavior, which indicates the formation of a Schottky diode in the 100nm CdS nanowires/Au structure. As shown in the Figure 4(a), current under illumination increased slightly over its dark value due to photoresponse which is additional electron-hole pairs generated by the light. The reverse J-V characteristics demonstrate current dependence on applied voltage bias due to barrier lowering effect. The forward J-V characteristics in Figure 4 (a) can be classified into two regions based on the applied forward bias. Above 0.6V, ln(J) dependence on voltage deviates from linearity, which is impacted by series resistance and interface between CdS nanowires/Au structure. Below 0.6V, ln(J) exhibits linear dependence on voltage, as shown in Figure 4(b). Thus, diode ideality factor n and reverse saturation current density J_o are obtained by using the slope and intercept of Figure 4(b) curve, which are tabulated in the Table 1.

The diode ideality factor n was obtained with value of 3.3 and 3.1 under dark and illumination. The value of n larger than 2 can be related with the presence of recombination current through the interface states. It is found that 100nm CdS nanowires/Au diode on 100nm SnO_2 has lower value of n comparing with 100nm CdS film/Au diode on 175 nm SnO_2 substrate. Thus inclusion of nanowires to form diode has lower recombination current through the interface states.

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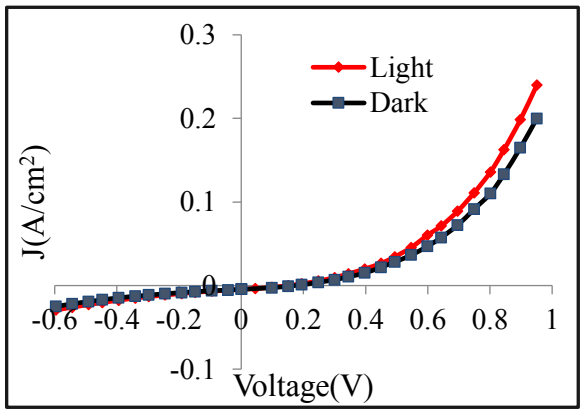

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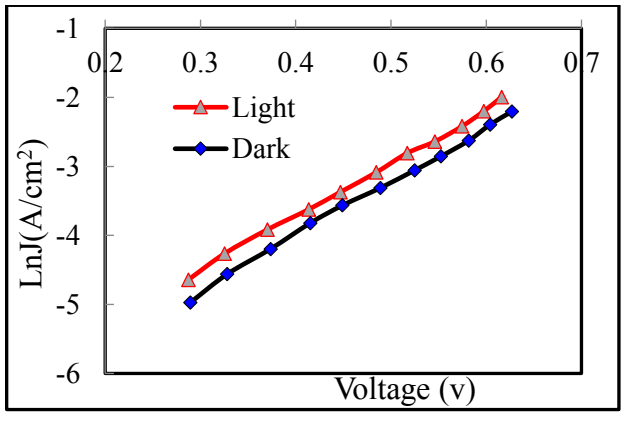

Figure 4, (a) : Current density (J) versus voltage V characteristics (b) : LnJ verse V characteristics of 100nm CdS nanowires/Au Schottky diodes on 100nm SnO_2 substrate.

It is seen that reverse saturation current density J_o gives considerably low values of $6.9*10^{-5}$ A/cm^2 and $8.0*10^{-5}$A/cm^2 in the light and the dark respectively. Compared with J_o of 100nm CdS film diodes, J_o of 100nm nanowire diodes is significantly reduced by three orders of magnitude in the dark and two orders of magnitude in the light. According to equation 1 (a) and (b), J_o is dependent on Richardson constant, temperature and barrier height. Due to same materials used for CdS film and CdS nanowires and all of the measurements at room temperature, equation 1(a) gives same value of J_o for CdS film and nanowire diodes when electron thermionic emission current dominates.

$$J = J_0[\exp(\frac{q(V-JR_S)}{nkT} - 1] \qquad \text{Equation 1(a)}$$

$$J_0 = A^*T^2e^{-\emptyset_B/KT} \qquad \text{Equation 1(b)}$$

where A* is the effective Richardson constant and Φ_B is barrier height.

It is highly possible that transport mechanism in these diodes is not purely thermionic emission. The possible phenomenon that explains the enormous difference of J_o between CdS film and nanowire diodes includes tunneling current and recombination current by traps. Tunneling through pinholes of CdS film to SnO_2/ITO substrate and defect recombination in CdS films become dominated current transport mechanism. CdS nanowires have significantly low defect features and uniformly and densely distribution. Very low J_o in CdS nanowire diodes indicates that tunneling current and recombination by trap are strongly suppressed due to low defect feature of nanowires.

It is found (table 1) that series resistance and shunt resistance of CdS nanowire diodes are 1.37 Ω/cm^2 and 24.4 Ω/cm^2 under illumination and corresponding values are 1.58 Ω/cm^2 and 30.8

Ω/cm^2 in the dark. Shunt resistance of CdS nanowire diode is significantly enhanced by 70 times when comparing with shunt resistance of 100nm CdS film diode. This widely difference of shunt resistance could be related with the fact that CdS nanowires considerably reduces shunt paths and hence improve diode properties, contributing to high shunt resistance.

Table 1 also lists that CdS nanowire diode has higher series resistance than that of CdS film diodes. It is possible that large shunt current flows through shunt paths in CdS film, leading to obvious increase in total current and impact and lower extracted value of series resistance for CdS film diodes. However such phenomenon is avoided in CdS nanowire diodes. The extracted high series resistance of CdS nanowire diodes may be attributed to the contact resistance between Au and AAO matrix. As a result, CdS nanowires significantly improves the diode properties without need to increase thickness of SnO_2.

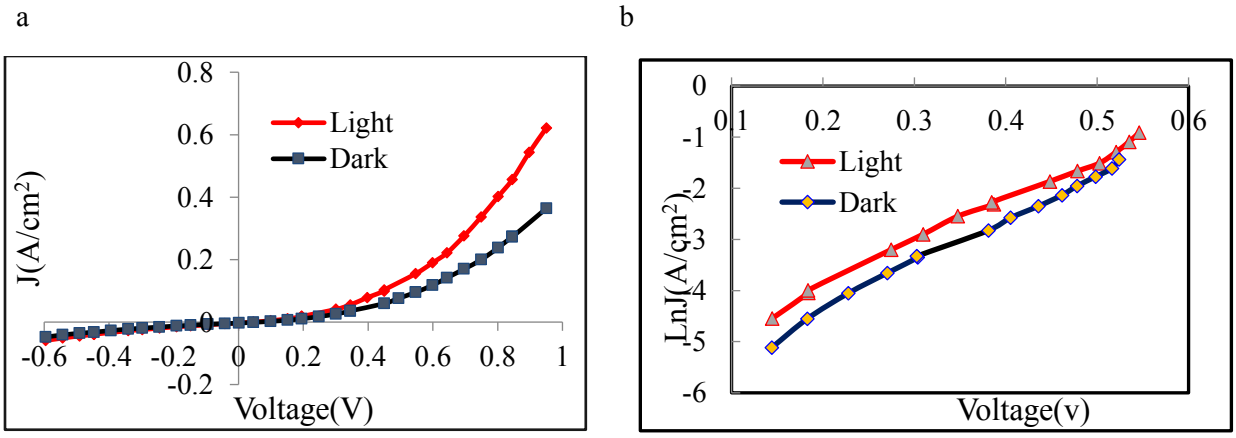

Figure 5, (a): Current density (J) versus voltage V characteristics (b): LnJ verse V characteristics of 200nm CdS nanowires/Au Schottky diodes on 100nm SnO_2 substrate.

CdS nanowires with 200nm length is configured into a Shottky diode to investigate effect of nanowire length on diode properties. Figure 5 (a) and (b) show J-V and extracted ln(J)-V curves of 200nm CdS nanowires/Au diode on 100nm SnO_2 substrate. Observed from Figure 4(a) and 5(a), nanowires with longer length shows higher current density and current density under illumination

and in the dark demonstrates larger difference than that of 100nm nanowire diodes. It can be assumed that more electron-hole pairs are generated due to longer length of nanowires under illumination. The difference between 100nm CdS nanowire and 200nm nanowire diodes is the diode ideality factor, series and shunt resistance. The diode with longer length nanowires reduce diode ideality factor to 2.2 and 2.6 in the dark and illumination, suggesting that longer nanowires may be related with reduced interface states of junctions. Extracted series resistance is decreased and extracted shunt resistance is simultaneously enhanced, which may be caused by spatial inhomogeneities at the longer CdS nanowires and Au interface. As a consequence, the diodes configured by CdS nanowires with 100nm length demonstrate the optimal diode behavior and properties without need to increase length of nanowires and SnO_2 thickness.

2.4 Simulation of CdS nanowire and film Schottky Diode

In order to understand carrier transport mechanisms which impact difference between the nanowire and film diode behaviors, simulation of J-V characteristics of CdS nanowire and film diodes in the light and dark were performed by SCAPS software [1]. By fitting simulated J-V with measured J-V, numerical models of CdS nanowire and film diodes were established.

Simulation of CdS nanowires/Au Diode

Table 2 show parameters to simulate the measured J-V curves of the 100nm nanowire CdS/Au diodes. In this simulation, thickness of CdS nanowires is 100nm, and energy band gap is 3.5eV and measured nanowire CdS absorption data was used to simulate CdS absorption spectrum. Simulation found that shallow donor (doping) concentration of CdS nanowires affects diode properties and mainly impacts diode current. Increase in shallow donor concentration considerably increases current at applied bias. Acceptor traps compensate free carrier density and space charge

in CdS nanowires. Simulation demonstrates that due to its large energy bandgap, the acceptor traps in the CdS nanowires have non-significant influence on diode J-V characteristics. It is found that interface states are a key parameter which impact diode properties. It is acceptor type interface states rather than donor type interface states that play a role on diode behavior. Reducing acceptor interface states is found to improve reverse saturation current. Series resistance and shunt resistance are included into the simulation model, demonstrating strong influence on diode J-V curves, mainly on J-V curves under the reverse bias and the high forward bias.

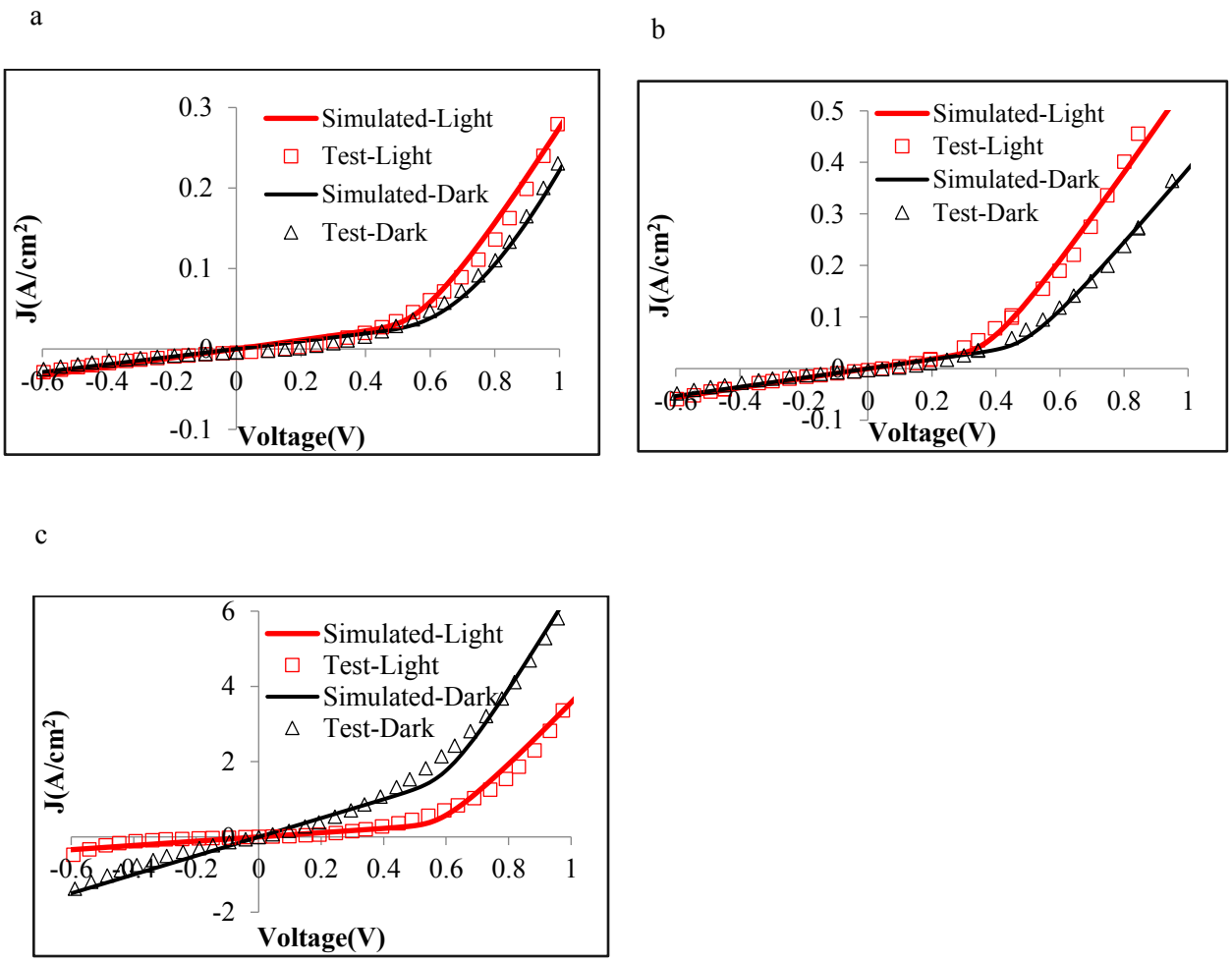

Figure 6, Light and dark simulated and measured current density (J) versus voltage (V) characteristics curves of (a): 100nm CdS nanowires/Au diode on 100nm SnO_2 substrate (b): 200nm CdS nanowires/Au diode on 100nm SnO_2 substrate. (c): 100nm CdS film/Au diode on 175 nm SnO_2 substrate

In order to fit the J-V curve of 100nm CdS nanowire diodes in the dark, shallow donor concentration of CdS nanowires was adjusted to $6.0*10^{16}$ /cm^3 and compensating acceptor type traps are located in the middle gap (1.75eV) of CdS nanowires and are introduced with density of $5.5*10^{15}$/cm^3. To realize a better correspondence between the simulated and measured curves, acceptor interface trap density was tuned to $5.0*10^{9}$/cm^2 where the acceptor interface traps are uniform distribution, located in the 1.5eV above valence band E_V. Low interface state density indicates interface recombination current isn't a dominated current transport mechanism in the nanowire diodes. Corresponding light J-V curve was simulated including slightly increased shallow donor concentration and slightly decreased acceptor type traps in CdS nanowires, which conform to data analysis above. In the simulation model, interface states and series and shunt resistances demonstrated similar values for simulated dark and light curves, suggesting that light has approximately negligible impact on interface recombination and shunt current.

Figure 6 (a) shows the simulated and measured J-V curves of 100nm CdS nanowire diodes in the dark and the light. In the figure, dotted lines is measured curves and solid lines are simulated curves. As shown in the Figure 6(a), simulated JV curve fits well with measured J-V curve. When voltage is less than 0.2V, simulated J-V curve slightly deviates from measured J-V curve. In the simulation model, a linear distribution of accept traps in the middle gap was assumed. However, these traps may not be linear distribution in the CdS nanowires. There is a slight difference when supply voltage is larger than 0.7V in the light curve. It is caused by series resistance. The nanowire diode samples have higher series resistance which is accord with data analysis above.

200nm nanowire CdS diodes were simulated and simulated J-V curves and parameters are shown in Figure 6 (b) and table 2 respectively. Shallow donor (doping) concentration of CdS nanowires was increased to $4.0*10^{17}$/cm^3 (dark) and $6.0*10^{17}$/cm^3 (light) in order to fit current

increase observed in the 200nm nanowire CdS diodes. The simulation model found that there are no obviously change of acceptor trap concentration. It can be deduced that nanowire length may have slight impact on defect recombination. Interface density between CdS nanowire/SnO_2 is increased and shunt resistance is obviously reduced in the model, which agree with experimental analysis above. Simulation shows that junction formation may be more challenging in longer nanowires.

Table 2: Simulated parameters used in CdS diodes

Diode	**Test Condition**	**Layer**	**Shallow Donor Doping Density**	**Trap Type and Trap Level**	**Trap Density**	**Series Resistance($\Omega.cm^2$)**	**Shunt Resistance ($\Omega.cm^2$)**
100nm CdS nanowires/ Au Diode on 100nm SnO_2	Light	CdS Nanowires	$7.0*10^{16}/cm^3$	Acceptor Middle Gap E_i =1.75eV	$4.5*10^{15}/cm^3$	$2.7*10^{-3}$	$5.0*10^{-2}$
		Interface between CdS and SnO_2		Acceptor Above E_v +1.5eV	$5.0*10^{9}/cm^2$		
	Dark	CdS Nanowires	$6.0*10^{16}/cm^3$	Acceptor Middle Gap E_i =1.75eV	$5.5*10^{15}/cm^3$	$2.8*10^{-3}$	$5.5*10^{-2}$
		Interface between CdS and SnO_2		Acceptor Above E_v +1.5eV	$5.0*10^{9}/cm^2$		
200nm CdS nanowires/ Au Diode on 100nm SnO_2	Light	CdS Nanowires	$6.0*10^{17}/cm^3$	Acceptor Middle Gap E_i =1.75eV	$5.0*10^{15}/cm^3$	$3.2*10^{-3}$	$3*10^{-2}$
		Interface between CdS and SnO_2		Acceptor Above E_v +1.5eV	$5.5*10^{9}/cm^3$		
	Dark	CdS Nanowires	$4.0*10^{17}/cm^3$	Acceptor Middle Gap E_i =1.75eV	$6.0*10^{15}/cm^3$	$3.9*10^{-3}$	$3*10^{-2}$
		Interface between CdS and SnO_2		Acceptor Above E_v +1.5eV	$5.5*10^{9}/cm^3$		
100nm CdS film/Au Diode on	Light	CdS film	$6.0*10^{19}/cm^3$	Acceptor Middle Gap E_i =1.2eV	$1.0*10^{18}/cm^3$	$3.0*10^{-4}$	$5.0*10^{-3}$

175nm SnO_2				Neutral 0.6eV above Ev	$1.0*10^{18}/cm^3$		
		Interface between CdS and SnO_2		Acceptor Above E_v +1.2eV	$6.0*10^{11}/cm^3$		
	Dark	CdS film	$4.0*10^{19}/cm^3$	Acceptor Middle Gap E_i =1.2eV	$5.0*10^{18}/cm^3$	$2.0*10^{-4}$	$1.0*10^{-3}$
				Neutral 0.6eV above E_v	$1.0*10^{19}/cm^3$		
		Interface between CdS and SnO_2		Acceptor Above E_v +1.2eV	$8.0*10^{11}/cm^3$		

2.5 Simulation of CdS film/Au Diodes

Simulation was conducted on 100nm CdS film/Au diodes on 175nm SnO_2 substrate to understand difference between nanowire and film diodes. Figure 5(c) shows the simulated and measured J-V curves of 100nm CdS nanowire diode in the dark and the light. In the simulation, energy band gap of CdS film is 2.4eV, and shallow donor concentration of $4.0*10^{19}/cm^3$ and $6.0*10^{19}/cm^3$ are introduced in CdS film layer to fit I-V curves in the dark and light respectively. Compared with the nanowire diodes, significantly increased donor concentration accounts for higher current density in the CdS film diodes. Acceptor traps in CdS film are increased to $1.0*10^{18}/cm^3$, which reveals that deep-level defect recombination is obviously enhanced in the CdS film diodes. Another neutral type defects are added into the model and they are located in 0.6eV above valence band of CdS film and have liner concentration of $1.0*10^{18}/cm^3$. Furthermore, simulation shows that interface state density is increased to $8.0*10^{11}/cm^2$, significantly increased by two order of magnitude and shunt resistance is reduced by one order of magnitude. The simulation agrees that a great amount of interface states exist between CdS film and SnO_2 and higher concentration of shunt paths occur in CdS films than CdS nanowires.

As shown in Figure 6 (c), simulated J-V curves fit with measured J-V curves and slight

difference between simulated and measure curves occur at the bias of 0.5-0.7 V. It is possible that other traps exist in the CdS film. Simulation model indicates that deep-level combination, interface recombination and shun paths that combine together to impact J-V characteristics of CdS film diodes. It is considered the CdS layer has small energy bandgap like 2.4eV and form poor quality film, hence acceptor traps and defects in the CdS layer significantly reduce diode properties. However, high energy bandgap of CdS nanowires and nanowire features lead to reduced interface and defect recombination and tunneling, contributing to improved diode behavior.

3. Conclusion:

CdS nanowires are fabricated by AAO assisted deposition method and configured to form diode structure. Electronic characterization and simulation are conducted to investigate transport mechanism and diode properties of CdS nanowire/Au diodes and film/Au diodes as comparison. 100nm CdS film/ Au on 100nm SnO_2 substrate demonstrates like-resistor characteristics and indicate that shunt transport dominates current transport mechanism. Effect of SnO_2 on J-V Characteristics of CdS film/Au diode properties is studied and increase in SnO_2 thickness corrects resistor behavior and shows rectification behavior. However, the effective reverse saturation current density and shunt resistance are significantly high and low respectively, implying that interface/defect recombination and shunt issues are main current transport mechanism. Furthermore, thickness of CdS film on J-V characteristics of the diodes is investigated. Increasing CdS film thickness to 200nm improved the reverse saturation current density (J_0) by one order of magnitude and however shunt resistance is low and maintain similar values with increasing SnO_2 method, suggesting poor quality and intrinsic issues of CdS film. 100nm CdS nanowire/Au diodes reduce reverse saturation current density J_o by three orders of magnitude in the dark and two orders of magnitude in the light respectively and their shunt resistance is significantly enhanced by 70

times times when comparing with those of the CdS film diodes. This widely difference of shunt resistance can be attributed to the fact that CdS nanowires considerably reduces shunt paths, contributing to high shunt resistance. However, CdS nanowire diodes have higher series resistance, it may be attributed to reduced shunt recombination currents and the contact resistance between Au and AAO matrix.

SCAPS simulation was conducted to stablish defect impact on these diode properties. The simulation models fit well with measured J-V of these diodes. In the simulation model of 100nm CdS nanowire diodes, shallow donor concentration is adjusted to $6.0*10^{16}$ /cm^3, and compensating acceptor type traps with a liner distribution of $5.5*10^{15}$/cm^3 was introduced in CdS nanowires. It is acceptor type interface states that impact diode properties and interface state density is tuned to $5.0*10^{9}$/cm^2. Low interface state density indicates that interface recombination current isn't a dominated current transport mechanism in the 100nm nanowire diodes. Compared with simulated 100nm nanowire diodes, shallow donor concentration is are slightly increased and there are no obviously change of interface density and acceptor trap concentration in 200nm CdS nanowires. Simulation is conducted for CdS film diodes and compared with the nanowire diodes, significantly increased donor concentration accounts for higher current density in the CdS film diodes. Acceptor traps are significantly increased by two order of magnitude, and another neutral type defects which are located in 0.6eV above valence band and have liner concentration of $1.0*10^{18}$/cm^3 are added into the model, revealing that deep-level defect recombination becomes dominated. The interface state density is significantly increased by two order of magnitude and shunt resistance is reduced by one order of magnitude, indicating that a great amount of interface states exist between CdS film and SnO_2 and high concentration of shunt paths occur in CdS film. Simulation model indicates that deep-level combination, interface recombination and shun paths that combine together to

negatively impact J-V characteristics of CdS film diodes. The high energy bandgap and nanowire features of CdS nanowires significantly reduce interface states, defect recombination and tunneling, contributing to improved diode properties.

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