Defect Characterization and Testing of Skyrmion-Based Logic Circuits

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***Abstract*—Magnetic skyrmion is an emerging digital technology that provides ultra-high integration density and requires ultra-low energy. Skyrmion is a magnetic pattern behaving like a stable pseudoparticle, created by a transverse current injection in ferromagnetic thin film. The state of a logic signal is represented by the presence (logic-1) or absence (logic-0) of a single skyrmion. Patterns on ferromagnetic and metal films form interconnects, called nanotracks, through which electric currents move skyrmions. Because skyrmion-based logic gates (e.g., AND, OR, inverter, and fanout) operate through skyrmion-to-skyrmion interaction, their logic circuit implementation and manufacturing defects differ from those of CMOS circuits. We examine breaks and bridges in nanotrack interconnects, and 19 technology-specific defects in skyrmion gate structures. Simulator $MuMax^3$ is used to exhaustively simulate all circuit elements. The results help map each defect onto a fault, modeled in an equivalent logic circuit. A break in a nanotrack interconnect maps onto a single stuck-at fault. Experiments on benchmark circuits demonstrate that tests for all nanotrack breaks can be found using the available ATPG and simulation tools. Others are classified as technology-specific defects. For example, a bridge between two nanotracks results in simultaneous AND and OR functions on respective nanotracks. A variety of technology-dependent faults are identified for future research.**

***Index Terms*—Skyrmion, magnetic logic, fault model, technology-specific defect, stuck-at fault, bridging fault.**

I. Introduction

Spintronic devices offer a feasible choice for post-Moore devices [1], [2]. Magnetic skyrmion is a possible choice for implementing various logic designs and non-volatile memories [3], [4]. It has been experimentally demonstrated that skyrmions can be stabilized in various material systems, including noncentrosymmetric chiral-lattice magnets such as MnSi/MnGe and $Fe_{0.5}Co_{0.5}Si$ [5], [6] as well as at heavy metal/perpendicular magnet interfaces with strong Dzyaloshinskii–Moriya interaction (DMI) [7], [8]. They can also be created, moved and annihilated by magnetic fields and low electrical current pulses [9]. Though the non-linear motion caused by skyrmion Hall effect poses an issue with skyrmions, their properties such as nanometer diameter for high-density storage, room-temperature stability, current-controlled motion, topological charge, and protection against large defects have made skyrmion-based devices promising candidates for beyond-Moore systems [10], [11].

Skyrmion logic gates utilize effects of skyrmion movement to implement such functions as spin-orbit torque-induced motion [12], [13], skyrmion Hall effect [14]–[18], skyrmion-edge repulsion [19], [20], and voltage control of magnetic anisotropy [21]–[23]. Skyrmion-based gates are also known to implement reversible computing [24].

Due to minimal power consumption and small physical size, a spin-based device like magnetic skyrmion is a promising candidate for a beyond CMOS technology. We believe a significant amount of work is still necessary to make these devices feasible for commercial applications. To the best of our knowledge, little is available on their testing [25]. In manufacturing, a wide variety of defects may occur, and finding tests for them is often impractical. Thus, modeled faults serve as the basis for tests, and their coverage measures the effectiveness of tests in detecting the manufacturing defects. Main contributions of this paper are as follows:

- *Defect characterization:* As technology-specific defects, we examine breaks, extra material, etching blemishes, bridges among interconnects, and a set of 19 physical defects in the skyrmion gate structures. *We believe we are the first to characterize such defects using magnetic simulation.*
- *Developing fault models:* Each defect is simulated for an exhaustive set of signals to map it onto an analyzable fault model using the principle of fault equivalence [26]. Thus, each defect is represented by either a technology-independent single stuck-at fault or a technology-dependent fault.
- *Testing of skyrmion-based circuits:* Single stuck-at, transition and certain bridge faults are directly analyzable by the available tools. Others are, as far as possible, represented by combinations of analyzable faults. This paper gives test generation results for skyrmion versions of benchmark circuits for defects that could be represented as single stuck-at faults. Our ongoing future research will address other faults, shown to require complex representations.

The approach outlined above can be extended to other emerging circuit technologies (e.g., memristors [27]). This paper is organized as follows. The background of skyrmion-based designs is provided in Section II. We characterize physical defects, likely to appear during the manufacturing process, in Section III using magnetic simulation. We present fault models for skyrmion circuits in Section IV. In Section V, we develop the testing strategy for detecting manufacturing defects, with some results given in Section VI. Finally, we conclude the paper in Section VII.

II. Background

In this section, we will study the movement of skyrmion in a nanotrack and simulate basic logic gates.

A. Skyrmion Motion in Nanotrack

Skyrmion is a stable magnetic field that acts like a pseudoparticle. It moves through a structure called *nanotrack*, which is made of a heavy metal (HM) layer and a ferromagnetic (FM) layer [24]. Figure 1 shows the 3D cross sectional view of a nanotrack consisting of a FM layer (gray) and a HM layer (green). The HM layer is wrapped around by the FM layer at the top and two sides. The skyrmion can be hosted at the FM/HM

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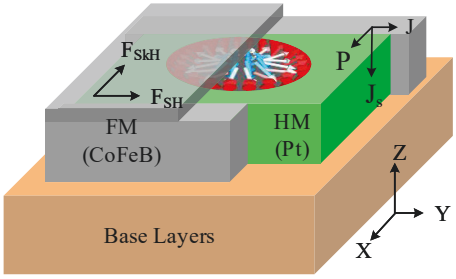

Figure 1: Nanotrack structure for skyrmion movement.

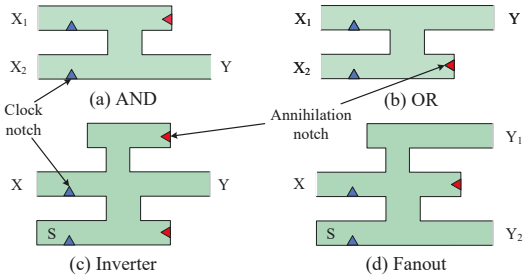

Figure 2: Structure of skyrmion gates. (a) AND gate (b) OR gate (c) Inverter, and (d) Fanout.

interface due to the strong interfacial DMI [7], [8]. Simulation shows that the side wall wrapping eliminates transverse motion of the skyrmion caused by the Hall effect, allowing only linear motion. The dimensions of the FM and HM layers can be controlled based on the device geometry. The HM layer consists of platinum (*Pt*), and the FM layer consists of *CoFeB*.

To drive a skyrmion in the nanotrack, a continuous electric current J is required in the HM layer. Due to spin Hall effect, J generates a spin current J_s in the FM layer. At the FM/HM interface, the spin current applies a spin-orbit torque to the skyrmion, driving it along y-axis. At the same time, Hall effect tends to move the skyrmion transversely along x-axis. However, the transverse motion is prevented by the HM side wall.

The dynamics of skyrmion is governed by the Landau–Lifshitz–Gilbert–Slonczewski equation [28]:

$$\frac{dm}{dt} = -|\gamma|\, m \times H_{eff} + \alpha \left(m \times \frac{d_m}{d_t} \right) + \tau_{SOT} \qquad (1)$$

where m is the normalized magnetization M/M_s, M being magnetization and M_s the saturation magnetization. H_{eff} is the effective magnetic field associated with magnetocrystalline anisotropic energy and the DMI energy [7], [8]. Further, γ is gyromagnetic ratio, α is damping coefficient, and τ_{SOT} represents the spin-orbit torque determined by multiple parts, namely, gyromagnetic ratio, effective field, spin polarization rate, permeability of vacuum, driving current density and thickness of magnetic film.

The skyrmion inside nanotrack is driven by a current flowing in the heavy metal (HM) layer via spin orbit torque (SOT). The forces on the micromagnetic skyrmion can be modeled by Thiele equation [29]:

$$G \times v - \alpha D \cdot v + F_{SOT} - \nabla V = 0 \qquad (2)$$

where the first term describes the Magnus force, G is the gyromagnetic coupling vector, and v is velocity of the skyrmion. The second term represents a dissipative force, α is the damping coefficient, and D is the dissipative tensor. The third term represents the driving force F_{SOT} generated by the spin Hall effect. The last term gives the resultant force acting on the skyrmion, and V is the confining potential due to boundaries, process impurities and other textures.

B. Micromagnetic Simulation Platform

The micromagnetic simulation tool $MuMax^3$ is a GPU-accelerated program that analyzes the dynamic behavior of skyrmions [30]. Skyrmion movement in the track is modeled based on equation 2 as the electrical current in the HM layer drives the skyrmion. Parameters used in simulation are: Gilbert damping factor α = 0.3, nonadiabatic STT factor $\beta = 0.1$, exchange stiffness $A_{ex} = 15 \times 10^{-12}$ J/M, perpendicular magnetic anisotropy $K_u = 0.6$ MJ/m^3, saturation magnetization $M_s = 5.8 \times 10^5$ A/m, and DMI constant = 3.5 mJ/m^2. Mesh sizes are $1nm \times 1nm \times 0.4nm$, along x, y and z axes. The parameters here are typical values for the magnetic layers [31].

C. Skyrmion Logic Gates

A traditional skyrmion gate combines phenomena such as spin Hall effect, skyrmion Hall effect, skyrmion-skyrmion repulsion and skyrmion curb repulsion [20], [32]. We have adopted the reversible gates of Friedman and coworkers [24] by modifying them as non-reversible logic gates. We simulated the basic two-input AND and OR gates, and an inverter. In addition, in this technology a specific fanout element is needed. Figure 2 shows the gates and fanout. For simplicity, we only show the top view of the nanotracks with the bottom HM layer and top FM layer to illustrate the design of gates. Other gates including complex gates can be similarly constructed.

Figure 2(a) is an AND gate consisting of two nanotracks with a junction. This makes the gate a transversely H-shape structure. The blue triangle on the inputs side is a clock notch to synchronize the input skyrmions so that the output of the gate is properly evaluated based on skyrmion-skyrmion interaction. The clock notch has the same material like the ferromagnetic layer. One can also implement voltage controlled magnetic anisotropy (VCMA) structure to synchronize the skyrmion [33]. The clock notch can hold/block the skyrmion movement when a standard current is applied. When a high current pulse is applied, the skyrmions can simultaneously cross the notchs, ensuring proper logic operation of the gate. The red triangle at the end of the upper nanotrack is an annihilation notch, which eliminates any arriving skyrmion. The three forces mentioned above, two of which shown in Figure 1, are responsible for the operation of the gate: (1) Spin-Hall force F_{SH} moves skyrmion along the nanotrack toward output (shown on the right in our diagrams); (2) Skyrmion-Hall force F_{SkH} moves skyrmion from one to other nanotrack whenever a junction becomes available; and (3) Skyrmion-skyrmion repulsion prevents the movement when another skyrmion is present in the other nanotrack.

For OR gate we swap the output (Y) and the annihilation (X_1) tracks of the AND gate as shown in Figure 2(b). Figure 2(c) gives the structure of an inverter. We need to add a source S, where a skyrmion is injected every clock cycle. Our source (S) is the same as the control $(C = 1)$ used by others [24]. The inverter can be regarded as an OR gate with an annihilation track added through a junction. For $X = 1$, skyrmion from X prevents the upward movement of the skyrmion from S, which is

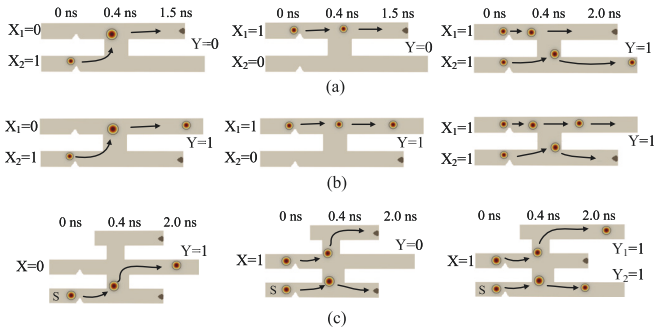

Figure 3: Simulation of skyrmion gates: (a) AND, (b) OR, and (c) Inverter and fanout.

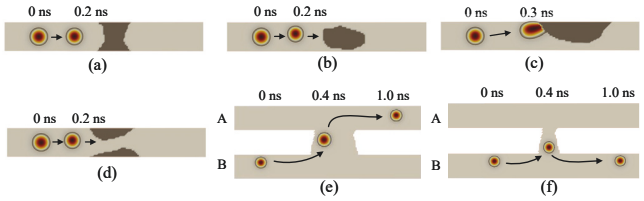

Figure 4: Simulation of interconnect defects: (a) break, (b) void, (c) and (d) etching blemishes, (e) wide bridge, and (f) narrow bridge. Defects (a) through (d) map onto stuck-at faults, (e) causes a bridging fault, and (f) causes no fault.

then annihilated. Meanwhile, the skyrmion from X goes up and is annihilated as well, leaving the output Y with no skyrmion, i.e., at logic 0. If $X = 0$, there will be no skyrmion from X to prevent that from S from moving up and appearing at Y.

The inverter is modified as a fanout gate in Figure 2(d). Since the source S is always 1, the two nanotracks Y_1 and Y_2 will output 1 only when there is a skyrmion at input X. Otherwise, the skyrmion from S will move to the middle track and get annihilated, leaving no skyrmion in the two output nanotracks.

Figure 3(a) shows the simulation of AND gate with various input combinations. Before clock pulse arrives, the skyrmions are held at the clock notch. After the clock arrival, the skyrmions cross the notches and keep moving in respective nanotracks. For inputs $X_1 = 0$ and $X_2 = 1$ the lower skyrmion will travel up through the junction under skyrmion Hall effect and will be annihilated. "Upper" and "lower" here refer to the left and right nanotracks when viewing in the direction of skyrmion motion. When X_1 = 1 and X_2 = 0, the skyrmion in the upper nanotrack will be directly annihilated. When the input pattern is 11, skyrmions will meet in the middle of the junction but skyrmion-skyrmion repulsion will keep them in their original tracks, sending the upper one to annihilation and the lower one to the output Y. Not shown is the simulation of input 00, which has no skyrmion and hence no action occurs, leaving $Y = 0$.

Figure 3(b) shows the simulation of OR gate. Figure 3(c) shows the simulation of inverter and fanout gates.

III. Defect Characterization

This section explores the testability aspects of skyrmion circuits with physical defects using $MuMax^3$ tool [30].

A. Interconnect Faults

Similar to other technologies (e.g., CMOS), these defects are not associated with gate implementations. However, the skyrmion interconnects are nanotracks and not simple wires. Also, logic 1 or 0 state is represented by presence or absence of a single skyrmion and not by high or low voltage. Not considering any influence of these two attributes, the interconnect defects can be regarded as technology-independent.

The interconnect defects include material void, crack in a nanotrack, and bridging between the two nanotracks. Figures 4(a)-(f) show snapshots of the skyrmion movement at three different simulation times. A break in the nanotrack is shown in Figure 4(a) such that the skyrmion cannot move along the nanotrack. A hollow structure/void appears on nanotrack and is shown in Figure 4(b). Although the FM or HM layers are not completely disconnected, the skyrmion still cannot propagate through the void. However, the effect of a void defect will be different depending on the speed of skyrmion. When the speed is low, the skyrmion will stop before the void defect. When the skyrmion is moving at a high speed, it will collide with the void and vanish. As shown in Figures 4(c) and (d), there are etching blemishes on one or both surfaces of the nanotrack, respectively. The uneven surface will block the propagation and destroy the skyrmion. Thus, all of these defects can potentially cause stuck-at-0 faults. We have not found any defect that could permanently trap a skyrmion in an interconnect to cause a stuck-at-1 fault.

Another possible defect is a bridge between two nanotracks, possibly where nanotracks are physically close to each other. As skyrmions move in one direction, which is along the electric field, it is unlikely that a feedback bridging will occur. Figures 4(e) and 4(f) show two types of bridging defects. When the bridge is wide, the skyrmion will cross over to the upper nanotrack as shown in Figure 4(e). However, a narrow bridge will not affect the skyrmion movement and will not produce incorrect response as shown in Figure 4(f). Interconnect response for wide bridge is, as Table I shows, logical OR, i.e., A+B, for interconnect A and logical AND, i.e., AB, for interconnect B. This differs from the conventional OR-bridging or AND-bridging faults [26]. We classify the interconnect bridge in a skyrmion circuit as technology-specific because the circuit layout must determine which interconnect will be OR and which will be AND.

Table I: Wide interconnect bridge of Figure 4(e).

Correct inputs and outputs		Faulty outputs	
A	B	A	B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

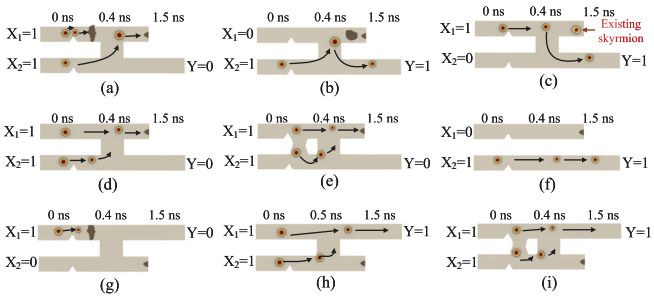

Figure 5: Some technology-specific defects in skyrmion gates. AND gate - (a) through (f), OR gate - (g), (h) and (i).

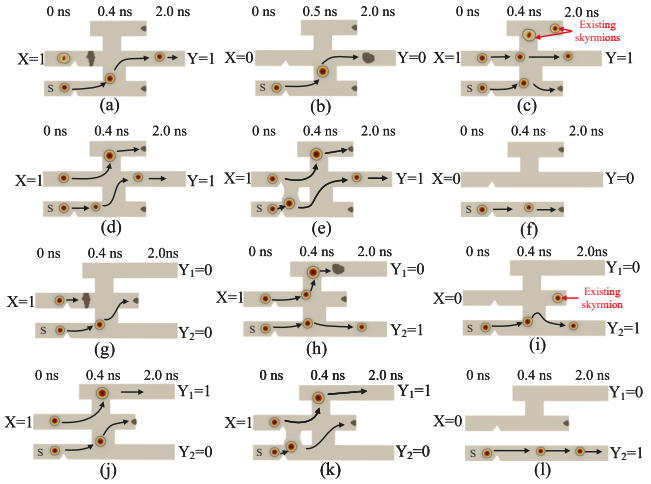

Figure 6: Technology-specific defects in skyrmion inverter and fanout gates.

B. Technology-Specific Defects in Gates

The defects inside a gate are technology-specific because their bahavior depends upon the device characteristics and gate structure. We present a comprehensive taxonomy of defects in two-input functions, $Y = X_1X_2$ and $Y = X_1 + X_2$, inverter, $Y = \overline{X}$, and fanout $(Y_1, Y_2) = X$, described below as T_1 through T_{19}. These were analyzed as single defects by a technology simulator [30] and the faulty outputs for exhaustive set of inputs are recorded in Table II:

- $\boldsymbol{T_1 - T_5}$: Breaks at different locations in nanotrack effect the gate function differently. For example, if the break is located before the junction (Figure 5(a) for AND gate or Figure 5(g) for OR gate), repulsion from the break will change the original trajectory of the skyrmion. This repulsion may either stall a slow moving skyrmion or destroy a fast moving skyrmion. Defects T1 through T4 are breaks at X_1, X_2, Y, or the dummy channel (with annihilation notch) in AND or OR gate. For an inverter or fanout having an additional nanotrack, only the T5 of Figures 6(a) and 6(g) are considered.
- $\boldsymbol{T_6 - T_{10}}$: A void may appear at different locations in the nanotrack. Unlike T_1 through T_5, a void can sometimes change the trajectory of skyrmion due to the skyrmion-edge repulsion. Defects T_6, T_7 and T_8 are voids in tracks X_1, X_2 and Y, respectively. T_9 in Figure 5(b) corresponds to a void in the dummy track. For inverter and fanout gates, defects T_6 through T_{10} represent voids in nanotracks X, S, Y, Y_1 and Y_2 shown in Figures 6(b) through 6(h), respectively.
- $\boldsymbol{T_{11} - T_{13}}$: The annihilation notch of a gate can be absent due to T_{11}. The skyrmion in the previous computation will not vanish as expected and the skyrmion-skyrmion repulsion due to that skyrmion will alter the original trajectory of the skyrmion, as shown in Figure 5(c). T_{11} and T_{12} are missing notches of nanotracks Y_1 and Y_2 in Figure 6(c). T_{13} is the missing notch of fanout gate in Figure 6(i).
- $\boldsymbol{T_{14} - T_{15}}$: These are missing clock notches, or the defects where the clock is absent at input tracks X_1 and X_2, respectively. Due to these defects, skyrmions enter logic gate at different times and the synchronization mismatch can cause logic malfunction. Figures 5(d) and 5(h) and Figures 6(d) and 6(j) show T_{14} defects in four types of gates, respectively.
- $\boldsymbol{T_{16}}$: T_{16} is a bridging defect between two input tracks of a gate, after the clock notch. This will cause the skyrmion to either change speed or directly pass through the bridge, thereby affecting the function of the gate. Figures 5(e) and 5(i) show T_{16} for AND and OR gates, and Figures 6(e) and 6(k) show T_{16} for an Inverter and fanout, respectively.
- $\boldsymbol{T_{17} - T_{18}}$: There can be breaks in the nanotrack that links the two input nanotracks. It might be missing as well. The two possible defects are denoted as T_{17} and T_{18}, respectively. Figure 5(f) shows T_{17} for an AND gate. Figures 6(f) and 6(l) show breaks between middle and lower tracks of inverter and fanout gate. T_{18} is a missing bridge in the upper track of the inverter and fanout gates.
- $\boldsymbol{T_{19}}$: This is a missing skyrmion sourse S, which is supposed to produce a skyrmion every clock. T_{19} will cause the inverter and fanout to function incorrectly.

Figure 5 shows the magnetic simulation using $MuMax^3$ tool [30] for technology dependent defects in AND and OR gates. We apply an input pattern so that a faulty response can be observed at the output. Figure 5(a) shows a break in the nanotrack of input X_1 of an AND gate. The skyrmion at X_2 moves to the upper track and causes a faulty response, i.e., $Y = 0$. Figure 5(b) shows a void defect located at the upper nanotrack of AND gate. When the input pattern $X_1X_2 = 01$ is applied, the skyrmion at X_2 is repulsed from the void and produces a faulty response $Y = 1$. As shown in Figure 5(c), a missing annihilation notch will cause redundant skyrmion, which was supposed to have been eliminated. The repulsion from the extra skyrmion will cause the new skyrmion to change the original trajectory and the skyrmion from X_1 will enter the lower nanotrack, to cause a faulty response. To detect this defect, it is necessary to provide a skyrmion initially, requiring a two pattern test. Figure 5(d) shows a missing clock notch at input X_1, which will cause the input skyrmions to arrive at different times and produce incorrect results. Figure 5(e) shows the defect with an additional bridging between X_1 and X_2. The extra bridging part will cause the lower skyrmion to either enter the upper layer or change its speed, thereby changing the function of the gate. Figure 5(f) shows the defect with a missing connection between the lower and upper nanotracks, and input $X_1X_2 = 01$ produces an incorrect result. Figures 5(g)-(i) show different defects related to an OR gate.

Figure 6 shows the magnetic simulation using the $MuMax^3$ tool [30] for technology-specific defects for an inverter/fanout gate. Figure 6(a) shows the simulation of a break in the input of an inverter, which will help move the skyrmion in the lower nanotrack to the output nanotrack and produce a faulty response $Y = 1$. Figure 6(b) shows the simulation for a void in the output nanotrack. Input pattern $X = 0$ produces a faulty response $Y = 0$. All other defects (Figures 6(c)-(l)) can be described based on skyrmion-skyrmion or skyrmion-edge repulsion.

In Figures 5 and 6, we observe the erroneous outputs under different input conditions. Table II summarizes the results for all defects under exhaustive input conditions. Column 1 gives the gate type, and Columns 2 and 3 provide the input pattern and the correct output response, respectively. Columns 4-22 show responses of defective gates. The asterisk "$*$" marks the

Table II: Exhaustive simulation of skyrmion-based gates with defects.

Gate Type	Input Pattern	Correct Output	Output in presence of defect T_i																		
			T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	T_{16}	T_{17}	T_{18}	T_{19}
AND	00	0	0	0	0	0	-	0	0	0	0	-	0	-	-	0	0	0	0	-	-
	01	0	0	0	0	0	-	0	0	0	1	-	*	-	-	0	0	0	1	-	-
	10	0	0	0	0	0	-	0	0	0	0	-	*	-	-	0	0	0	0	-	-
	11	1	0	0	0	1	-	0	0	0	0	-	*	-	-	0	0	0	1	-	-
OR	00	0	0	0	0	0	-	0	0	0	0	-	0	-	-	0	0	0	0	-	-
	01	1	1	0	0	1	-	1	0	0	1	-	*	-	-	*	*	1	0	-	-
	10	1	0	1	0	1	-	0	1	0	1	-	*	-	-	*	*	1	1	-	-
	11	1	1	1	0	1	-	1	1	0	1	-	*	-	-	*	*	*	1	-	-
Inverter	0	1	1	0	0	1	1	1	0	0	1	1	*	*	-	1	1	0	0	1	0
	1	0	1	0	0	0	0	1	0	0	1	1	*	*	-	1	1	1	0	1	0
Fanout	0	00	00	00	00	00	00	00	00	01	00	00	-	-	*	00	00	10	01	00	00
	1	11	00	10	11	01	10	00	10	11	01	10	-	-	*	10	10	10	11	01	10

Table III: Skyrmion gate defect mapping onto single stuck-at faults in AND ($Y = X_1X_2$) and OR ($Y = X_1 + X_2$)logic gates.

Gate Type	Inputs X_1X_2	Defects equivalent to single stuck-at faults					
		X_1 sa0	X_1 sa1	X_2 sa0	X_2 sa1	Y sa0	Y sa1
AND	01		T_{17}				
	11	$T_1, T_2, T_3, T_6, T_7, T_8, T_{14}, T_{15}T_{16}$		$T_1, T_2, T_3, T_6, T_7, T_8, T_{14}, T_{15}T_{16}$		$T_1, T_2, T_3, T_6, T_7, T_8, T_{14}, T_{15}T_{16}$	
OR	01			T_2, T_7, T_{17}		T_3, T_8	
	10	T_1, T_6				T_3, T_8	
	11					T_3, T_8	

Table IV: Skyrmion gate defect mapping onto single stuck-at faults in inverter ($Y = \overline{X}$) and fanout ($(Y_1, Y_2) = X$).

Gate Type	Input X	Defects equivalent to single stuck-at faults			
		X sa0	X sa1	Y sa0, Y_1 sa0, Y_2 sa0	Y sa1, Y_1 sa1, Y_2 sa1
Inverter	0		$T_2, T_3, T_7, T_8, T_{17}, T_{19}$	$T_2, T_3, T_7, T_8, T_{17}, T_{19}$	
	1	$T_1, T_6, T_9, T_{10}, T_{14}, T_{15}, T_{18}$			$T_1, T_6, T_9, T_{10}, T_{14}, T_{15}, T_{18}$
Fanout	0				T_8, T_{17}
	1	T_1, T_6		$T_1, T_2, T_4, T_5, T_6, T_7, T_9$ $T_{10}, T_{14}, T_{15}, T_{18}, T_{19}$	

defects that will produce faulty response only with a pair of input patterns. Also, "$-$" denotes a "no fault" response.

IV. Fault Modeling

To deal with technology-dependent defects, it is beneficial to model them as stuck-at faults, whenever possible, so that we can take advantage of traditional EDA tools. When analyzing the results of Table II, it can be found that some special patterns can detect defects in skyrmion circuits just like they detect stuck-at faults in CMOS circuits. An input pattern 01 applied to an AND gate will produce a faulty output 1 when T_{17} is present. Similarly, the test pattern 01 can be used to detect X_1 and Y_1 stuck-at-1 faults. Also, the input pattern 11 can detect defects T_1 through T_3, T_6 through T_9 and T_{14} through T_{16}. This pattern detects the fault stuck-at-0 at X_1, X_2 and Y. Thus, defects T_1 through T_3, T_6 through T_9 and T_{14} through T_{16} can be modeled as X_1, X_2 or Y stuck-at-0. Note that these three faults are equivalent [26]. The skyrmion-based circuit defects can be mapped onto traditional stuck-at faults of a logic circuit. Table III shows how we converted the skyrmion defects to equivalent stuck-at faults. First, we find the test patterns for the skyrmion-based circuit that will produce faulty results. Then, for those patterns we list out the stuck-at faults detected in the logic gate of the same function. This way the skyrmion-based defects have been converted into conventional stuck-at fault of CMOS (logic) gates. This internal defect based fault modeling will guarantee that when the circuit is analyzed by a conventional ATPG tool, the tool will generate patterns to detect the defects in the skyrmion-based circuit.

Table IV shows that defects of inverter and fanout can also be represented by stuck-at faults. To detect defects T_{11} through T_{13} (missing annihilation notch), at least two patterns are required. The first pattern is for presetting the skyrmion in missing notch defect and then produce the incorrect operation in the second pattern. These defects cannot be modeled as stuck-at faults. To test defects T_{11} through T_{13}, we model defect T_{11} as a delay fault, for which at least two test patterns are required. Defects T_{11}, T_{12}, T_{16} of inverter and T_{13}, T_{16} of the fanout are considered as technology-dependent faults, Defects T_4, T_5 of inverter and T_3 of the fanout are considered as no faults.

V. Test Pattern Generation

To generate patterns for testing of skyrmion logic circuits, it is necessary to first covert a CMOS gate level netlist to skyrmion-based netlist. We use a commercial synthesis tool (e.g., Synopsys Design Compiler [34]) to synthesize the RTL code with specifying cell preferences with conventional CMOS cell library. In this paper, we only use AND, OR, inverter and fanout to realize circuits. However, in traditional CMOS circuits, interconnect crossover is common through vias. But, this is not permitted in skyrmion-based circuits.

To achieve crossover in skyrmion-based circuits, an additional element MTJ is required. The magnetic tunnel junction (MTJ) [35] consists of two layers of magnetic metal separated by an ultra-thin insulating layer. The insulating layer is very thin, and if a bias voltage is applied between the two metal electrodes, electrons will pass through the barrier. In MTJ, the tunneling current depends on the relative direction of the magnetization of the two ferromagnetic layers, which can be changed by the applied magnetic field. In spintronics, MTJ is often used to generate or read skyrmion. The addition of element magnetic tunnel junction (MTJ) may also cause defects in the circuit, but because we currently only focus on gate level netlist, the impacts of crossover and MTJ are not to consider at this time. However, our future work will include complex gates (e.g., more than 2 input gates, XOR, and AOI) and node crossover, the overlap of two nanotracks, to mimic the traditional synthesis including MTJ-induced defects. As we only use simple gates, we synthesize circuits with AND, OR and inverter gates. During the synthesis process, we restrict the EDA tool to use only these gates. We use set_prefer command to indicate preferred cells and set_dont_use command to exclude cells from the target library [34]. In addition, skyrmion fanout gates are added, when we encounter a fanout in the gate level netlist.

The test pattern generation for skyrmion logic circuits is straightforward. Once the circuit is synthesized and mapped with skyrmion gates, a commercial test pattern generation tool (e.g., Synopsys TestMAX ATPG [36]) is invoked to generate test patterns. It is necessary to add all faults (resulted from both technology dependent and independent defects, see Section III for details) and to provide this fault list to the ATPG tool. At this point, we only demonstrate test pattern generation for single stuck-at faults, which requires just one test pattern to detect a fault. However, some skyrmion defects (e.g., T_{11}, T_{14}, T_{15} and T_{16}) require two pattern test (like transition delay fault test [26]). Our future work will address the detection of these defects using delay fault tests.

VI. Results and Discussion

To evaluate the effectiveness of the proposed test generation process, we used Synopsys tools, Design Compiler [34] for synthesis, and TestMAX ATPG [36] for test pattern generation. We used Synopsys 32nm SAED32 EDK Generic Library [37] to synthesize ISCAS'85 benchmark circuits [38]. Table V shows the results, which include collapsed faults count,test pattern count and fault coverage for skyrmion logic circuits and compare them with traditional CMOS circuits. The first column of this table indicates the benchmark circuit name. The second and third columns show the pattern count for both conventional CMOS and skyrmion logic circuits. The fourth and fifth columns show the fault coverages for the same circuit pair. It can be inferred that our pattern generation method for skyrmion logic circuits has reduced the number of test patterns and increased fault coverage compared to the traditional CMOS circuits due to smaller number of stuck-at-1 faults in the netlist.

Figure 7 shows a gate implementation of half adder and the design of a skyrmion circuit using AND, OR and fanout gates. Our future work includes designing of NAND, NOR, and complex gates such as 3-input AND and OR, and AND-OR-Invert (AOI) gates so that traditional EDA tool can synthesize a scalable skyrmion circuit.

Table V: Testing stuck-at faults in CMOS and Skyrmion circuits.

Circuit	Number of collapsed faults		Number of test patterns		Fault coverage %	
	CMOS	Skyrmion	CMOS	Skyrmion	CMOS	Skyrmion
c17	26	16	7	7	100	100
c432	534	461	84	80	100	100
c499	1398	1199	112	109	100	100
c880	982	779	72	62	100	100
c1355	1460	1209	142	125	99.94	99.96
c1908	1262	1060	112	99	100	100
c3540	2536	2272	184	170	100	100
c6288	6766	6538	82	71	100	100

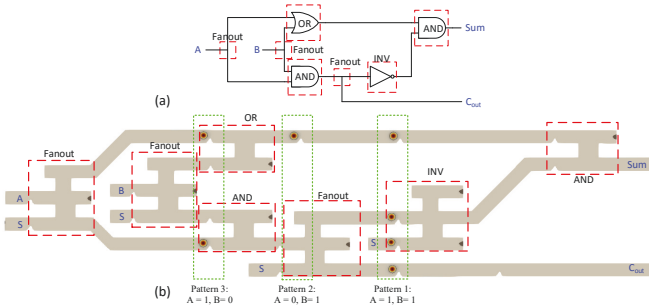

Figure 7: Skyrmion circuit design for a half adder.

VII. Conclusion

We have considered defect scenarios for skyrmion based digital circuits. We describe these defects under two separate categories, technology-independent and technology-specific defects. The defects include break in nanotrack, extra material, etching blemishes, and bridges between pairs of nanotracks. Those defects are analyzed by exhaustively simulating small structures (interconnects or single gates) using a technology simulator [30]. They are mapped onto analyzable fault models (single stuck-at, for now) using the fault equivalence [26].

The defects are classified into three categories: (1) Technology-independent such as single stuck-at faults; (2) Technology-specific faults that are not analyzable by available tools; and (3) No faults that do not cause error but may lead to aging or latent failure.

ISCAS'85 benchmark circuit results on single stuck-at faults using commercial tools show higher coverage than in CMOS circuits. A possible reason is fewer faults in the skyrmion version, in which many stuck-at-1's do not exist.

Although we have laid the groundwork, the test methodology for the skyrmion circuits is not complete. Remaining work includes technology-specific defects in Table II that could not be placed in Table III or IV. Included among those are the "no fault" defects whose latent effects must be examined.

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