A 3.75 nW Analog Electrocardiogram Processor Facilitating Stochastic Resonance for Real-Time R-wave Detection

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***Abstract*—An energy-efficient real-time processor that enhances R-waves in an electrocardiogram (ECG) signal is presented. The processor leverages a non-linear filter that models a system consisting of a particle inside a monostable well potential. The system is known to facilitate stochastic resonance (SR), where additive noise helps improving detectability of a weak signal. The processor is designed using analog signal processing techniques for simplicity of implementation and energy efficiency. Based on the schematic-level circuit simulations on the MIT-BIH arrhythmia database, the processor achieves an average sensitivity of 99.78% and an average positive predictivity of 99.65%. The power consumption excluding the bias circuitry and the thresholding stage is 3.75 nW with 1V supply voltage. The results serve as a proof-of-concept demonstration towards facilitating SR in practical signal enhancement and detection scenarios with limited power budgets.**

Keywords— analog signal processing, ECG processor, energy-efficient signal processing, stochastic resonance

I. Introduction

Electrocardiogram (ECG) is a biopotential originating from electrical activity of the heart muscles and thus carries invaluable information on cardiac health. From a single lead ECG, abnormalities in heart rate (HR), which can originate because of cardiovascular diseases [1, 2], can be detected. Accordingly, ECG has extensive clinical use for arrhythmia detection in several patient groups such as with premature ventricular complexes (PVC), left ventricular ejection fraction (LVEF), and cardiac arrest survivor [3].

Notably, arrhythmia events are intermittent and thus the success of detecting such events increases if ECG monitoring is performed outside the clinic for extended time periods from days [4] to weeks, and to months [5]. To accommodate, several research- and commercial-scale wearable [6] and injectable and implantable [7, 8] ECG monitoring approaches have been reported. Although wearable systems are well suited for ECG monitoring for hours; injectable and implantable systems are more appropriate for weeks and months of monitoring, from both signal quality and convenience of use perspectives. It should be mentioned that for implantable systems such as cardio bands and pacemakers to have sufficiently long battery life, large batteries are used, thereby increasing the footprint. Accordingly, implantable ECG systems necessitate surgery, which is not desired especially when the age group of patients are considered, and they are potentially associated with complications including bleeding and migration [9, 10]. On the other hand, injectable monitors offer smaller footprint for ease of subcutaneous placement at the cost of limited battery size and thus battery capacity. In fact, an injectable ECG system can consume as low as 65 nW in total, which translates to five days of battery lifetime with 3.7 mm^2 thin film battery [11], [12]. With the motivation of reducing the power consumption of long-term implantable/injectable ECG monitoring systems, we propose a real-time ECG processor performing R-wave detection:

An implantable/injectable ECG monitor typically consists of an ECG readout, signal conditioning, data acquisition, and data transmission blocks [11], [13]. When the scarcity of arrhythmia events is considered, digitizing and transmitting the ECG waveform continuously is not a power efficient solution. Instead, digitization and data transmission can be made when it is important to store and analyze the full ECG waveform, such as during arrhythmia events. An integrated energy-efficient processor consisting of a low-power R-wave detection processor and a succeeding low-power arrhythmia detector block such as in [14] can detect such events using a power budget negligible compared to typical μW-level radio power consumptions [15], [16].

Previously, R-wave detectors using digital processing techniques [17], [18] and analog processing techniques [19], [20] have demonstrated detection sensitivities as high as 99.3% [18] and power consumption as low as 4.8 nW [19]. In [21], an analog implementation of the Pan Tompkins algorithm [22] is reported to achieve a simulated R-wave detection sensitivity of 98.98% with a simulated power consumption of 0.5 nW. In this study, we investigate low-power circuit implementation of a new algorithm, which facilitates stochastic resonance (SR) to enhance the R-waves.

SR is a phenomenon describing the use of noise in a counterintuitive manner to enhance and detect weak signals [23], [24]. In [25], [26], we have investigated a digital signal processing algorithm that makes use of additive noise in the system to enhance neural spikes. Motivated by the observation

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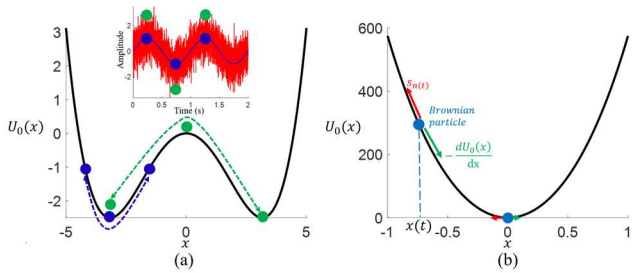

Fig. 1. Stochastic resonance (SR). See Section II.A. (a) Classical SR diagram of particle in a bistable well illustrating how optimum amount of an additive noise can enhance a weak periodic signal. (b) A monostable well also facilitates SR. The forces acting upon the particle are shown.

of SR in many biological and physical detection systems [24] [27], [28], in this study, we investigate the implementation of the algorithm in the physical domain using analog signal processing principles. Another motivation for the analog implementation stems from the high energy-efficiencies of the analog R-wave detection algorithms in the literature. Specifically, we present a new proof-of-concept application-specific integrated circuit (ASIC) heart-beat detection processor designed in a 65nm CMOS technology. We present the algorithm and the circuit implementation, as well as schematic-level circuit simulation results on the MIT-BIH arrhythmia dataset [29].

II. Stochastic Resonance and the ECG Processor

Below, we provide a description of stochastic resonance (SR) and an algorithm facilitating SR. Then, the physical implementation of the algorithm is presented in Section II.B.

A. Stochastic Resonance (SR) and Signal Enhancement

SR is a phenomenon where additive noise is used, counterintuitively, to enable detectability of a weak signal [24], [27], [28]. SR is classically explained by considering a particle in a bistable well as illustrated in Fig. 1(a) [23]. In that system, the particle stays inside one of the stable points. The input, which is a weak periodic signal, is applied as force exerted onto the particle. The other force acting upon the particle is proportional to the local slope of the well potential, wherever the particle is, in the opposite direction of the sign of the slope. The output of the system is the x-position of the particle. The weak signal, by itself, cannot make the particle pass the barrier and move to the other stable point. Instead, it swings around the stable point. On the other hand, if the input is added a proper amount of noise, the particle will be able to move back and forth between the two stable points, thereby increasing the output signal amplitude. The major consideration to take advantage of additive noise is the noise intensity. A small noise will not exert the desired push on the particle and a high noise will swamp the signal.

SR can also be facilitated when the particle is inside a monostable well potential. In fact, in [26], we have shown that electrocorticogram (ECoG) neural spikes can be enhanced by as much as 92 dB when an underdamped monostable well is used. In a monostable well, the additive noise, similar to the bistable scenario, can push the particle up along the walls of the potential well, more than the noise-free signal. In [26], we have shown that there is an optimum noise intensity maximizing the output for the particle in a monostable well, which demonstrates the existence of SR in the system.

The system consisting of a particle inside a monostable well potential can be considered as a non-linear filter with a time-varying noisy input signal of $s_n(t)$ and a time-varying output of $x(t)$. The expression describing the input-output relationship of the non-linear filter is governed by the generalized Langevin equation as [30]:

$$\frac{d^2x(t)}{dt^2} + \gamma \frac{dx(t)}{dt} = -\frac{dU_0(x)}{dx} + s_n(t), \quad (1)$$

where γ is the damping factor of the system and $U_0(x)$ is the monostable well potential:

$$U_0(x) = \frac{ax^2}{2} + \frac{bx^4}{4}. \quad (2)$$

In (2), a and b determine the wall slope and thus affect the amount of force applied on the particle by the well potential.

The solution to (1) can be obtained in the digital signal processing domain via the numerical Runge-Kutta method [14], which provides an approximate solution through iterations. Alternatively, (1) can be solved in the physical domain by implementing the differential equation as an analog electronic circuit. In fact, there have been physical demonstrations of SR using analog electronic components [23], [31]. Unlike previous circuit implementations, which aimed to build physical systems allowing *analytical investigation* of the SR phenomenon, this study aims to *facilitate* SR for signal enhancement in a practical sensing application. Accordingly, this paper presents an ultra-low power ASIC processor implementing (1) for the first time to the best of authors knowledge. The processor performing real-time R-wave detection for implantable and injectable ECG monitor systems is detailed in the next sub-section.

B. The ECG Processor

Equation (1) includes the 1st and 2nd time derivatives of $x(t)$ that can be implemented with integrators. It also requires the 3rd power of $x(t)$, which can be implemented via translinear loops on current signals. Operating on current signals is advantageous also because of the ease of implementing additions and multiplications, which are needed to introduce the constants, a, b, and γ. Schematic of the proposed processor is presented in Fig. 2 (a). The processor output, $I_x(t)$ in Fig. 2 (a), corresponds to $x(t)$ of the non-linear filter. The processor is designed in a TSMC 65nm CMOS technology and is supplied by 1 V single supply. All bias voltage and currents are supplied externally.

A 13-transistor source-degenerated operational transconductance amplifier (OTA) is designed to serve as a Gm-element in integrator blocks (Fig. 2 (b)). A leaky Gm-C integrator followed by voltage-to-current buffer serves as a current-mode integrator (Fig. 2 (c)). The cutoff frequency of the Gm-C integrator is set to 100 mHz by using a C = 20pF and setting the bias current as 30 pA. Squaring is achieved in the current domain via a translinear loop stage. Accordingly, a wide dynamic-range (1pA – 1nA) translinear loop stage is designed for squaring I_x (Fig. 3 (a)). To process both positive and negative values, bidirectionality is achieved by steering the positive and negative currents to PMOS- and NMOS- translinear circuits via a class-B stage. The devices of the class-B stage are

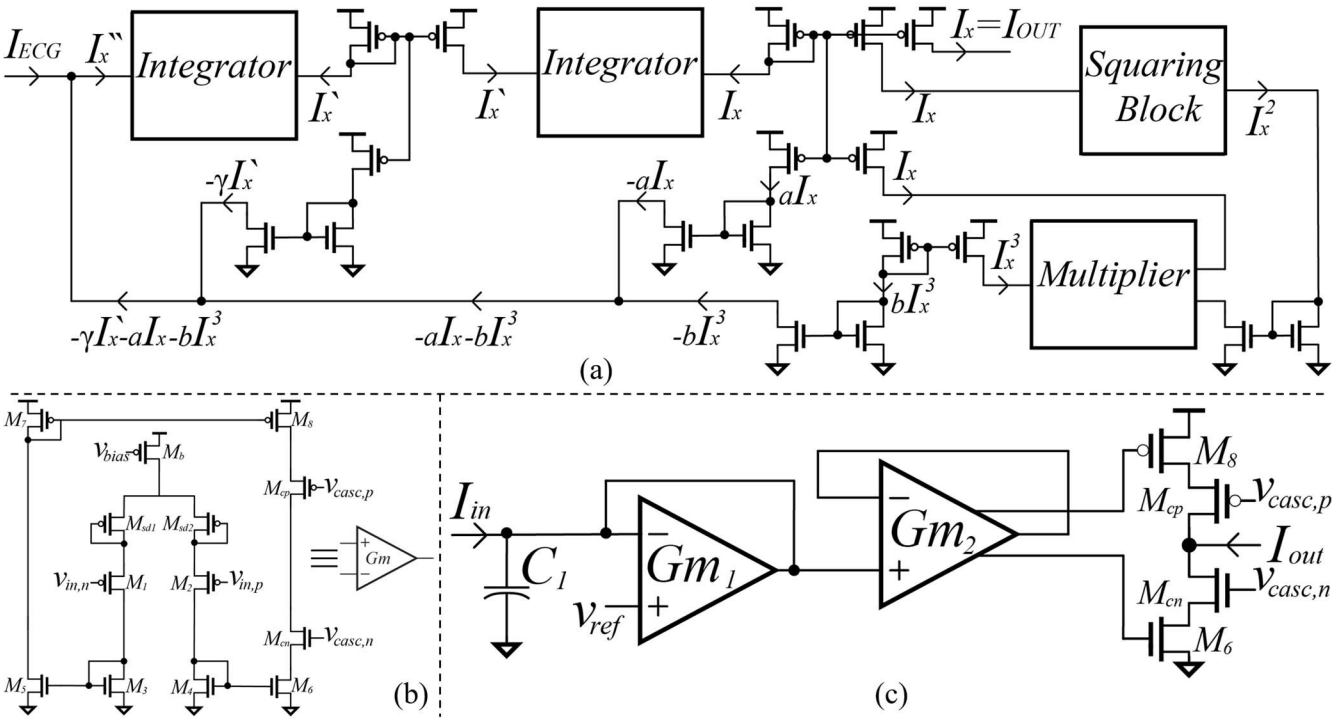

Fig. 2. The schematics of the proposed processor. (a) Complete system architecture of the proposed processor. (b) 13-transistor OTA that is used as Gm block in integrators. (c) Current mode integrator realized by current-to-voltage Gm-C leaky integrator and voltage-to-current converter.

controlled by the output of an inverter. The devices $M_{N1} - M_{N5}$ and $M_{P1} - M_{P5}$ are sized to operate in subthreshold region. A KVL analysis along the branch starting from the source of $M_{N1(P1)}$ and ending at the source of $M_{N5(P5)}$ yields to the following input-output relationship:

$$I_x^2 = \begin{cases} \frac{I_x^{\kappa_n+1}}{I_{D_{N4}}^{\kappa_n}} - I_{D_{subs}}, & I_x < 0 \\ 0, & I_{in} = 0, \\ \frac{I_x^{\kappa_p+1}}{I_{S_{P4}}^{\kappa_p}} - I_{D_{subs}}, & I_x > 0 \end{cases} \quad (3)$$

where $I_{D_{subs}}$ is a subtraction current controlled by V_{subs} to remove the dc offset originating from difference between $\kappa_n$and κ_p, with $\kappa_{n(p)}$ being the capacitive ratio of depletion and oxide capacitances of the NMOS (PMOS) in subthreshold regime, $\kappa_{n(p)} = \frac{C_{ox,n(p)}}{C_{ox,n(p)}+C_{dep,n(p)}}$. Similar to the squaring block, a wide dynamic-range (1p – 20nA) multiplier is designed with two translinear stages for bidirectionality (Fig. 3 (b)). Notably, I_x^2 represents a positive value and thus is unidirectional. On the other hand, the current steering scheme of the squaring block explained above is implemented for the bidirectional I_x. The well parameters of a and b are introduced via current mirrors at the multiplier output. I_x^3 is mirrored with a factor of b and I_x is mirrored with a factor of a, which is followed by reversing the directions of aI_x and bI_x^3 to obtain $\frac{dI_x^2(t)}{dt^2}$ at the input of the 1st integrator (I_x'' in Fig. 2 (a)) as:

$$\frac{dI_x^2(t)}{dt^2} = -\gamma \frac{dI_x(t)}{dt} - aI_x(t) - bI_x^3(t) + I_{ECG}. \quad (4)$$

In (4), which has the same form as (1), $I_x(t)$ and I_{ECG} respectively correspond to $x(t)$ and $s_n(t)$ in (1).

III. Results and Discussion

The processor is simulated in Cadence Virtuoso Analog Design environment for validation and R-wave detection performance assessment. For R-wave detection performance assessment, the 48 ECG recordings of the MIT-BIH arrhythmia database [29] is used. The recordings are sampled at 360 Hz with 11-bit resolution. To feed recordings into the simulation environment, recordings are pre-conditioned by representing them in the current domain with a maximum amplitude of 100 pA_{pp}. Pre-conditioned recordings are fed to the Virtuoso simulation environment and outputs of the proposed processor are moved to MATLAB, where a 10 pA constant threshold is applied to identify the detected R-waves. The R-waves detected are compared with the true R-waves provided in the database. R-wave detection performance of the processor is assessed using the metrics of detection sensitivity (Se), positive predictivity ($+P$), error rate (DER), and accuracy (Acc) calculated using true positive (TP), false positive (FP), and false negative (FN) values as:

$$Se = \frac{TP}{TP+FN} * 100 \qquad +P = \frac{TP}{TP+FP} * 100$$
$$DER = \frac{FP+FN}{TP} * 100 \qquad Acc = \frac{TP}{TP+FN+FP} * 100. \quad (5)$$

The performance metric values are presented in Table I and example simulated waveforms from the processor are presented in Fig. 4. Based on the analysis, the proposed processor achieves an average Se=99.78% (±0.84) and an average +P=99.65% (±1.38). The worst R-wave detection performance is obtained from the recording 207 (Se=94.35% and $+P$=90.74%). Reasons for poor performance in recording 207 include high amplitude ringing, R-waves with only negative portion, and tall T-waves.

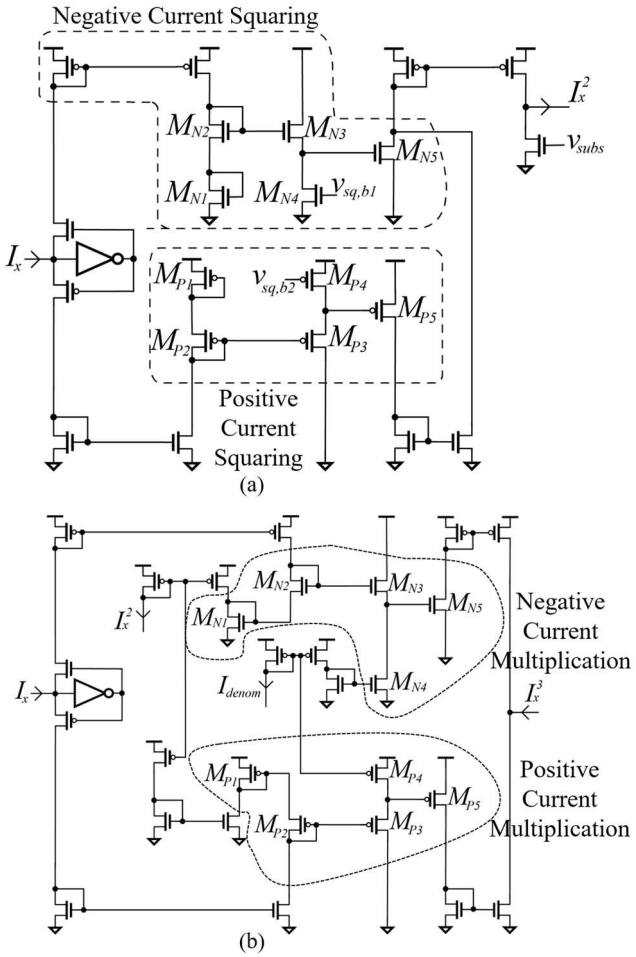

Fig. 3. Schematics of squaring and multiplication circuits. (a) Squaring block. Squaring is done with two translinear loops each for one direction of the input current. (b) Multiplication block. Similarly, multiplication is realized by two translinear loop to achieve bidirectionality.

In recording 207, 35% of FNs are caused by short R-waves and 43% percent of FNs are caused by R-waves with only negative portion. 30% and 70% of FPs are caused by tall T-waves and high amplitude ringing, respectively. To analyze the effect of the temperature on the processor performance, operating temperature is swept from -100°C to 100°C while *recording 100* is fed to the processor. Sweep results indicate that the temperature changes the peak amplitude of the output, which can be eliminated via adaptive thresholding.

A comparison of the results with low power R-wave detection implementations is presented in Table II. The proposed processor achieves better power performance than the analog approaches in [19], [20]. In fact, in terms of power consumption, there is only one processor [21] that outperforms the proposed processor. On the other hand, detection sensitivity of the proposed processor is better than [21]. A closer investigation on the output signals reveal that, tall T-waves in some recordings are falsely detected as R-waves (Fig. 5).

Previously we showed that, well and damping parameters a, b, and γ can be tuned to maximize signal enhancement and noise suppression [26]. In light of those results, the R-wave

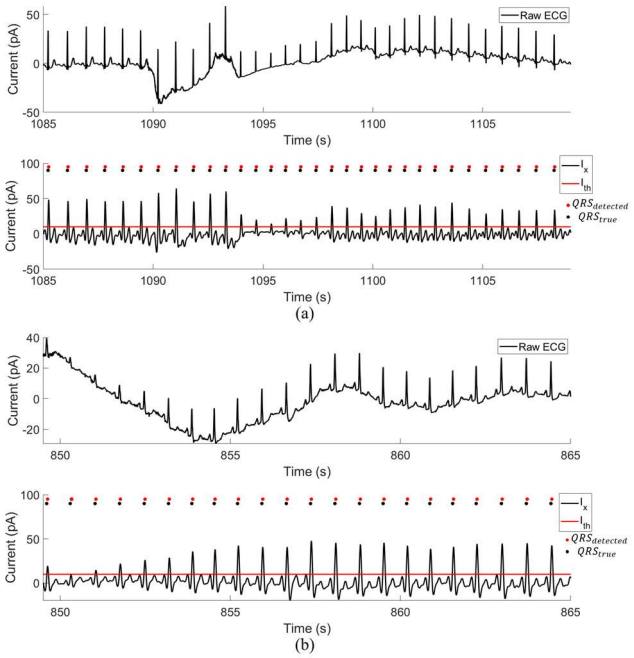

Fig. 4. Example simulated waveforms from the raw ECG signal and the proposed processor output are shown for two recordings from the MIT-BIH arrhythmia database. $QRS_{detected}$ is detected R-waves by the proposed processor and QRS_{true} is ground truth R-wave locations obtained from database (a) 25s portion of recording 103. (b) 15s portion of recording 105.

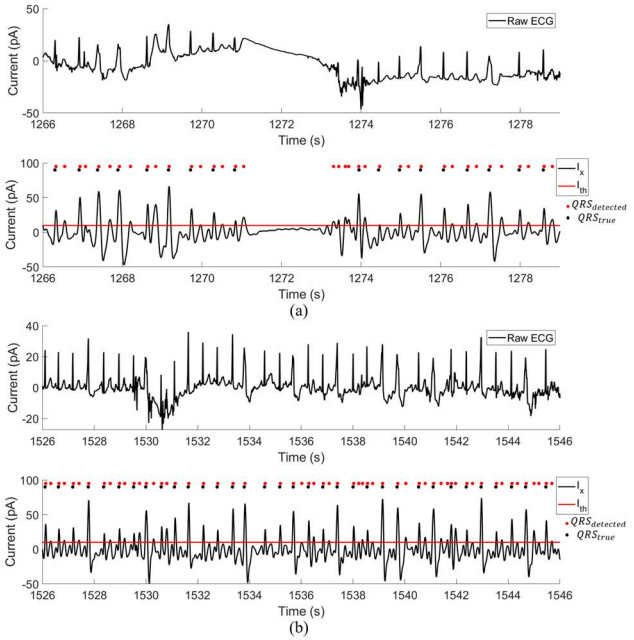

Fig. 5. Two example simulated waveforms experiencing false positives due to tall T-waves are shown. (a) 13s portion from recording 208. (b) Another 20s portion from recording 208.

detection performance of the processor can be potentially improved by fine tuning on well parameters and damping factor to better suppress tall T-waves and noise only portions. Moreover, adaptively controlling the threshold level with the

TABLE I
PERFORMANCE EVALUATION OF THE PROPOSED ECG PROCESSOR

ECG record #	Total # of Beats	Se (%)	+P (%)	DER	Acc (%)
100	2273	100	100	0	100
101	1865	100	100	0	100
102	2187	100	99.82	0.18	99.89
103	2084	100	100	0	100
104	2229	100	100	0	100
105	2572	99.96	99.5	0.54	99.46
106	2027	100	99.9	0.09	99.9
107	2137	100	99.76	0.23	99.76
108	1774	99.88	99.94	0.16	99.83
109	2532	100	100	0	100
111	2124	99.95	100	0.04	99.95
112	2539	99.96	100	0.03	99.96
113	1795	99.94	99.83	0.22	99.78
114	1879	100	99.79	0.21	99.79
115	1953	100	100	0	100
116	2412	99.09	99.96	0.96	99.05
117	1535	99.94	100	0.06	99.94
118	2288	100	100	0	100
119	1987	100	100	0	100
121	1863	99.95	100	0.05	99.95
122	2476	100	100	0	100
123	1518	100	100	0	100
124	1619	100	100	0	100
200	2601	99.76	100	0.23	99.76
201	1963	99.79	97.51	2.75	97.32
202	2136	99.95	99.76	0.28	99.72
203	2980	99.83	99.96	0.2	99.79
205	2657	99.89	100	0.12	99.89
207	1860	94.35	90.74	16.18	86.07
208	2955	99.72	99.93	0.33	99.66
209	3005	99.93	99.93	0.13	99.87
210	2650	99.93	99.78	0.3	99.7
212	2748	100	100	0	100
213	3251	100	100	0	100
214	2262	100	99.96	0.05	99.96
215	3363	99.94	100	0.05	99.94
217	2208	100	100	0	100
219	2154	100	99.27	0.74	99.27
220	2048	100	100	0	100
221	2427	100	100	0	100
222	2483	98.35	98.15	3.56	96.56
223	2605	99.93	100	0.09	99.93
228	2053	99.86	99.86	0.29	99.71
230	2256	100	100	0	100
231	1573	99.94	99.94	0.12	99.88
232	1780	99.78	99.78	0.45	99.55
233	3079	100	100	0	100
234	2753	100	100	0	100
Overall	**109518**	**99.78**	**99.65**	**0.59**	**99.46**

help of an energy-efficient analog memory such as in [34] could further enhance the detection performance.

It is worth noting that, the proposed processor should be provided with current-mode ECG, which can be obtained via a current-mode instrumentation amplifier architecture such as in [35, 36]. Also, although the thresholding is performed digitally in this proof-of-concept study, the constant threshold can be applied to the current output of the processor via a winner-take-all circuit [37, 38] while consuming ~6 pW [39]. Additionally, bias voltages and currents can be generated by pW-level bias circuitry based on the principle of self-regulated push-pull voltage reference generator [40] with ~10 pW power consumption [41].

TABLE II
COMPARISON WITH ENERGY-EFFICIENT R-WAVE DETECTORS

	Algorithm / Domain	Type / Technology	Performance		Power
			Se (%)	Pp (%)	
This work	SR-based Analog	ASIC / 65nm	99.78	99.65	3.75 nW (Simulated)
[21]	PT-based Analog	ASIC / 65nm	98.98	98.9	0.5 nW (Simulated)
[17]	QSWT Digital	ASIC / 180nm	99.29	N/A	457 nW
[2]	PT-based Digital	ASIC / 65nm	99.83	98.65	2.78 µW
[33]	PT-based Digital	ASIC / 130nm	99.85	99.93	3.84 µW
[18]	A-CLT Digital	ASIC / 65nm	99.3	99.38	6.5 nW (Simulated)
[19]	Analog	ASIC / 180nm	N/A	N/A	4.8 nW
[20]	Analog + Digital	ASIC / 180nm	N/A	N/A	800 nW (Excluding digital)

It should be noted that, the investigation of physical implementation of a system known to facilitate SR in enhancing the weak signals is performed with the primary goal of achieving high accuracy R-wave detection while consuming low power. Demonstration of the characteristic bell-shape curve of SR [26], [31] and investigation of the effects of well types and parameters are left as a future work. However, those studies are expected to provide valuable insights as to how the processor parameters should be tuned, and if and how much noise should be added to the ECG signal to optimize the R-wave detection performance.

IV. CONCLUSION

An energy-efficient ECG processor to detect R-waves in real time is presented. The processor innovatively implements a non-linear filter modeling the physical interaction of a particle in a monostable well potential, a system known to facilitate stochastic resonance (SR). The processor implemented in a 65nm CMOS process using analog signal processing techniques demonstrates low power consumption and high R-wave detection sensitivity and positive predictivity when validated against a public ECG database through schematic-level simulations. The processor is the first example towards leveraging SR to enhance weak signals and improve detectability in low power-budget sensor system scenarios.

REFERENCES

[1] M. Shabaan, K. Arshid, M. Yaqub et al., "Survey: smartphone-based assessment of cardiovascular diseases using ECG and PPG analysis," in *BMC Med Inform Decis Mak*, vol. 20, pp. 177, 2020, doi: https://doi.org/10.1186/s12911-020-01199-7.

[2] N. Bayasi, T. Tekeste, H. Saleh, B. Mohammad, A. Khandoker and M. Ismail, "Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 24, no. 5, pp. 1962-1974, May 2016, doi: 10.1109/TVLSI.2015.2475119.

[3] D. S. Cannom, E. N. Prystowsky, "Management of Ventricular Arrhythmias: Detection, Drugs, and Devices," in *JAMA,* vol. 281, no. 2, pp. 172–179, 1999, doi:10.1001/jama.281.2.172I.

[4] A. Page, T. Soyata, J. -P. Couderc and M. Aktas, "An Open Source ECG Clock Generator for Visualization of Long-Term Cardiac Monitoring Data," in *IEEE Access*, vol. 3, pp. 2704-2714, 2015, doi: 10.1109/ACCESS.2015.2509426

[5] S. S. Lobodzinski, M. M. Michael, “New devices for very long-term ECG monitoring,” in *Cardiology Journal*, vol.19, no. 2, pp. 210-214, 2012.

[6] AliveCor. KardiaBand. Accessed: June 10, 2021. [Online]. Available: https://store.alivecor.com/products/kardiamobile

[7] Medtronic. Reveal LINQ. Accessed: June 10, 2021. [Online]. Available: https://www.medtronic.com/us-en/healthcare-professionals/products/cardiac-rhythm/cardiac-monitors/reveal-linq-icm.html

[8] Abbott. Confirm Rx. Accessed: June 10, 2021. [Online]. Available: https://confirmyourrhythm.com

[9] J. Bong, O. Yasin, V. R. Vaidya, et al., “Injectable Flexible Subcutaneous Electrode Array Technology for Electrocardiogram Monitoring Device,” *ACS Biomaterials Science & Engineering*, vol. 6, no. 5, pp. 2652-2658, 2020, doi: 10.1021/acsbiomaterials.9b01102.

[10] R. J. Nuis, N. M. Van Mieghem, C. J. Schultz et al., “Timing and potential mechanisms of new conduction abnormalities during the implantation of the Medtronic CoreValve System in patients with aortic stenosis,” *European Heart Journal*, vol. 32, no. 16, pp. 2067–2074, 2011, doi: https://doi.org/10.1093/eurheartj/ehr110.

[11] Y. -P. Chen et al., "An Injectable 64 nW ECG Mixed-Signal SoC in 65 nm for Arrhythmia Monitoring," in IEEE Journal of Solid-State Circuits, vol. 50, no. 1, pp. 375-390, Jan. 2015, doi: 10.1109/JSSC.2014.2364036.

[12] Y. H. Jung, et al., “Injectable Biomedical Devices for Sensing and Stimulating Internal Body Organs,” *Adv. Mater.*, vol. 32, no. 16, pp. 1907478, 2020, doi:https://doi.org/10.1002/adma.201907478.

[13] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim and C. Van Hoof, "A 30 μW Analog Signal Processor ASIC for Portable Biopotential Signal Monitoring," in *IEEE Journal of Solid-State Circuits,* vol. 46, no. 1, pp. 209-223, Jan. 2011, doi: 10.1109/JSSC.2010.2085930.

[14] S. Shah, H. Töreyin, C. B. Güngör and J. Hasler, "A Real-Time Vital-Sign Monitoring in the Physical Domain on a Mixed-Signal Reconfigurable Platform," in *IEEE Transactions on Biomedical Circuits and Systems,* vol. 13, no. 6, pp. 1690-1699, Dec. 2019, doi: 10.1109/TBCAS.2019.2949778

[15] Y. Lee et al., "A Modular 1 mm^3 Die-Stacked Sensing Platform With Low Power I^2C Inter-Die Communication and Multi-Modal Energy Harvesting," in IEEE Journal of Solid-State Circuits, vol. 48, no. 1, pp. 229-243, Jan. 2013, doi: 10.1109/JSSC.2012.2221233.

[16] X. Zhang, Z. Zhang, Y. Li, C. Liu, Y. X. Guo and Y. Lian, "A 2.89 μW Dry-Electrode Enabled Clockless Wireless ECG SoC for Wearable Applications," in IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2287-2298, Oct. 2016, doi: 10.1109/JSSC.2016.2582863.

[17] X. Liu et al., "A 457 nW Near-Threshold Cognitive Multi-Functional ECG Processor for Long-Term Cardiac Monitoring," *in IEEE Journal of Solid-State Circuits,* vol. 49, no. 11, pp. 2422-2434, Nov. 2014, doi: 10.1109/JSSC.2014.2338870.

[18] T. Tekeste, H. Saleh, B. Mohammad and M. Ismail, "Ultra-Low Power QRS Detection and ECG Compression Architecture for IoT Healthcare Devices," in *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 66, no. 2, pp. 669-679, Feb. 2019, doi: 10.1109/TCSI.2018.2867746.

[19] D. Da He and C. G. Sodini, "A 58 nW ECG ASIC With Motion-Tolerant Heartbeat Timing Extraction for Wearable Cardiovascular Monitoring," in *IEEE Transactions on Biomedical Circuits and Systems,* vol. 9, no. 3, pp. 370-376, June 2015, doi: 10.1109/TBCAS.2014.2346761.

[20] L. Yan et al., "A 13 μA Analog Signal Processing IC for Accurate Recognition of Multiple Intra-Cardiac Signals," in *IEEE Transactions on Biomedical Circuits and Systems,* vol. 7, no. 6, pp. 785-795, Dec. 2013, doi: 10.1109/TBCAS.2013.2297353.

[21] C. B. Güngör and H. Töreyin, "A 0.5 nW Analog ECG Processor for Real Time R-wave Detection Based on Pan-Tompkins Algorithm," *2019 IEEE EMBS International Conference on Biomedical & Health Informatics (BHI),* Chicago, IL, USA, 2019, pp. 1-4, doi: 10.1109/BHI.2019.8834508.

[22] J. Pan and W. J. Tompkins, “A Real-Time QRS Detection Algorithm,” in *IEEE Trans. Biomed. Eng.,* vol. 32, no. 3, pp. 230–236, 1985.

[23] L. Gammaitoni, P. Hanggi, P Jung, F Marchesoni “Stochastic resonance,” *Rev. Mod. Phys.*, vol. 70, pp. 223–287, 1998.

[24] D. Dai, Q. He, “Multiscale noise tuning stochastic resonance enhances weak signal detection in a circuitry system,” vol. 23, pp. 115001, 2012.

[25] C. B. Güngör and H. Töreyin “Facilitating stochastic resonance as a pre-emphasis method for neural spike detection,” *J. Neural Eng.*, vol. 17, no.4, pp. 046047, 2020.

[26] C. B. Güngör, P. P. Mercier, and H. Töreyin “Investigating well potential parameters on neural spike enhancement in a stochastic-resonance pre-emphasis algorithm,” *J. Neural Eng.*, vol. 18, no.4, pp. 046062, 2021.

[27] D. Russell, L. Wilkens, F. Moss, “Use of behavioural stochastic resonance by paddle fish for feeding,” *Nature* vol. 402, pp. 291–294, 1999, doi: https://doi.org/10.1038/46279.

[28] J. Liu , Y. Leng, Z. Lai, S. Fan, “Multi-frequency signal detection based on frequency exchange and re-scaling stochastic resonance and its application to weak fault diagnosis,” *Sensors*, vol. 18, no. 5, pp. 1325, 2018.

[29] G. B. Moody and R. G. Mark, “The Impact of the MIT-BIH Arrhythmia Database: History, Lessons Learned, and Its Influence on Current and Future Databases,” in *Ieee Eng. Med. Biol.,* no. June, pp. 45–50, 2001.

[30] S. Lu, Q. He, F. Kong, “Effects of underdamped step-varying second-order stochastic resonance for weak signal detection,” *Digit. Signal Process.*, vol. 36, pp. 93–103, 2015.

[31] D. G. Luchinsky, R. Mannella, P. V. E. McClintock and N. G. Stocks, "Stochastic resonance in electrical circuits. I. Conventional stochastic resonance," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 9, pp. 1205-1214, Sept. 1999, doi: 10.1109/82.793710.

[32] N. Bayasi, T. Tekeste, H. Saleh, B. Mohammad, A. Khandoker and M. Ismail, "Low-Power ECG-Based Processor for Predicting Ventricular Arrhythmia," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 24, no. 5, pp. 1962-1974, May 2016, doi: 10.1109/TVLSI.2015.2475119.

[33] S. K. Jain and B. Bhaumik, "An Energy Efficient ECG Signal Processor Detecting Cardiovascular Diseases on Smartphone," in *IEEE Transactions on Biomedical Circuits and Systems,* vol. 11, no. 2, pp. 314-323, April 2017, doi: 10.1109/TBCAS.2016.2592382.

[34] C. B. Güngör and H. Töreyin, "Using Floating-Gate MOS as a Non-Volatile Analog Memory for Energy-Efficient Adaptive Thresholding in ECG Sensors," 2019 IEEE SENSORS, 2019, pp. 1-4, doi: 10.1109/SENSORS43011.2019.8956765.

[35] Y. H. Ghallab, W. Badawy, K. V. I. S. Kaler and B. J. Maundy, "A novel current-mode instrumentation amplifier based on operational floating current conveyor," in IEEE Transactions on Instrumentation and Measurement, vol. 54, no. 5, pp. 1941-1949, Oct. 2005, doi: 10.1109/TIM.2005.854254.

[36] S. J. Azhari and H. Fazlalipoor, "A novel current mode instrumentation amplifier (CMIA) topology," in IEEE Transactions on Instrumentation and Measurement, vol. 49, no. 6, pp. 1272-1277, Dec. 2000, doi: 10.1109/19.893269.

[37] T. Serrano and B. Linares-Barranco, "A modular current-mode high-precision winner-take-all circuit," Proceedings of IEEE International Symposium on Circuits and Systems - ISCAS '94, 1994, pp. 557-560 vol.5, doi: 10.1109/ISCAS.1994.409436.

[38] S. Ramakrishnan and J. Hasler, "Vector-Matrix Multiply and Winner-Take-All as an Analog Classifier," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 2, pp. 353-361, Feb. 2014, doi: 10.1109/TVLSI.2013.2245351.

[39] A. Fish and O. Yadid-Pecht, "CMOS current/voltage mode winner-take-all circuit with spatial filtering," ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196), 2001, pp. 636-639 vol. 2, doi: 10.1109/ISCAS.2001.921391.

[40] H. Wang and P. P. Mercier, "A 14.5 pW, 31 ppm/°C resistor-less 5 pA current reference employing a self-regulated push-pull voltage reference generator," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), 2016, pp. 1290-1293, doi: 10.1109/ISCAS.2016.7527484.

[41] C. B. Güngör, P. P. Mercier and H. Töreyin, "A 1.2nW Analog Electrocardiogram Processor Achieving a 99.63% QRS Complex Detection Sensitivity," in IEEE Transactions on Biomedical Circuits and Systems, vol. 15, no. 3, pp. 617-628, June 2021, doi: 10.1109/TBCAS.2021.3092729.