Stable Universal 1- and 2-Input Single-Molecule Logic Gates

Ran Liu, Yingmei Han, Feng Sun, Gyan Khatri, Jaesuk Kwon, Cameron Nickle, Lejia Wang, Chuan-Kui Wang, Damien Thompson, Zong-Liang Li, Christian A. Nijhuis*, and Enrique del Barco**

Dr. R. Liu, G. Khatri, Dr. J. Kwon, Dr. C. Nickle, Prof. E. del Barco
Department of Physics, University of Central Florida, Orlando, FL 32816, USA
E-mail: delbarco@ucf.edu

Dr. Y. Han, Dr. L. Wang, Prof. C.A. Nijhuis
Department of Chemistry, National University of Singapore, 3 Science Drive 3, Singapore 117543, Singapore
E-mail: c.a.nijhuis@utwente.nl

F. Sun, Prof. C. K. Wang, Prof. Z. L. Li
Key Laboratory of Medical Physics and Image Processing of Shandong Province, School of Physics and Electronics, Shandong Normal University, Jinan 250358, China
E-mail: lizongliang@sdnu.edu.cn

Dr. L. Wang
School of Materials and Chemical Engineering, Ningbo University of Technology, Ningbo, China.

Prof. D. Thompson
Department of Physics, Bernal Institute, University of Limerick, Limerick, Ireland

Prof. C.A. Nijhuis
Hybrid Materials for Opto-Electronics Group, Department of Molecules and Materials, MESA+ Institute for Nanotechnology, Molecules Center and Center for Brain-Inspired Nano Systems, Faculty of Science and Technology, University of Twente, 7500 AE Enschede, The Netherlands

Keywords: Molecular computing, Coulomb blockade, Logic gate, Molecular electronics, Single-electron transistor.

Abstract: Controllable single-molecule logic operations would enable development of reliable ultra-minimalistic circuit elements for high-density computing but require stable currents from multiple orthogonal inputs in molecular junctions. Utilizing the two unique adjacent conductive molecular orbitals (MOs) of gated Au/S-$(CH_2)_3$-Fc-$(CH_2)_9$-S/Au (Fc=ferrocene) single-electron transistors (~2 nm), we present a stable Single-Electron Logic Calculator (SELC) allowing real-time modulation of output current as a function of orthogonal input bias (*Vb*) and gate (*Vg*) voltages. Reliable and low-voltage ($|Vb|$<80 mV, $|Vg|$<2 V) operations of SELC depend upon the unambiguous association of current resonances with energy shifts of the MOs (which show an invariable, small energy separation of ~100 meV) in response to the changes of voltages, which is confirmed by electron transport calculations. Stable multi-logic operations based on the SELC modulated current conversions between the two resonances and Coulomb blockade regimes were demonstrated via the implementation of all universal 1-input (YES/NOT/PASS_1/PASS_0) and 2-input (AND/XOR/OR/NAND/NOR/INT/XNOR) logic gates.

1. Introduction

Effective control of electronic properties of molecular junctions for stable rectification[1-2], switching[3-4], memory[5-6] and logic operation[7-12] is critical for reducing the area and power consumption of electrical circuits. Important advances have been made in the design of multifunctional molecular devices that employ external stimuli (*e.g.*, chemical, light, magnetic or electric field) to modulate electron transport through molecular junctions[2-3,5,7,11,13-21]. The modulations typically rely on stimulus-induced changes in molecular electronic states[5,14,22] and therefore the functional diversity and signal stability of molecular devices depend on the availability of different stable electronic states and efficient conversions between them[2-3,7,23]. As all-electrical-driven devices, three-terminal solid-state single-electron transistors (SETs)[17,24-30] not only reflect the quantum behavior of intramolecular electron transport, such as Coulomb blockade[19-20,31-32], Zeeman effect[20-21], thermoelectric properties[25-26,33] and Kondo effect[21,34-36], but also have the unique advantage of controlling the molecular orbitals (MOs) by applying external electrostatic potentials[17,26,36-39], thereby providing new opportunities for the ultra-miniaturization of computing elements[40-43]. However, there are still two key challenges in utilizing SETs in single-molecule functional devices. First, the

background electrostatic potentials of molecular junctions that affect the absolute energy of MOs are difficult to control, and so the resonance regions determined by MOs are normally different for different junctions formed with the same molecule[19-20,31,43]. Second, the multifunctional implementation requires clear boundaries between Coulomb blockade and resonance regimes[20,28,32], which are complicated by the electrode-induced energy-level broadening of MOs[17,28-29,44].

Targeting these two challenges, we screened Au/S-$(CH_2)_3$-Fc-$(CH_2)_9$-S/Au (Fc=ferrocene) SETs from five different kinds of Fc-based gated SET junctions (see **Figure 3** and Supplementary Information (SI) S8) and designed a prototype Single-Electron Logic Calculator (SELC). First, instead of relying on absolute currents affected by the uncertainty of background electrostatic potentials, we employ current conversions between two sturdy and well-defined resonance regimes rendered by two adjacent conductive MOs of Fc. The MOs have a stable, small energy separation of around 100 meV and sit close to the Fermi energy of the electrodes in all five different Fc-based SETs and our DFT calculations show that this energy signature is not dependent on the conformation of the molecule inside the transistor[24-25],[45-48]. Crucially, our measurements and calculations show that the current conversions due to the modulation of MOs by gate (*Vg*) and bias (*Vb*) voltages are stable. Second, we used n-alkyl (-$(CH_2)_n$-, n≥3) linkers to minimize the broadening of the MO energy levels[25] on the Fc moiety by effectively isolating Fc from the electrodes[16,49-50]. Hence, we obtained a sharp-edged diamond-shaped Coulomb blockade regime in Au/S-$(CH_2)_3$-Fc-$(CH_2)_9$-S/Au SETs that allows the generation of clear current switching signals. The small energy separation of the two adjacent conductive MOs of Fc supports logic operations at low input voltages ($|Vb|$<80 mV, $|Vg|$<2 V) far below the 1.5-5 V drive voltage and 3-15 V gate voltage of CMOS (Complementary Metal Oxide Semiconductor). By implementing all universal logic gates (the four 1-input gates YES, NOT, PASS_1, and PASS_0 and the seven 2-input gates AND, XOR, OR, NAND, NOR, INT, and XNOR), we demonstrate reliable programmable logic operations based on one single-molecule SET.

2. The SELC Design

Figure 1A, B show the schematic configuration and circuit design of the three-terminal SELC comprising the functional Au/S-$(CH_2)_3$-Fc-$(CH_2)_9$-S/Au molecular junction (see SI-S1 and S2 for details) strung over an Al back-gate (third terminal) with Al_2O_3 as the insulating layer between the junction and the gate. Along the junction, the Fc moiety is electronically isolated by the -$(CH_2)_3$- and -$(CH_2)_9$- linkers on either side and the molecule is connected to the source

and drain nano-electrodes by thiolate–metal bonds. Studies of similar Fc-based molecules in three-terminal SETs[24-25] and SAM-based junctions[49,51-53] have shown that asymmetric -$(CH_2)_n$- linkers cause unequal coupling between the molecule and the electrodes, leading to current rectification[49] and thus providing a natural route to encode information *via* orthogonal modulations of the MOs by *Vg* and *Vb*. To minimize the probability of several molecules bridging one nanogap, we created low coverage of molecules on an array of gold electrodes[21] (see SI-S2). In the experiment, after electromigration, 37 of the 214 correctly broken nanowires showed a molecular signal (current of nA scale, see Figure S3). That is, the molecules were sufficiently diluted that less than 20% of the nanogaps could be successfully connected by molecules, which greatly reduces the possibility of multiple molecules connecting between the same nanogap at the same time (< 4%).

Figure 1C, D show representative *I-Vg* and *I-Vb* curves measured from the three-terminal junction at different values of *Vb* and *Vg*, respectively. The distinct current bi-plateau feature and the linear variation of the switch points and widths of the plateaus with *Vg* and *Vb* indicate that the molecular junction has been formed and the current through it can be effectively controlled by *Vg* and *Vb*.

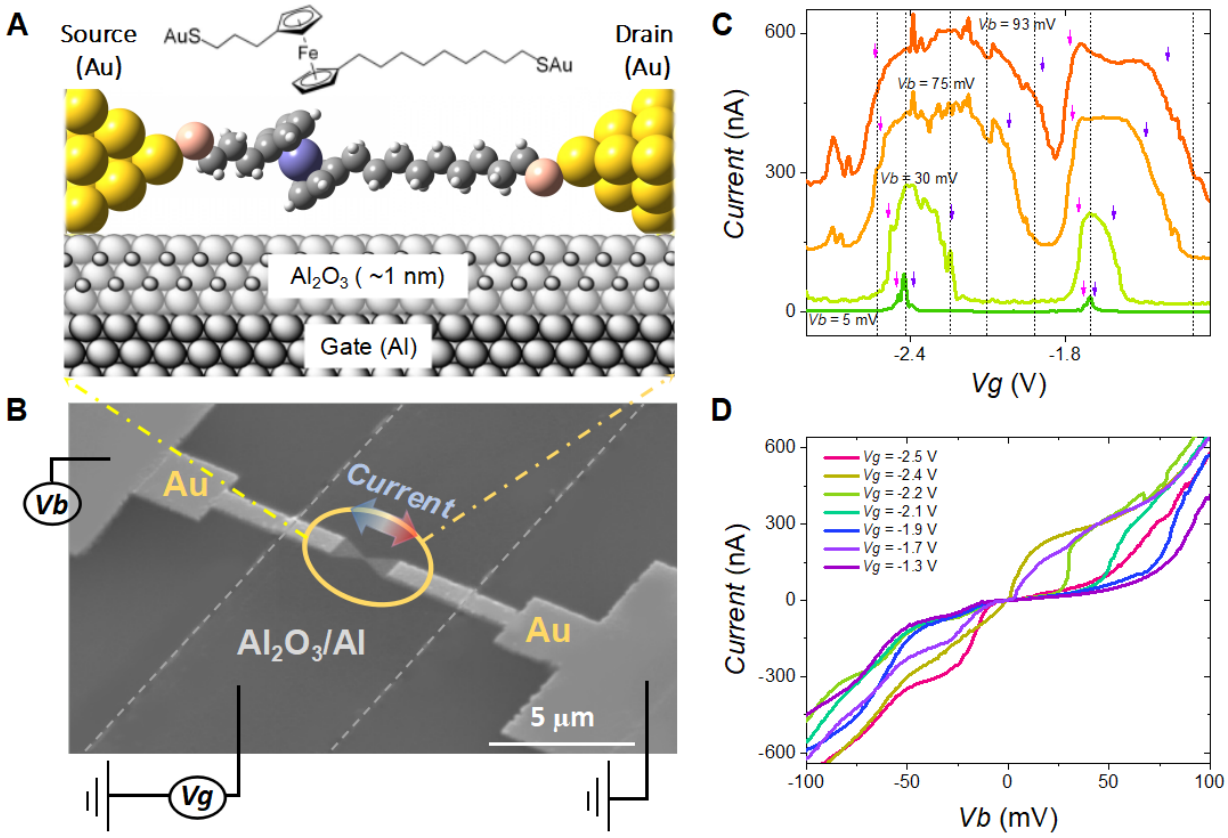


Figure 1. The design of SELC. (**A**) Chemical structure and schematic of a S-$(CH_2)_3$-Fc-$(CH_2)_9$-S molecule bridging the nanogap between two nano-electrodes. (**B**) SEM image of a SELC showing the Au nanowire on

the Al_2O_3/Al back-gate on a Si wafer and positions where V_b and V_g are applied. The nanowire and the back-gate were patterned by electron-beam and optical lithography, respectively[54]. The molecular junction formed in the center of the nanowire was produced using current feedback-controlled electromigration[17,25,55-56] (see SI-S2 for details). (**C**) Representative *I-Vg* curves for different values of *Vb* measured at 225 mK. The arrows mark the switch points of the current plateaus. The dashed lines indicate the *Vg* values corresponding to the seven *I-Vb* curves in (D). (**D**) Representative *I-Vb* curves for the seven different *Vg* values. T = 225 mK.

3. Results and Discussion

3.1. Current map measurements and calculations

The color-map of the measured current through the SELC as a function of *Vb* and *Vg* is shown in **Figure 2**B. The color code divides the map into different transmission regimes. The red and blue colors respectively indicate the positive and negative currents in the resonance regime, where the energy levels of the conductive MOs (ε_1: HOMO-1 and ε_2: HOMO-2, see SI-S3 (2)) lie within the bias window, are well-separated, and are conductive due to their coupling to both electrodes (in contrast to ε_0: HOMO, where the long-alkyl chain isolates the Fc-centered level from one electrode). In the map, ε_1 and ε_2 indicate their resonance regions. One distinct characteristic, which is shared by all five different kinds of Fc-based gated SETs (see SI-S8), is evident in Figure 2, showing that ε_1 and ε_2 overlap at around ±100 meV. The left (*ɤ'*) and right (*ɤ''*) dashed lines indicate the edges of the ε_1 resonance region. Clear transitions between the resonance regime and the Coulomb blockade regime (white diamond-shaped areas) are shown in the corresponding differential conductance (*dI/dV*) map of Figure 2D. '1', '3' and '5' indicate the Coulomb blockade regions under different gate voltages near zero-bias. They correspond directly to the energy diagram in Figure 2A, with both MO levels above/below the Fermi energy for region '1'/'5', respectively, and with the electrostatic potential of the leads sandwiched between the two MO levels for region '3', *i.e.*, the bias window sits within the energy gap between the two MOs. This creates the diamond-shaped Coulomb blockade region trapped within a ~100 mV bias voltage range which corresponds to the energy difference between the two MOs ($\Delta MOs = \varepsilon_1 - \varepsilon_2$), as marked by the crossing of the ε_1 and ε_2 resonance boundaries. The computed electron transmission spectrum (Ts) overlaid in Figure 2A (state '5') is the zero-bias Ts of the molecular junction calculated by DFT-NEGF method (see SI-S3 (2) for details). The energy difference between the two Ts peaks describes the calculated *ΔMOs*, which is about 110 meV in good agreement with the measurements and is robust even for different conformations of the molecule and different electrode distances in the SET (see SI-**Figure S5** and **Figure S6**). The narrow widths of the peaks represent the small broadenings of the MOs, ensuring small currents in the Coulomb blockade region. Due to the asymmetry of the -$(CH_2)_9$-

and -$(CH_2)_3$- linkers, the molecule–electrode couplings under positive and negative biases are different, resulting in different extensions of the Ts peaks. Consequently, the background (blockade) current under negative bias voltage is higher than at positive bias (as seen in Figure 2B and C, corresponding to the measured and calculated current maps, respectively). In addition, no Kondo effect was observed in the experiment and the molecule should be in the ground state (S = 0) (see SI-S12). DFT calculations show the spin degeneracy of the ground state molecule in the absence of magnetic field. For convenience of Helium-3 cryostat, the experiments were performed at temperatures below 4.2 K (mainly 225 mK) and the measured current is independent with the temperature. In our previous work[25], where similar molecules were studied, a clear edge between the resonance regime and the Coulomb blockade regime can persist up to 120 K.

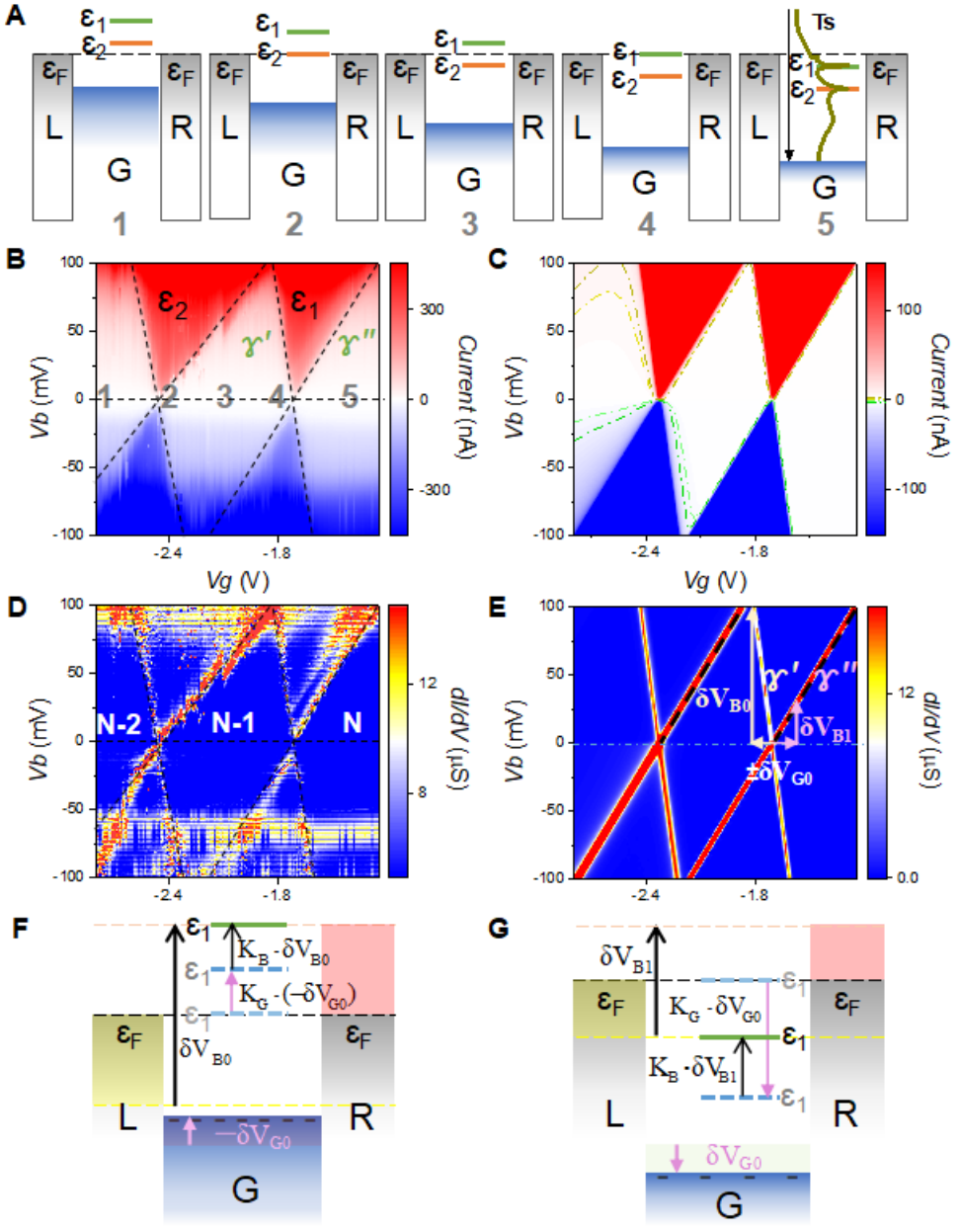


Figure 2. The current modulation of SELC. (**A**) Schematic diagrams of the shift of MOs manipulated by the gate voltage at zero-bias. The Ts of state '5' indicates that the conductive MOs (ε_1: HOMO-1, ε_2: HOMO-2) are below the Fermi energy when *Vg* is close to zero. At charge points '2' and '4', ε_1 and ε_2 are respectively aligned with the Fermi level of the electrodes. (**B**) Measured current map at 225 mK with *Vb*: 231 × *Vg*: 231 points. The red/blue colors indicate positive/negative resonance currents, respectively. The numbers correspond to the diagrams in (A). ε_1 and ε_2 resonance regions correspond to the MOs. (**C**) Calculated current map with *Vb*: 101 × *Vg*: 142 points. The background pattern (marked by the dashed contour lines) is contributed by the extension of transmission peaks. (**D**) Measured differential conductance map highlighting the edges between resonance and Coulomb blockade regimes. 'N-2', 'N-1' and 'N' indicate the number of fully occupied MOs. (**E**) The calculated differential conductance map. $-\delta V_{G0}$ and $+\delta V_{G0}$ indicate charging and discharging of the Gate. δV_{B0} and δV_{B1} indicate the increase of *Vb* from 0 V to *r'* and *r''* edges, respectively. (**F** and **G**) schematically show how the energy of ε_1 MO modulated by *Vb* and *Vg* aligns with the Right and Left electrode Fermi levels. The light blue dashed line indicates the initial energy of ε_1. The dark blue dashed line indicates the energy of ε_1 when *Vg* changes ((F) $-\delta V_{G0}$ or (G) $+\delta V_{G0}$). The green line indicates the final energy of ε_1 after adding the change of *Vb* (δV_{B0} or δV_{B1}). K_B and K_G are the energy change rates.

Due to the monotonic evolution of the energy eigenvalues of MOs under bias and gate voltages[17,39,46], we developed a theoretical model to describe the energy change rates (K_B and K_G) of MOs, which are directly related to the molecular dipole moments along the directions of voltages (see SI-S3 (1) for details). Thus, K_B and K_G can be calculated by the shift rates of Ts under bias and gate voltages, respectively (see SI-S3 (3))[38-39]. However, K_B, K_G and the MO energy shift (*MOs Shift*) are directly related to the configuration and background electrostatic potential of the molecular junction. Thus, to understand the junction configuration in the experiment, we calculated 12 different configurations for the 3-terminal molecular junction of the same molecule (see SI-S3 (4)) and analyzed their corresponding K_B, K_G, *ΔMOs* and *MOs Shift* values (see SI-S3 (5) **Table S1**). The data show that *ΔMOs* remains near constant (~110 meV) for the different configurations, in line with the experimental observations and proving that the Coulomb region lies stably within a well-defined and easily accessed bias voltage range (see SI-S4) despite the potentially shifted current maps for different junction configurations. Indeed, the experimental K_B and K_G can be extracted from the slopes of *r'* and *r''* edges for both MO resonance regions[17] as (see SI-S3 (5) for details): $K_B = (r'+r'')/2(r'-r'')$, $K_G = -r'r''/(r'-r'')$. Figure 2F and G illustrate the combined modulation of the shifts of ε_1 energy level in terms of the energy change rates K_B and K_G.

The corresponding DFT-NEGF calculated current and differential conductance (*dI/dV*) maps

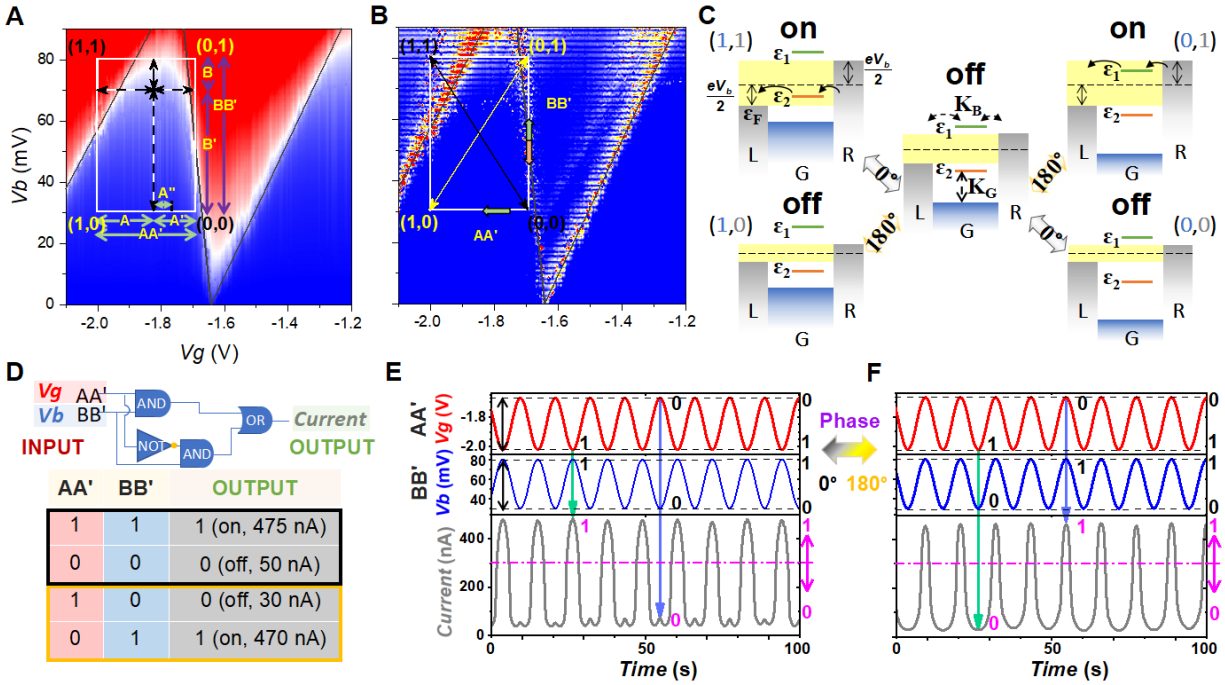
of the junction (see SI-S3 (6)) are shown in Figure 2C and E, respectively. The Ts not only reproduces the asymmetric background of Coulomb blockade regions under bias reversal, but also resolves the different widths of the *r'* and *r"* edges (see Figure 2E and D), which can be understood by the directional shift of the Ts towards the bias window controlled by the gate voltage (note the asymmetric Ts peaks in Figure 2A-5, discussed in SI-S3 (6)). Since the K_B and K_G values correspond directly to the electronic structure of the conductive MOs, it reflects the dipole moments of each MO. Therefore, the similarity of experimental and theoretical calculations on the parallel evolution of the two MOs along the gate voltage (see Figure S6) is a good proof that there is only one molecule in the junction. If the two resonance regions are provided by two independent molecules, then the slopes of their corresponding edges will not be parallel to each other due to the different dipole moments at different attachment positions within the gap. Thus, the agreement between the theoretical calculations and experimental measurements (data for different Fc-based SETs are shown in SI-S8) strongly demonstrates that the electrostatic modulation of the two conductive MOs of the Fc moiety provides a two-state Coulomb blockade region at *Vb*=1~100 mV. The differences between the theoretical current map (Figure 2C) and the measured results (Figure 2B) are due to the fact that the effect of the gate voltage field on the molecular configuration, the leaking currents through the gate to source/drain, and the inelastic electron tunneling (IET) current of the molecule are not considered. As discussed in SI-S7, Figure 2B shows the current shift in the high gate voltage region ($|Vg| > 2.2$ V), which is caused by a small change in the molecular configuration under high gate electrostatic field. Furthermore, the current in the Coulomb blockade region of Figure 2B is > 0.1 nA (see SI-S11), while the blockade current in the theoretical case can reach 10^{-6} nA. Finally, the measured IET spectra and corresponding vibrational modes shown in SI-S9 also provide strong evidence that an individual molecule is responsible for the transport behavior.

3.2. Working principle of the resettable SELC

Using the two-state diamond-shaped Coulomb blockade feature provided by the two MOs, we establish SELC by using the current as Output signal, and the gate (Input1: *Vg*) and the bias (Input2: *Vb*) voltages as two orthogonal Input signals. **Figure 3** summarizes the working principle of our SELC. Figure 3A shows the detailed current map. Four input ranges of *Vg* and three of *Vb* are determined based on the current oscillation signal (see SI-S5) across the Coulomb diamond region, labelled A (-1.82 V '0' to -2.02 V '1'), A' (-1.67 V '0' to -1.82 V '1'), A" (-1.77 V '0' to -1.82 V '1'), AA' (-1.67 V '0' to -2.02 V '1') and B (70 mV '0' to 80 mV '1'), B'

(30 mV '0' to 70 mV '1'), BB' (30 mV '0' to 80 mV '1'). The (1, 1) input represents the *Vg* and *Vb* both at high states in their own ranges, which is opposite to the (0, 0) input, for instance. Correspondingly the (1, 0) input means that the *Vg* is at high state while the *Vb* is at low state, opposite to the (0, 1) input. The current (Output) is represented by the color code in the map, red indicating high current state (>300 nA, 'on', '1') and blue the low current state (<300 nA, 'off', '0). The white rectangles indicate logic operation areas, defined by two orthogonal input ranges (*i.e.*, one *Vg* range and one *Vb* range). The horizontal/vertical black dashed arrows represent the operating ranges of the gate/bias voltage under a particular bias/gate voltage.

We take the 2-input logic operation along AA' and BB' as an example to introduce the working principle of the logic gates within a set operating area. Figure 3B is the corresponding logic diagram in the differential conductance map. The arrows in the white rectangle illustrate how *Vg* and *Vb* are combined to govern the current switching across the edges of the resonance and Coulomb blockade regions. The black arrow indicates that the changes of *Vg* (along the short-green-left arrow of AA') and *Vb* (along the short-green-up arrow of BB') are in the same phase (0º). The corresponding multi-cycle logic input and output signals are shown in Figure 3E. As the input gate signal and input bias signal change in phase from (0, 0) to (1, 1), the signal of output current changes from '0' (off) to '1' (on). Thus, high *Vg* and high *Vb* inputs (1,1) lead to high output current '1', while low *Vg* and low *Vb* inputs (0,0) lead to low output current '0'. However, when the change of *Vg* (along the short-green-left arrow of AA') and *Vb* (along the short-orange-down arrow of BB') are out of phase (180º), the logic operation changes (Figure 3F). In this case, as *Vg* and *Vb* change from (0, 1) to (1, 0), output current changes from '1' (on) to '0' (off).



AA'	BB'	OUTPUT
1	1	1 (on, 475 nA)
0	0	0 (off, 50 nA)
1	0	0 (off, 30 nA)
0	1	1 (on, 470 nA)

Figure 3. Logic calculation based on resonance excitations of MOs. (**A**) Measured 231 × 231 points current map at 225 mK marked with logic operating voltage-ranges. A, A', A'', AA' and B, B', BB' are the voltage-ranges of input-gate and input-bias, respectively. White rectangles mark 2-input logic operation areas. Input (1, 1) means high-gate and high-bias voltages, (0, 0) is the opposite case. Input (1, 0) means high-gate and low-bias voltages, (0, 1) is the opposite. (**B**) Differential conductance map corresponding to (A). Input AA'-BB' is an example to illustrate how gate (*Vg*) and bias (*Vb*) voltages are combined to achieve logic operations. The black arrow goes from (0, 0) to (1, 1), when *Vg* and *Vb* both change along the short green arrows. The yellow arrow goes from (0, 1) to (1, 0), when *Vb* and *Vg* change along the short orange and green arrows, respectively. (**C**) The schematic diagrams describe the energy level distributions of the four input cases in (B). Phase 0° and 180° correspond to the black and yellow arrow, respectively. (**D**) Equivalent logic circuit and truth table with AA'-BB' inputs at 0° and 180° phases. (**E** and **F**) show the curves of input *Vg* and *Vb* and measured output current at 0° and 180°, respectively.

Figure 3C schematically shows the energy distributions of MOs (ε_1 and ε_2) under the voltages indicated by black and yellow arrows in Figure 3B. The two orthogonal inputs switch the output current by shuttling the MOs in and out of the bias window. The central diagram corresponds to the intersection of the arrows. The four diagrams on the corners correspond to the four terminals of the arrows (1,1), (0,0), (1,0) and (0,1). The top two diagrams show the resonance states, where ε_1 or ε_2 is in the bias window, generating high-current "on" states (>300 nA, output=1). The rest belong to the Coulomb blockade regime, with no MO in the bias window. They correspond to low-current "off" states (<300 nA, output=0). This logic operation is illustrated in the truth table in Figure 3D and repeated for several cycles in Figure 3E, F to show the stability of SELC. Note that the signal remained stable throughout the whole experiment

for about 2 months, even independent of the scan rate variation of the input signal, see SI-**Figure S12**. At least 37 cycles were taken for each curve, see SI-**Figure S11**; for illustrative purposes only 9 cycles (40 points per cycle) are shown in Figure 3. The result of this logic operation can be interpreted as a complex logic gate array of one "INH" gate (inhibit) and one "AND" gate feeding their outputs into an "OR" gate. In this logic operation, SELC acts as a high-bias voltage indicator, *i.e.*, a high-bias input produces a high-current output, while a low-bias input produces a low-current output. The on/off ratio of high and low output currents is ~10.

3.3. SELC 1-input logic gates

For the 1-input logic gates, *Vg* is the only input, current is the output, and *Vb* is fixed at 70 mV. **Figure 4**A shows *Vg* ranges A and A' for 1-input logic gates "YES" and "NOT", respectively. Figure 4B, C show corresponding electronic symbols, truth tables and Input/Output signals. The 1-input "YES" logic gate is based on current switching between the ε_2 resonance regime and the Coulomb blockade region. In this case, the high *Vg* ('1', -2.02 V) leads to resonance conductance of ε_2 MO, resulting in high current ('1', ~410 nA). The low *Vg* ('0', -1.82 V) reduces the energy of ε_2 MO and moves it out of the bias window, resulting in current blockade ('0', ~120 nA). Thus, high-input leads to high-output and low-input leads to low-output, "YES" logic. Conversely, for the 1-input "NOT" logic gate the operation is based on current switching between the Coulomb blockade region and the ε_1 resonance regime. In this case, at the high *Vg* ('1', -1.82 V) no MO lies in the bias window, so the current is in the blockade region ('0', ~120nA). The low *Vg* ('0', -1.67 V) further reduces the energy of MOs and shifts ε_1 into the bias window, so the current is in the resonance region ('1', ~410 nA). Thereby, high-input leads to low-output and low-input leads to high-output, "NOT" logic.

Figure 4D shows the *Vg* ranges AA' and A" for 1-input logic gates "PASS 1" and "PASS 0", respectively. According to the discussion above, the 1-input "PASS 1" logic gate involves current switching between ε_2 and ε_1 resonance regimes. Both high and low inputs led to high outputs, "PASS 1" logic. Since the switching process of the output current spans the entire Coulomb blockade region, the frequency of the output current signal is doubled compared with the input gate signal. This interesting feature can be used as a frequency multiplier. The current signal is also used as an address for the logic operations to define the Coulomb diamond region, which provides important information for calibrating the *Vg* ranges (see SI-S5 for details). By contrast, the 1-input "PASS 0" logic gate is based on the stability of the blockade current. In this case, at both high ('1', -1.82 V) and low ('0', -1.77 V) *Vg*, the two MOs are distributed on

both sides of the bias window (as shown in Figure 3C-'off'), so the output current is in the Coulomb blockade region ('0', ~120 nA) contributed by the extension between the two transmission peaks of Ts (shown as Figure 2A '5'). High-input and low-input both lead to low-outputs, "PASS 0" logic.

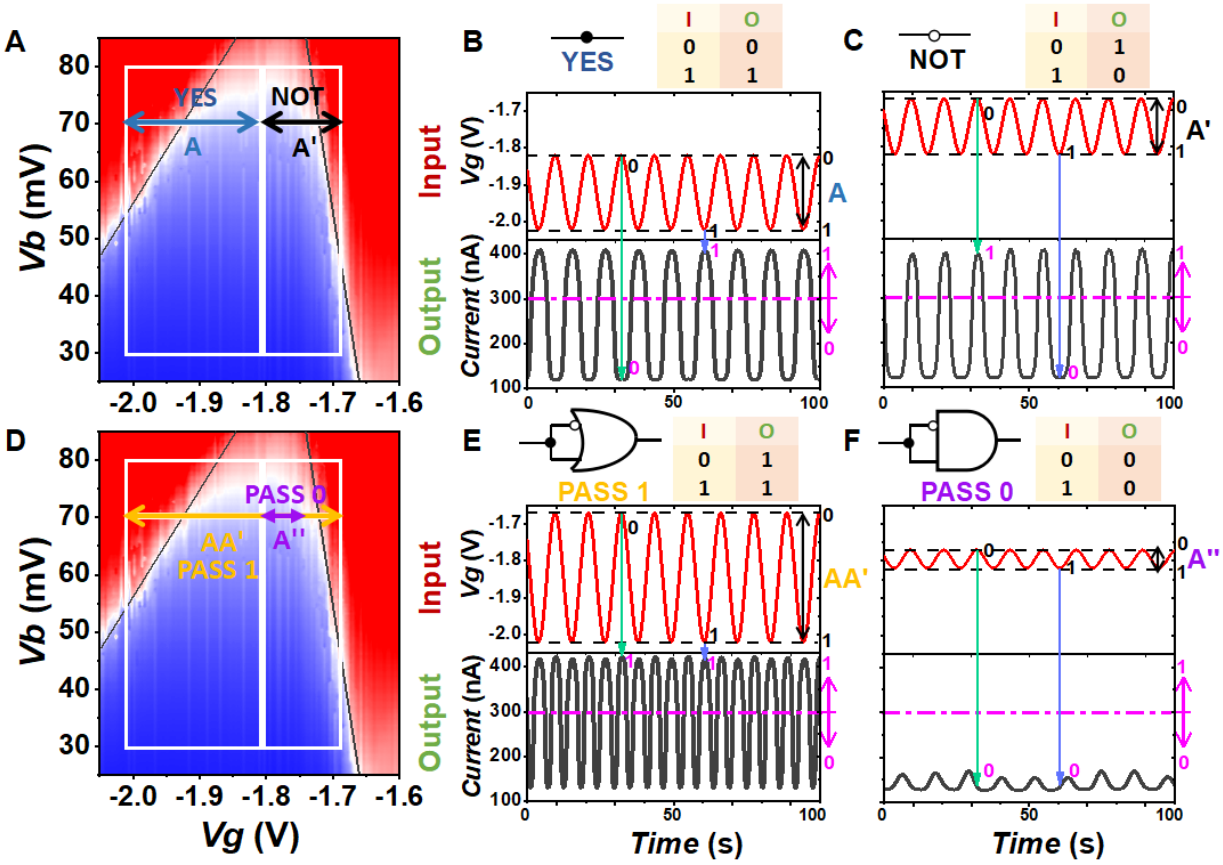


Figure 4. Four resettable universal 1-input logic gates. In (**A** and **D**), input gate voltages with A, A', AA' and A'' ranges are marked on the current maps, which indicate 1-input "YES", "NOT", "PASS 1" and "PASS 0" logic gates. (**B**) Equivalent circuit, truth table and corresponding Input/Output signal for 1-input "YES" gate. With the gate voltage change from -2.02 V '1' to -1.82 V '0', the current changes from 410 nA '1' to 120 nA '0'. (**C**) For 1-input "NOT" gate, with gate voltage change from -1.82 V '1' to -1.67 V '0', the current changes from 120 nA '0' to 405 nA '1'. (**E**) For 1-input "PASS 1" gate, with the gate voltage change from -2.02 V '1' to -1.67 V '0', the current changes from 410 nA '1' to 405 nA '1'. The frequency of the current signal is doubled compared with the input gate signal. (**F**) For 1-input "PASS 0" gate, with the gate voltage change from -1.82 V '1' to -1.77 V '0', the current changes from 120 nA '0' to 130 nA '0'. All 1-Input logic gates operate at 70 mV bias.

3.4. SELC 2-input logic gates

Based on the gate voltage ranges of the 1-input logic gates, bias voltage control is added, so that all seven universal 2-input logic gates can be realized, as demonstrated in **Figure 5**. In the 2-input logic gates, gate voltage is Input-signal 1 and bias voltage is Input-signal 2. The main

difference between the operation of 2-input and 1-input logic gates is the phase control. The 2-input logic gate contains two input signals, and the phase difference between them determines the moving direction of the MOs relative to the bias window, thereby affecting the state of the output current. Thus, phase control combined with different operating voltage makes it possible to realize all 2-input universal logic gates.

Figure 5A shows the 2-input "AND" gate. Its operation area is defined by A-B' in both 0° and 180° phases. The input ranges of *Vg* and *Vb* are shown on the current map. The graphs on the right are the Input/Output signals in 0° and 180° phases, respectively. In 0° phase, by changing *Vg* (Input-1, red curve) from -2.02 V '1' to -1.82 V '0' (range A) and changing *Vb* (Input-2, blue curve) from 70 mV '1' to 30 mV '0' (range B'), the current (Output, grey curve) changes from 400 nA '1' to 25 nA '0', *i.e.*, (1,1) → 1, (0, 0) → 0. In 180° phase, as *Vg* changes from '1' to '0' (A) and *Vb* changes from '0' to '1' (B'), the current changes from 40 nA '0' to 120 nA '0', *i.e.*, (1,0) → 0, (0,1) → 0. "AND" gate works as a Carry in a Half-adder logical circuit that performs an addition operation on two binary digits.

Figure 5B shows the "INH" gate. Its operation area is defined by A'-B' in both 0° and 180° phases. In 0° phase by changing *Vg* from -1.82 V '1' to -1.67 V '0' (range A') and changing *Vb* from 70 mV '1' to 30 mV '0' (range B'), the current changes from 120 nA '0' to 50 nA '0', *i.e.*, (1,1) → 0, (0,0) → 0. In 180° phase, by changing *Vg* from '1' to '0' (A') and changing *Vb* from '0' to '1' (B'), the current changes from 25 nA '0' to 420 nA '1', *i.e.*, (1,0) → 0, (0,1) → 1. It works as a Borrow in Half-subtractor.

Figure 5C and D show the "XOR" and "XNOR" gates, respectively. They have different input voltage ranges in different phases. For the "XOR" gate in 0° phase, as *Vg* changes from -1.82 V '1' to -1.67 V '0' (A') and *Vb* changes from 80 mV '1' to 30 mV '0' (BB'), current changes from 230 nA '0' to 75 nA '0', *i.e.*, (1,1) → 0, (0,0) → 0. At 180° phase, as *Vg* changes from -2.02 V '1' to -1.67 V '0' (AA') and *Vb* changes from 70 mV '0' to 80 mV '1' (B), current changes from 400 nA '1' to 480 nA '1', *i.e.*, (1,0) → 1, (0,1) → 1. Notably, the input gate voltage and bias voltage in both phases have the same minimum value of -1.67 V and the same maximum value of 80 mV, respectively. This means that only the amplitudes of the input voltage ranges are changed with the phase. It works as a Sum in Half-adder and Diff. in Half-subtractor. For the "XNOR" gate, with AA' and B inputs in 0° phase, current changes from 480nA '1' to 420 nA '1', *i.e.*, (1,1) → 1, (0,0) → 1. In 180° phase, the corresponding inputs are A and BB', and current changes from 25 nA '0' to 200 nA '0', *i.e.*, (1,0) → 0, (0,1) → 0. The input gate voltage and bias voltage in both phases have the same maximum value of -2.02 V and 80 mV, respectively.

Figure 5E, F and G show the "NAND", "NOR" and "OR" gates. These three logic gates have

the same bias voltage range in both phases, only the gate voltage range changes with phase. To avoid repetition, we omitted the curves of the input signals and kept only the input voltage range and Boolean states. For “NAND” gate, the inputs in 0° phase are A’ for *Vg* and B for *Vb*. The current changes from 200 nA '0' to 420 nA '1', *i.e.*, (1,1) → 0, (0,0) → 1. The inputs in 180° phase are AA’ and B. The current changes from 400 nA '1' to 480 nA '1', *i.e.*, (1,0) → 1, (0,1) → 1. For “NOR” gate, the Input/Output signal in 0° phase are the same with “NAND” gate (A’-B), *i.e.*, (1,1) → 0, (0,0) → 1. The inputs in 180° phase are A” and B. The current changes from 120 nA '0' to 210 nA '0', *i.e.*, (1,0) → 0, (0,1) → 0. For “OR” gate, the inputs in 0° phase are A for *Vg* and B for *Vb*. The current changes from 480 nA '1' to 120 nA '0', *i.e.*, (1,1) → 1, (0,0) → 0. In 180° phase, the input ranges are AA’ and B, the same as “NAND” and “XOR” gates, *i.e.*, (1,0) → 1, (0,1) → 1. To clearly show the relationship between the input and output signals, two cycles are shown in Figure 5. The multi-cycle output curves for the 2-input logic gates are shown in SI-S6 **Figure S10**.

From Figure 5 it is clear that SELC can realize all the universal 2-input logic gates within one gated single-molecule junction, in contrast to conventional CMOS (see SI-S10). It allows dynamic logic circuits to be scaled down to a few nanometers, and the single-junction design greatly reduces charge leakage, charge sharing, and back-gate coupling between devices. Crucially, only a 2 V gate voltage (CMOS is in the 3-15 V range) and 100 mV drive voltage (well below the 1.5-5 V of CMOS) are required to run the SELC.

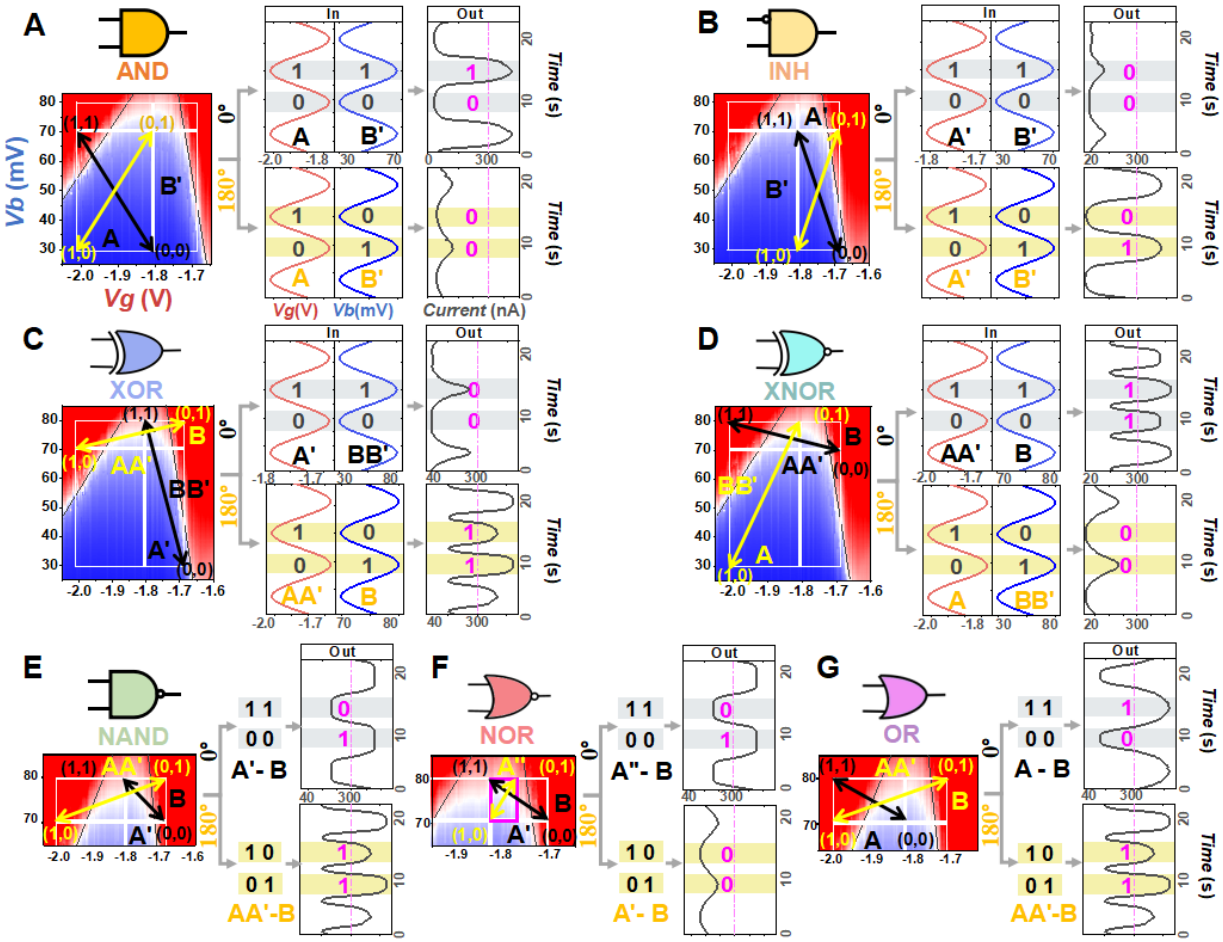


Figure 5. Seven resettable universal 2-Input logic gates. (**A** and **B**) "AND" and "INH" logic gates with A-B' and A'-B' inputs in both phases, respectively. The black and yellow arrows in current map are corresponding to the Input/Output signals in 0° phase and 180° phase, respectively. (**C**) "XOR" logic gate with A'-BB' input in 0° phase and AA'-B input in 180° phase. The input gate voltages in both phases have the same minimum value and the input bias voltages in both phases have the same maximum value, *i.e.*, the (0,1) point is the same in the voltage ranges in both phases. The highest gate voltage and the lowest bias voltage (*i.e.*, the (1,0) point) from 0° phase to 180° phase is changed. (**D**) "XNOR" logic gate with AA'-B input in 0° phase and A-BB' input in 180° phase. The input gate and bias voltages in both phases have the same maximum value, *i.e.*, the (1,1) point is the same in the voltage ranges in both phases. The lowest gate voltage and the lowest bias voltage (*i.e.*, the (0,0) point) from 180° phase to 0° phase is changed. (**E**, **F** and **G**) "NAND", "NOR" and "OR" logic gates have the same input bias voltage range in both phases and change the gate voltage range with phase only. "NAND" has A'-B input in 0° phase and AA'-B input in 180° phase. "NOR" has A'-B input in 0° phase and A"-B input in 180° phase. "OR" has A-B input in 0° phase and AA'-B input in 180° phase.

4. Conclusion

We report molecular-scale SELC in a three-terminal SET by utilizing adjacent conductive MOs provided by a single Fc-based molecule. Its operating principle is based on predictable and reliable current conversions modulated by voltages crossing the stable Coulomb blockade regime, avoiding dependence on absolute current and improving function reproducibility.

Compared with other approaches[24,26-27,32-33,57], the non-conjugated asymmetric Fc-based molecule naturally provides logic operations via its robust and unique Coulomb blockade characteristics. The isolation provided by the asymmetric n-alkyl (n>3) linkers on either side of the Fc moiety ensures narrow MO levels, efficiently suppressing current in the Blockade regime and enabling encoding of information via orthogonal modulation for the realization of sophisticated operation functions. This results in clear and multi-cycle stable current signals controlled by two orthogonal electrostatic fields, enabling in-situ implementation of all four universal 1-input and all seven universal 2-input logic gates in a single molecule with high stability. Through phase control of an external circuit, the benefits of implementing multiple logic operations within a single molecule (instead of connecting several separate devices with switching characteristics in series) are low charge leakage, with no mutual interference, small functional area (~2 nm), low operating voltage (because the applied potential only drops over one element[5]) and simple device construction. Crucially, our design can be extended to multi-channel mesoscopic Coulomb blockade systems, field-effect single molecules or molecular layers, with promising future applications of SELC in realizing multifunctional nanodevices including frequency multipliers, diodes, switches, voltage indicators, and calculators, among others.

5. Methods

Synthesis of the molecule: We followed a previously reported procedures[16,25,58] to synthesize and characterize AcS-$(CH_2)_3$-Fc-$(CH_2)_9$-SAc and AcS-$(CH_2)_6$-Fc-$(CH_2)_6$-SAc as described in SI-S1.

Sample preparation for SELCs: The previously reported method[25] was followed to fabricate the chip with nanowires and back-gates, as presented in SI-S2. After the chip has been properly fabricated, it is immersed into the diluted molecular solution (dissolved in ethanol) for about 30–40 minutes to allow the molecules to adsorb to the surface of the gold nanowire. The chip is then gently washed several times with the molecular solution, then washed with ethanol and blow dried with N_2 to remove excess molecular solution to ensure that the remaining molecules were firmly attached to the gold surface. We mounted the chip on the chip holder in a home-made probing box, which can be used for current feedback-controlled electromigration, to narrow the nanowire into single-atom-contact nanoelectrodes (see SI-S2 **Figure S3**). The whole process was carried out in a nitrogen-filled environment at room temperature and pressure. After the nanoelectrodes formed, the chip was transferred to a Helium-3 cryostat for measurements at low temperature. The base temperature of the cryostat (225 mK) was used for convenience, as these

measurements could be done at LN_2 temperatures[25].

The current measurements: The current through the SELC as a function of bias and gate voltages was measured via a Keithley 6430 Source Meter by applying the bias voltage on the Au electrodes in DC. The gate voltage was applied through the Al_2O_3/Al gate and controlled by a Keithley 2400. The SELCs were mounted on the chip holder in a vacuum tube and placed in vacuum inside the sample holder of the Helium-3 cryostat.

DFT-NEGF calculations: The transmission spectra (Ts) of different structures of the Al_2O_3/Al gated Au/S$(CH_2)_3$Fc$(CH_2)_9$S/Au junction were calculated using the DFT-NEGF method implemented in the Atomistix ToolKit (ATK)[59] package (see SI-S3 (2) for details). Based on these Ts, the theoretical modulation parameters of the molecular orbitals (MOs) of different structures by the bias voltage and the gate voltage were calculated (see SI-S3 (3) for details). The mechanisms of the modulation were defined by the theoretical model (see SI-S3 (1) for details). The comparison between measured parameters and calculated parameters is shown in Table S1 (see SI-S3 (4)). The calculated current map is drawn by integrating Ts as a function of bias voltage and gate voltage. The values of K_B, K_G and *MOs Shift* in Exp.1 in SI-Table S1 are used in the integration. The Ts under positive bias and negative bias are represented by Ts calculated at 100 mV and -100 mV, respectively (see SI-S3 (6) for details).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no competing financial interests.

Acknowledgments

R.L. and E.d.B. acknowledge support from the National Science Foundation (grants NSF-ECCS #1402990 and #1518863). C.A.N. acknowledges support from the National Research Foundation, Prime Minister's Office, Singapore under its Medium-Sized Centre programme, and the NRF fellowship award No. NRF-RF 2010-03. Singapore Ministry of Education (MOE) for supporting this research under award No. MOE2015-T2-1-050. D.T. acknowledges support from Science Foundation Ireland (SFI) under award number 12/RC/2275_P2. Z.L.L. and C.K.W. acknowledge support from the National Natural Science Foundation of China (grants No.11974217 and No. 11874242).

Received: ((will be filled in by the editorial staff))
Revised: ((will be filled in by the editorial staff))
Published online: ((will be filled in by the editorial staff))

References

[1] X. Chen, M. Roemer, L. Yuan, W. Du, D. Thompson, E. Del Barco, C. A. Nijhuis, *Nat Nanotechnol* **2017**, 12, 797.

[2] C. Guo, K. Wang, E. Zerah-Harush, J. Hamill, B. Wang, Y. Dubi, B. Xu, *Nat Chem* **2016**, 8, 484.

[3] C. Jia, A. Migliore, N. Xin, S. Huang, J. Wang, Q. Yang, S. Wang, H. Chen, D. Wang, B. Feng, Z. Liu, G. Zhang, D.-H. Qu, H. Tian, M. A. Ratner, H. Q. Xu, A. Nitzan, X. Guo, *Science* **2016**, 352, 1443.

[4] S. Kumar, M. Merelli, W. Danowski, P. Rudolf, B. L. Feringa, R. C. Chiechi, *Adv Mater* **2019**, 31, e1807831.

[5] Y. Han, C. Nickle, Z. Zhang, H. Astier, T. J. Duffin, D. Qi, Z. Wang, E. Del Barco, D. Thompson, C. A. Nijhuis, *Nat Mater* **2020**, 19, 843.

[6] L. Bogani, W. Wernsdorfer, *Nat Mater* **2008**, 7, 179.

[7] S. Cai, W. Deng, F. Huang, L. Chen, C. Tang, W. He, S. Long, R. Li, Z. Tan, J. Liu, J. Shi, Z. Liu, Z. Xiao, D. Zhang, W. Hong, *Angew Chem Int Ed Engl* **2019**, 58, 3829.

[8] W. H. Soe, C. Manzano, A. De Sarkar, F. Ample, N. Chandrasekhar, N. Renaud, P. de Mendoza, A. M. Echavarren, M. Hliwa, C. Joachim, *Physical Review B* **2011**, 83.

[9] C. Joachim, N. Renaud, M. Hliwa, *Adv Mater* **2012**, 24, 312.

[10] N. Zhang, W. Y. Lo, A. Jose, Z. Cai, L. Li, L. Yu, *Adv Mater* **2017**, 29.

[11] F. Meng, Y. M. Hervault, Q. Shao, B. Hu, L. Norel, S. Rigaut, X. Chen, *Nat Commun* **2014**, 5, 3023.

[12] Y. Liu, A. Offenhausser, D. Mayer, *Angew Chem Int Ed Engl* **2010**, 49, 2595.

[13] P. Gehring, J. M. Thijssen, H. S. J. van der Zant, *Nature Reviews Physics* **2019**, 1, 381.

[14] S. Goswami, S. P. Rath, D. Thompson, S. Hedstrom, M. Annamalai, R. Pramanick, B. R. Ilic, S. Sarkar, S. Hooda, C. A. Nijhuis, J. Martin, R. S. Williams, S. Goswami, T. Venkatesan, *Nat Nanotechnol* **2020**, 15, 380.

[15] W. Du, T. Wang, H.-S. Chu, C. A. Nijhuis, *Nature Photonics* **2017**, 11, 623.

[16] L. Yuan, N. Nerngchamnong, L. Cao, H. Hamoudi, E. del Barco, M. Roemer, R. K. Sriramula, D. Thompson, C. A. Nijhuis, *Nat Commun* **2015**, 6, 6324.

[17] H. Song, Y. Kim, Y. H. Jang, H. Jeong, M. A. Reed, T. Lee, *Nature* **2009**, 462, 1039.

[18] S. Zhang, C. Guo, L. Ni, K. M. Hans, W. Zhang, S. Peng, Z. Zhao, D. C. Guhr, Z. Qi, H. Liu, M. Song, Q. Wang, J. Boneberg, X. Guo, T. Lee, E. Scheer, D. Xiang, *Nano Today* **2021**, 39.

[19] H. Park, J. Park, A. K. L. Lim, E. H. Anderson, A. P. Alivisatos, P. L. McEuen, *Nature* **2000**, 407, 57.

[20] J. Park, A. N. Pasupathy, J. I. Goldsmith, C. Chang, Y. Yaish, J. R. Petta, M. Rinkoski, J. P. Sethna, H. D. Abruna, P. L. McEuen, D. C. Ralph, *Nature* **2002**, 417, 722.

[21] W. Liang, M. P. Shores, M. Bockrath, J. R. Long, H. Park, *Nature* **2002**, 417, 725.

[22] S. J. van der Molen, J. Liao, T. Kudernac, J. S. Agustsson, L. Bernard, M. Calame, B. J. van Wees, B. L. Feringa, C. Schonenberger, *Nano Lett* **2009**, 9, 76.

[23] J. Zhou, K. Wang, B. Xu, Y. Dubi, *J Am Chem Soc* **2018**, 140, 70.

[24] L. Yuan, L. Wang, A. R. Garrigues, L. Jiang, H. V. Annadata, M. Anguera Antonana, E. Barco, C. A. Nijhuis, *Nat Nanotechnol* **2018**, 13, 322.

[25] A. R. Garrigues, L. Wang, E. Del Barco, C. A. Nijhuis, *Nat Commun* **2016**, 7, 11595.

[26] P. Gehring, J. K. Sowa, C. Hsu, J. de Bruijckere, M. van der Star, J. J. Le Roy, L. Bogani, E. M. Gauger, H. S. J. van der Zant, *Nat Nanotechnol* **2021**, 16, 426.

[27] S. Kubatkin, A. Danilov, M. Hjort, J. Cornil, J. L. Bredas, N. Stuhr-Hansen, P. Hedegard, T. Bjornholm, *Nature* **2003**, 425, 698.

[28] P. Gehring, J. K. Sowa, J. Cremers, Q. Wu, H. Sadeghi, Y. Sheng, J. H. Warner, C. J. Lambert, G. A. D. Briggs, J. A. Mol, *ACS Nano* **2017**, 11, 5325.

[29] P. Puczkarski, P. Gehring, C. S. Lau, J. Liu, A. Ardavan, J. H. Warner, G. A. D. Briggs, J. A. Mol, *Applied Physics Letters* **2015**, 107.

[30] P. Gehring, M. van der Star, C. Evangeli, J. J. Le Roy, L. Bogani, O. V. Kolosov, H. S. J. van der Zant, *Applied Physics Letters* **2019**, 115.

[31] P. Gehring, H. Sadeghi, S. Sangtarash, C. S. Lau, J. Liu, A. Ardavan, J. H. Warner, C. J. Lambert, G. A. Briggs, J. A. Mol, *Nano Lett* **2016**, 16, 4210.

[32] S. Caneva, M. Hermans, M. Lee, A. Garcia-Fuente, K. Watanabe, T. Taniguchi, C. Dekker, J. Ferrer, H. S. J. van der Zant, P. Gehring, *Nano Lett* **2020**, 20, 4924.

[33] P. Gehring, A. Harzheim, J. Spiece, Y. Sheng, G. Rogers, C. Evangeli, A. Mishra, B. J. Robinson, K. Porfyrakis, J. H. Warner, O. V. Kolosov, G. A. D. Briggs, J. A. Mol, *Nano Lett* **2017**, 17, 7055.

[34] D. Goldhaber-Gordon, H. Shtrikman, D. Mahalu, D. Abusch-Magder, U. Meirav, M. A. Kastner, *Nature* **1998**, 391, 156.

[35] J. J. Parks, A. R. Champagne, G. R. Hutchison, S. Flores-Torres, H. D. Abruna, D. C. Ralph,

549 *Phys Rev Lett* **2007**, 99, 026601.
550 [36] X. Guo, Q. Zhu, L. Zhou, W. Yu, W. Lu, W. Liang, *Nat Commun* **2021**, 12, 1566.
551 [37] B. Fu, M. A. Mosquera, G. C. Schatz, M. A. Ratner, L. Y. Hsu, *Nano Lett* **2018**, 18, 5015.
552 [38] S. Alavi, B. Larade, J. Taylor, H. Guo, T. Seideman, *Chemical Physics* **2002**, 281, 293.
553 [39] T. Seideman, H. Guo, *Journal of Theoretical and Computational Chemistry* **2003**, 02, 439.
554 [40] X. Wang, L. Cong, D. Zhu, Z. Yuan, X. Lin, W. Zhao, Z. Bai, W. Liang, X. Sun, G.-W.
555 Deng, K. Jiang, *Nano Research* **2020**, 14, 1156.
556 [41] S. J. Kim, J. J. Lee, H. J. Kang, J. B. Choi, Y. S. Yu, Y. Takahashi, D. G. Hasko, *Applied*
557 *Physics Letters* **2012**, 101.
558 [42] S. J. Shin, J. J. Lee, H. J. Kang, J. B. Choi, S. R. Yang, Y. Takahashi, D. G. Hasko, *Nano*
559 *Lett* **2011**, 11, 1591.
560 [43] M. El Abbassi, M. L. Perrin, G. B. Barin, S. Sangtarash, J. Overbeck, O. Braun, C. J.
561 Lambert, Q. Sun, T. Prechtl, A. Narita, K. Mullen, P. Ruffieux, H. Sadeghi, R. Fasel, M. Calame,
562 *ACS Nano* **2020**, 14, 5754.
563 [44] Q. Sun, O. Groning, J. Overbeck, O. Braun, M. L. Perrin, G. Borin Barin, M. El Abbassi,
564 K. Eimre, E. Ditler, C. Daniels, V. Meunier, C. A. Pignedoli, M. Calame, R. Fasel, P. Ruffieux,
565 *Adv Mater* **2020**, 32, e1906054.
566 [45] M. Camarasa-Gomez, D. Hernangomez-Perez, M. S. Inkpen, G. Lovat, E. D. Fung, X. Roy,
567 L. Venkataraman, F. Evers, *Nano Lett* **2020**, 20, 6381.
568 [46] G.-P. Zhang, Y.-Q. Mu, M.-Z. Wei, S. Wang, H. Huang, G.-C. Hu, Z.-L. Li, C.-K. Wang,
569 *Journal of Materials Chemistry C* **2018**, 6, 2105.
570 [47] S. Wang, M.-Z. Wei, G.-C. Hu, C.-K. Wang, G.-P. Zhang, *Organic Electronics* **2017**, 49,
571 76.
572 [48] X. Zhao, G. Kastlunger, R. Stadler, *Physical Review B* **2017**, 96.
573 [49] D. Thompson, C. A. Nijhuis, *Acc Chem Res* **2016**, 49, 2061.
574 [50] L. Cao, L. Yuan, M. Yang, N. Nerngchamnong, D. Thompson, X. Yu, D.-C. Qi, C. A.
575 Nijhuis, *Nanoscale Advances* **2019**, 1, 1991.
576 [51] B. Han, Y. Li, X. Ji, X. Song, S. Ding, B. Li, H. Khalid, Y. Zhang, X. Xu, L. Tian, H. Dong,
577 X. Yu, W. Hu, *J Am Chem Soc* **2020**, 142, 9708.
578 [52] C. Jia, I. M. Grace, P. Wang, A. Almeshal, Z. Huang, Y. Wang, P. Chen, L. Wang, J. Zhou,
579 Z. Feng, Z. Zhao, Y. Huang, C. J. Lambert, X. Duan, *Chem* **2020**, 6, 1172.
580 [53] H. Jeong, D. Kim, G. Wang, S. Park, H. Lee, K. Cho, W.-T. Hwang, M.-H. Yoon, Y. H.
581 Jang, H. Song, D. Xiang, T. Lee, *Advanced Functional Materials* **2014**, 24, 2472.
582 [54] J. J. Henderson, C. M. Ramsey, E. del Barco, A. Mishra, G. Christou, *Journal of Applied*

Physics **2007**, 101.

[55] R. Liu, J.-J. Bi, Z. Xie, K. Yin, D. Wang, G.-P. Zhang, D. Xiang, C.-K. Wang, Z.-L. Li, *Physical Review Applied* **2018**, 9.

[56] Q. Wang, R. Liu, D. Xiang, M. Sun, Z. Zhao, L. Sun, T. Mei, P. Wu, H. Liu, X. Guo, Z. L. Li, T. Lee, *ACS Nano* **2016**, 10, 9695.

[57] H. Song, M. A. Reed, T. Lee, *Adv Mater* **2011**, 23, 1583.

[58] A. Escorcia, A.-A. Dhirani, *Journal of Electroanalytical Chemistry* **2007**, 601, 260.

[59] M. Brandbyge, J.-L. Mozos, P. Ordejón, J. Taylor, K. Stokbro, *Physical Review B* **2002**, 65.

Table of Contents

Single-molecule logic devices are ideal candidates for ultra-minimalistic circuit elements to perform high-density computing. Gated Au/S-$(CH_2)_3$-Fc-$(CH_2)_9$-S/Au single-electron transistors not only hold the advantage of controlling molecular orbitals (MOs) via bias and gate voltages, but also exhibit a unique electronic structure with two adjacent MOs. This provides a Single-Electron Logic Calculator to implement all universal logic gates within a single-molecule device.

R. Liu, Y. Han, F. Sun, Z. L. Li, G. Khatri, J. Kwon, C. Nickle, L. Wang, C. K. Wang, D. Thompson, C. A. Nijhuis*, E. del Barco*

Stable Universal 1- and 2-Input Single-Molecule Logic Gates