

Hardware Implementation of High-Order PSK Modulation for MIMO Acoustic Modem Using Microcontrollers

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Abstract—This paper proposes a low-cost microcontroller (MCU) implementation of a high-order PSK modulation for MIMO acoustic modems with phase precoding. The multiple channels of high-order PSK modulation are achieved by using two cycles of a timer that has multiple pairs of control registers (TAxCCR0, TAxCCRn, and the output mode register), where TAxCCR0 determines the carrier frequency, TAxCCRn and the output mode register control the high-order PSK symbol modulation. The phase precoding of multiple transmission channels is achieved by setting different values on TAxCCRn for different transmit elements. If using Texas Instruments' microcontrollers MSP430F5529, the highest timer clock is $f_{clk} = 25$ MHz, the proposed scheme can reach a carrier frequency of $f_c = f_{clk}/(2mN)$ where m is the m -ary PSK modulation, and $N < 14$ is the number of transmit elements.

Index Terms—acoustic modem, high-order PSK, MIMO, frequency efficiency, low power

I. INTRODUCTION

Underwater acoustic (UWA) sensor networks play an important role in applications of Internet of Underwater Things (IoUT) and marine Cyber Physical Systems (CPS), such as environmental monitoring, undersea explorations, assisted navigation, and disaster prevention. Many of the IoUT devices are battery-powered and are deployed for long missions. However, the limitation of battery power and the inconvenience of battery charging constrain the lifetime and efficiency of UWA devices. The size and form factor of the existing UWA modem also limit the possible utility on systems with small dimensions. Therefore, it is desirable to design a UWA modem with small size and low cost while maximizing transmission rate and reliability [1].

UWA channels are extremely challenging because of their limited bandwidth, time-varying multipath fading, and large propagation delays [2] which result in low data transmission rates and high bit error rates. With limited bandwidth, High-order phase-shift keying (PSK) modulations and Multi-Input Multi-Output (MIMO) technology can increase the achievable data rate by improving spectral efficiency and channel capacity [3]–[5].

Microcontroller (MCU)-based modems have features of low-cost, low-power, and small form factor compared with DSP-based or FPGA-based modems, and are especially suitable for use in battery-powered underwater IoT devices deployed for long missions. In the past decades, many MCU-based acoustic modem designs have been proposed and sin-

gle channel transmission with frequency-shift keying (FSK) modulation or binary phase-shift keying (BPSK) modulation is studied in these design [6]–[9]. The application report [10] introduces the strategy to implement the BPSK modulation on TI MCU MSP432P401R, which uses one cycle of a timer to generate the carrier frequency on the PWM ports, and uses the output mode register to toggle the carrier phase based on the BPSK symbol value thus implementing the BPSK modulation. In recent studies, high-order PSK modulations and multi-input multi-output (MIMO) technology are implemented in FPGA-based and DSP-based software-defined modems in [11], [12], respectively.

This paper introduces hardware implementation of high-order PSK modulation MIMO acoustic modem based on low-cost microcontrollers. For high-order PSK modulation, more phase control of the carrier is required. For example, QPSK and 8PSK modulation schemes require four and eight phase levels in the carrier signal, respectively. Therefore, using the output mode register alone cannot implement PSK modulations other than BPSK. Our proposed method uses TAxCCR0 register to set the carrier frequency, and uses the output mode register and TAxCCRn register to control the carrier phase. We achieve it by selecting the output mode that only inverts the carrier voltage when the timer counts to the value stored in TAxCCRn. As a result, every two timer cycles generate one carrier cycle. The advantage of this approach is that the carrier phase can be controlled through TAxCCRn and the output mode register to implement high-order PSK modulation and phase precoding. The disadvantage is the loss of control of the duty cycle and the decrease of carrier frequency. But the carrier frequency can be compensated by reducing TAxCCR0 value or increasing the timer clock frequency. The contributions of this paper are:

- Utilizing two cycles of the MCU timer to implement high-order PSK modulation.
- Low-cost implementation of phase precoding for multiple transmit elements using the PWM ports.

A hardware prototype is designed to verify the high-order PSK MIMO transmission. The experimental results show that the proposed modem can successfully transmit multiple QPSK outputs with a carrier frequency of 115 kHz when using 8 MHz as the timer clock.

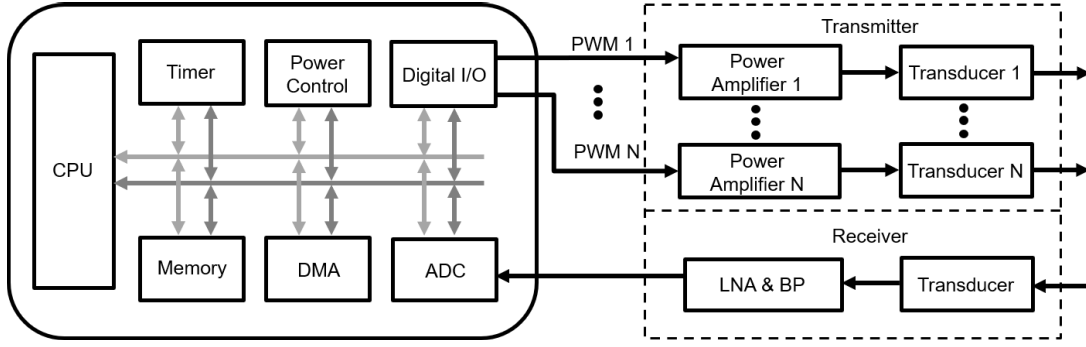


Fig. 1: Block diagram of the proposed UWA modem.

II. MCU-BASED ACOUSTIC MODEM DESIGN

MCU-based acoustic modems consists of three fundamental components as shown in Fig. 1: transducers, an analog front-end and a MCU platform for signal processing and control. The MCU utilizes the timer to modulate bits into carrier-modulated PSK waveforms and output to ports. The N -channel MIMO transmitter consists of multi-channel power amplifiers (PA) and transducers. The receiver consists of low noise amplifiers (LNA) and bandpass (BP) filters, and the received signals are fed into the analog-to-digital converters (ADC) of the MCU for subsequent digital processing.

A. Conventional BPSK Modulation

The application report [10] describes the implementation of conventional BPSK modulation on TI microcontrollers. Users can utilize timers in the MCU to periodically generate interrupts or Pulse Width Modulation (PWM) outputs. A counter is the fundamental hardware element inside the timer. With a clock input, the counter is incremented each time a clock pulse is applied. Therefore, the 16-bit counter in the timer is able to count from zero to 0FFFFh. $TxCCR0$ and $TxCCRn$ are two 16-bit registers that control the timer together with the counting mode register and the PWM output mode register. As shown in Table I, several different PWM output modes are available when using TI MSP430 MCU series. In different output modes, PWM output is controlled to be toggled/reset/set when the timer counts to $TxCCR0$ or $TxCCRn$. Therefore, these PWM output modes can conveniently generate opposite phase PWM waveforms with adjustable duty cycles and the opposite phase PWM wave can be considered as the carriers of BPSK modulation.

Fig. 2 shows the PWM output scheme of BPSK, where two 16-bit register values $TxCCR0$ and $TxCCRn$ are preset for the period of carrier frequency and duty cycle, respectively. Using the counting up mode, the timer repeatedly counts from 0 up to $TxCCR0$ and generates an interrupt. The output mode register toggles the output, yielding the period of the carrier frequency as $(TxCCR0 + 1)/f_{Tclk}$, where f_{Tclk} denotes the frequency of the timer clock frequency. The PWM output modes 2 and 6 are set to implement PWM waveforms with

TABLE I: Output modes of Timer_A module

Mode	Description
Mode 0	The output is defined by the OUT bit. The output updates immediately when OUT is updated.
Mode 1	The output is set when the timer counts to $TxCCRn$.
Mode 2	The output is toggled when the timer counts to $TxCCRn$. It is reset when the timer counts to $TxCCR0$.
Mode 3	The output is set when the timer counts to $TxCCRn$. It is reset when the timer counts to $TxCCR0$.
Mode 4	The output is toggled when the timer counts to $TxCCRn$. The output period is double the timer period.
Mode 5	The output is reset when the timer counts to $TxCCRn$.
Mode 6	The output is toggled when the timer counts to $TxCCRn$. It is set when the timer counts to $TxCCR0$.
Mode 7	The output is reset when the timer counts to $TxCCRn$. It is set when the timer counts to $TxCCR0$.

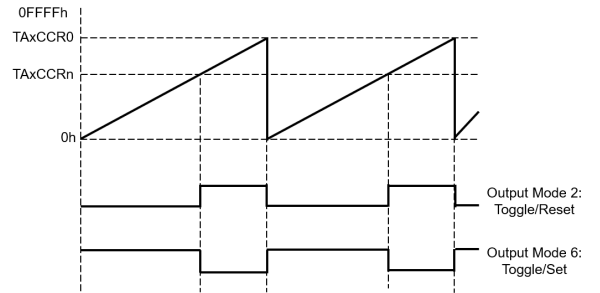


Fig. 2: PWM output scheme in conventional BPSK implementation. The carrier frequency is determined by one cycle of counting up with timer register $TxCCR0$.

180° phase difference. The carrier frequency f_c of the BPSK modulation is:

$$f_c = \frac{\text{timer clock frequency}}{\text{divider} \times (TxCCR0 + 1)}, \quad (1)$$

where the maximum timer clock frequency is 25 MHz, the divider takes values 1, 2,..., 16, and $TxCCR0$ is a 16 bit integer from 1 to 0FFFFh with TI MCU MSP430F5529. As a result, the carrier frequency f_c can theoretically be as high as 12.5 MHz for BPSK if no phase precoding is needed. The symbol rate or bandwidth can be written as:

$$\text{Bandwidth} = \frac{f_c}{n}, \quad (2)$$

where n is the number of carrier cycles occupied by each symbol and can be implemented by a software counter.

The advantage of the above conventional BPSK implementation scheme is that the duty cycle is adjustable by setting the $TAxCCRn$ value. Its limitations include: 1) It cannot configure the carrier's initial phase; 2) Only BPSK can be implemented, not high-order PSK modulation.

B. High-order PSK Modulation

We propose a novel scheme to achieve high-order PSK modulation MIMO transmit by the same hardware resource to improve spectral efficiency and channel capacity. PSK is a digital modulation scheme that conveys data by modulating the phase of a reference signal (the carrier). High-order PSK need more phase control of carrier compared with BPSK. For example, in QPSK modulation, the carrier phase takes on one of four equally spaced values, such as $0, \pi/2, \pi, 3\pi/2$, where each phase value corresponds to a unique modulation symbol. Different from the conventional BPSK modulation using PWM output modes 2 and 6, we use PWM output modes 0 and 4 in this work. Fig. 3 illustrates the control flow of a timer to generate high-order PSK symbols.

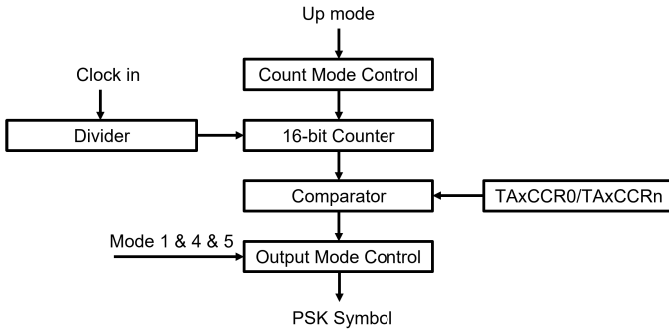


Fig. 3: Control flow of timers for PSK modulation.

In Fig. 3, we first configure the timer clock and the counting mode. With MSP430F5529, the timers support a clock frequency of up to 25 MHz and have a 5-bit clock divider that can provide up to 16 frequency divisions. The counting mode is set as up mode. We then set the PWM output mode according to Table I. PWM output mode 1 and 5 can respectively set/reset the output voltage, which can control the initial output voltage. PWM output mode 4 can toggle high/low output voltages when the timer counts to the preset $TAxCCRn$ value. In output mode 4, the PWM output is only toggled once per timer period, while in output mode 2 or 6, the PWM output is toggled twice per timer period. Therefore, in output mode 4, two cycles of timer produce one cycle of carrier waveform. The benefit of this method is that we can not only use the $TAxCCR0$ value to configure the carrier frequency, but also control the carrier phase by configuring the $TAxCCRn$ value and the initial voltage value p . Being able to configure the phase of the carrier means that different symbols can be generated in high-order PSK modulation. Both the p and $TAxCCRn$ values are reconfigured for each PSK

symbol before it is transmitted. The drawback is that the carrier frequency will be reduced to half but it can be compensated by increasing the clock frequency. In Fig. 4, two PWM waveforms with the same frequency and different phases are generated.

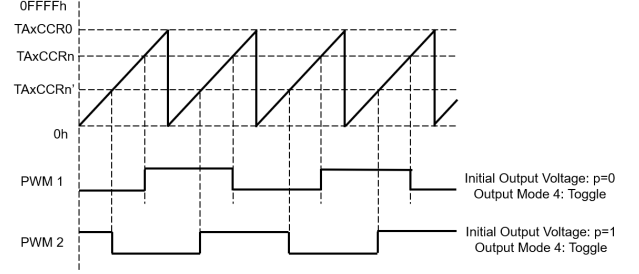


Fig. 4: Phase control in high-order PSK implementation. The carrier frequency is determined by one cycle of counting up with timer register $TAxCCR0$.

The carrier frequency $\tilde{f}_c$ is

$$\tilde{f}_c = \frac{\text{timer clock}}{\text{divider} \times (TAxCCR0 + 1) \times 2} \quad (3)$$

where the feature of timer clock and divider remain the same as (1), but the minimum value of $TAxCCR0$ will change according to the order of PSK modulation since the $TAxCCR0$ value determines the resolution of $TAxCCRn$. For QPSK, 8PSK, 16PSK, the minimum value of $TAxCCR0$ are 3, 7, 15 respectively. The symbol rate or bandwidth is:

$$\text{Bandwidth} = \frac{\tilde{f}_c}{\tilde{n}} \quad (4)$$

where $\tilde{n}$ is the number of carrier cycles occupied by each symbol and is counted by software when a timer interrupt occurs. In Table II, we illustrate a configuration of the timer to implement a QPSK modulation with a carrier frequency of 125 kHz and a bandwidth of 25 kHz. Its four different PWM waveforms are shown in Fig. 5.

TABLE II: Timer configuration of QPSK modulator

Timer Clock	8 MHz			
Divider	1			
TA0CCR0	31			
Carrier frequency ($\tilde{f}_c$)	125 kHz			
Wave Counter ($\tilde{n}$)	10			
Bandwidth	25 kHz			
Output Mode	Modes 4 and 0			
TA0CCR1	31	15	31	15
Initial Output Value (p)	1	0	0	1
PWM waveform	S0	S1	S2	S3

In the proposed high-order PSK implementation scheme, the $TAxCCR0$ value quantizes the configurable phase with $\Delta\phi$, where $\Delta\phi = \frac{\pi}{TAxCCR0+1}$. Since the $TAxCCRn$ value can only take an integer value from 0 to $TAxCCR0$, up to $(TAxCCR0+1)$ PWM waveforms with different phases can be generated, so the maximum achievable order of PSK modulation is $(TAxCCR0+1)$. Proportionally increasing the

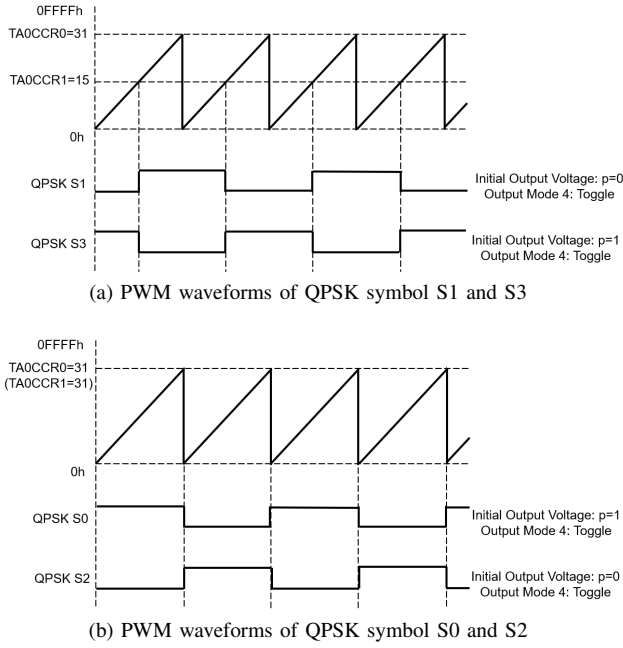


Fig. 5: PWM waveforms for QPSK modulated symbols S0:S3 = $\{1, j, -1, -j\}$, with $j = \sqrt{-1}$.

clock frequency and the value of TAxCCR0 can obtain a higher resolution phase configuration while keeping the carrier frequency unchanged but increasing power consumption. On the contrary, resolution can be sacrificed to reduce power consumption. Therefore, the proposed PSK implementation scheme has flexibility in power consumption and control accuracy.

C. Phase precoding for MIMO transmission

The MCU MSP430F5529 has multiple timers and 13 registers TAxCCRn with $n=1:13$ for use. Each of them can cooperate with TAxCCR0 to generate a PWM output with different phases. Their outputs are synchronized since they can be configured in the same timestamp and then triggered by the same hardware interrupt. Therefore, users can obtain up to 13 multi-channel outputs according to system requirements. Furthermore, each transmit element of the PSK modulated signals can have a different initial phase as needed to achieve phase precoding for MIMO transmission. Fig. 6 shows a constellation diagram of binary QPSK outputs after phase precoding. Both transmitter 1 and transmitter 2 use QPSK modulation, but the carrier phase of transmitter 1 takes $0, \pi/2, \pi, 3\pi/2$ while the carrier phase of transmitter 2 takes $\pi/8, 5\pi/8, 9\pi/8, 13\pi/8$. The constraints of the proposed phase precoding is that the angle is quantized, and the amplitude is fixed. Amplitude precoding is possible by using power amplifiers with a controllable amplification factor for different channels.

D. Signaling and Data Structure

Consider the transmitter of an $N \times M$ MIMO UWA modem, where each of the N bitstreams is independently encoded,

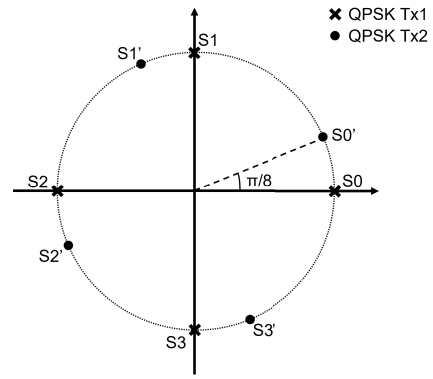


Fig. 6: constellation diagrams of two QPSK modulation.

interleaved, modulated, and then transmitted by a transducer. Fig. 7 shows the block diagram of the n th transmit branch.



Fig. 7: Block diagram of transmitter.

The (2,1,7) convolutional channel encoder and the block interleaver are used in the prototype. The generator of the encoder in octal is (133,171). The interleaver block size is 64×32 . Other encoders and interleavers are also applicable depending on the user requirements.

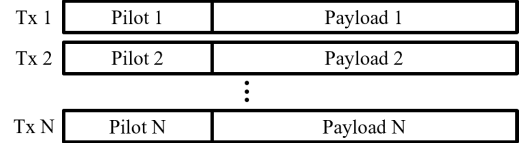


Fig. 8: Data frame structures of MIMO transmitter.

The data frame structure is shown in Fig. 8, where each transmit element separately follows the payload behind its own pilot. The pilots are pseudorandom noise (PN) sequences of the same length but generated by different primitive polynomials. Therefore, they have good autocorrelation and cross-correlation characteristics. The pilot uses BPSK modulation for symbol synchronization and channel estimation. The payload can use high-order PSK modulation, such as QPSK, 8PSK, as needed.

E. Receiver algorithm

At the receiving end, we use the carrier center frequency to down-convert the received passband signal to a baseband signal, and use the baseband signal and the pilot sequence to calculate the cross-correlation to complete symbol synchronization. Taking into account the Doppler shift caused by the underwater acoustic channel, we repeat the above steps using the frequency within the range of plus or minus 5 Hz of the carrier center frequency, and use the frequency that maximizes the pilot cross-correlation result as the result of the

Doppler estimation. Then, use pilot for channel estimation and use the estimated channel for linear equalization, and get the transmitted information after de-interleaving and convolutional code decoding.

III. EXPERIMENTAL RESULTS

To verify the multiple high-order PSK modulated elements output by the proposed implementation, we produced four QPSK modulated transmit elements and used an oscilloscope to capture and record the i th and n th output branches as depicted in Fig. 9. The yellow and blue waveforms are from the i th and n th transmit branches, respectively. The green waveform represents the pure carrier as a reference for identifying the phase. The distinction between different symbols is marked with red lines. It can be clearly observed that the i th and n th transmit branches are synchronized, and the modulated symbols can be clearly distinguished according to the phase.

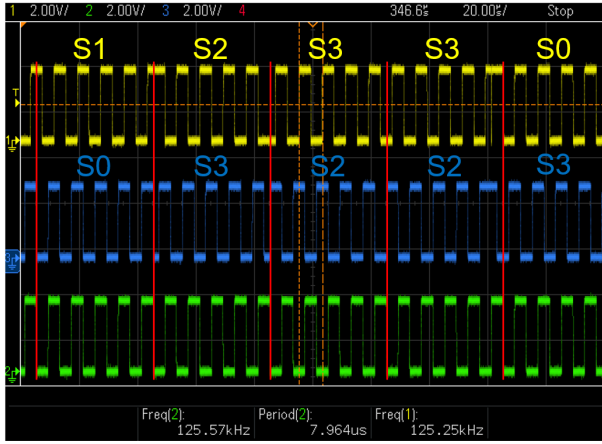
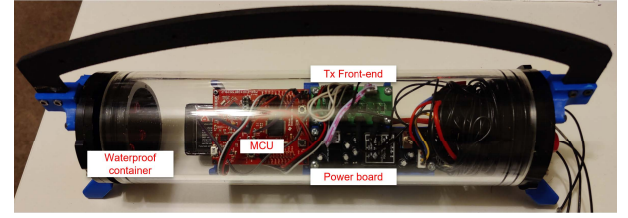
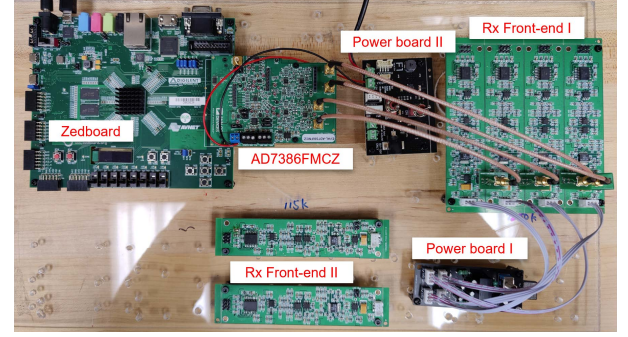


Fig. 9: Waveform of QPSK modulation on the i th (yellow) and n th (blue) transmit branches in comparison to pure carrier (green). Carrier frequency = 125 kHz, symbol bandwidth = 25 kHz.

To evaluate the proposed implementation in a real environment, we designed and built a prototype for lake tests as depicted in Fig. 10. The experimental data was collected in the lake at Nockamixon state park, Quakertown, Pennsylvania. As shown in Fig. 11, we placed the transmitter and the receiver platforms at Node 1, 2, 3 during the tests. Node 1 was 300 meters away from Node 2, and the distance between Node 1 and Node 3 was 450 meters. The nodes were more than 50 meters away from the shore, the water depth was more than 7 meters, and the transducers were 80 cm below the water surface. The parameters for the experiments were: center frequency = 115 kHz, bandwidth = 11.5 kHz, data transmitted were 256-symbol pilot and 2048-symbol payload, with a time duration of 200 ms. We collected 40 packets of data in the lake test, half of which were between node 1 and node 2, and the remaining half were between node 1 and node 3.



(a) MCU-based transmitter



(b) Receiver platform

Fig. 10: Hardware prototype used in the lake tests.

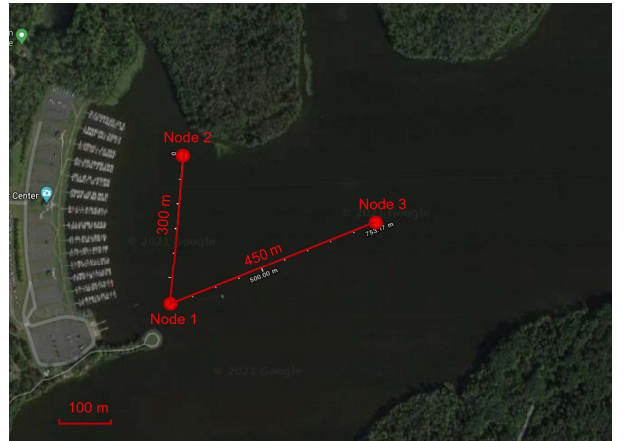


Fig. 11: Experimental nodes used in the lake experiments at the Nockamixon state park, Quakertown, PA.

A. Multi-channel transmission tests

For multi-channel transmission tests, we designed the following experiment: Two images of a dog and a panda composed of 1024 black and white pixels were subjected to (2,1,7) convolutional code and interleaving to produce a length of 2048 payload 1 and payload 2. They are respectively packaged with 256-symbol pilot 1 and 256-symbol pilot 2 and then sent through Tx 1 and Tx 2 simultaneously. We placed the receiving platform on node 1, and placed the transmitter on node 2 and node 3 to collect data.

The received signal is cross-correlated with pilot 1 and pilot 2 to synchronize the symbol, and then the received pilot signal is used for channel estimation. We then use the estimated channel and pilot to obtain the tap value of the linear equalizer, and perform equalization, de-interleaving, convolutional code

decoding and demodulation on the payload data. Fig. 12 shows the scatter plot after equalization and the bit error rate after the decoding is zero.

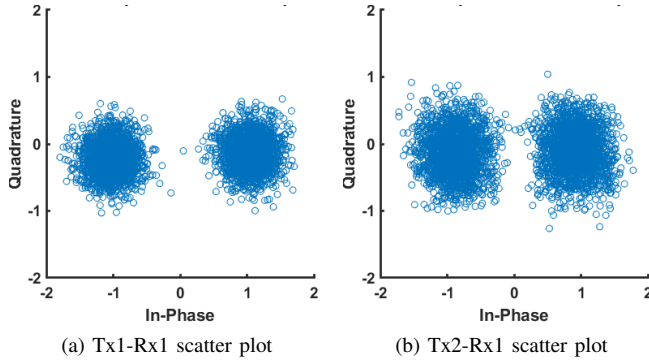


Fig. 12: scatter plots of the BPSK signals after channel equalization.

B. High-order PSK modulation tests

In order to evaluate the performance of high-order PSK implementation, we changed the payload data from BPSK modulation to QPSK and 8PSK modulation. For QPSK tests, the data packet consists of a 256-symbol BPSK-modulated pilot and a 1024-symbol QPSK-modulated payload. Therefore, the transmission period is reduced from 200 milliseconds to 111 milliseconds and data rate increases by 80%. For 8PSK tests, a 512-symbol BPSK-modulated pilot and a 1365-symbol 8PSK-modulated payload are packaged and sent out. The transmission period of such a package is 163 milliseconds while the amount of information bits it contains requires 400 ms with BPSK modulation, so the data rate is increased by 145%. Since we still use BPSK-modulated pilots, the symbol synchronization and channel estimation are similar to the previous BPSK experiments. After processing the payload data including equalization, demapping, de-interleaving, and decoding, we also successfully restored the image with a bit error rate of zero. Fig. 13 shows the QPSK scatter plot after equalization.

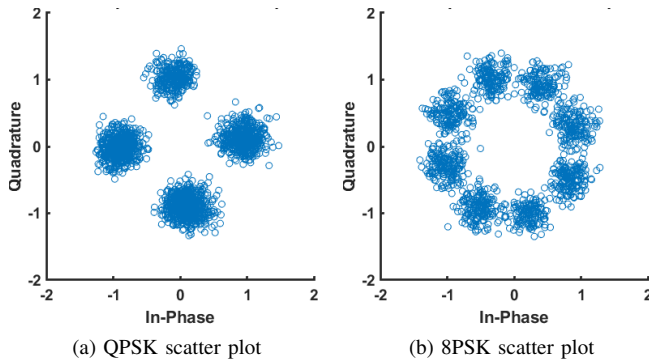


Fig. 13: scatter plots of the QPSK/8PSK signals after channel equalization.

IV. CONCLUSION

In this paper, we propose a low-cost microcontroller implementation of a high-order PSK modulation for MIMO acoustic modem with phase precoding. We highlight the hardware implementation scheme of high-order PSK modulation and phase precoding using two cycles of the MCU timer. Experimental results show that the proposed modem prototype can transmit multiple high-order PSK modulated signals at a distance of 450m. By using two channels for transmission instead of single channel, the data rate is doubled. Compared with the use of BPSK modulation, the use of QPSK and 8PSK modulation increases the data rate by 80% and 145%, respectively. This experiment convinced us that it is feasible to use more transmission channels and higher order modulation, and there is still great potential for data rate improvement.

V. ACKNOWLEDGMENT

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