

Design and Experimental Study of a GaN-based Three-Port Multilevel Inverter

Mohamed Tamasas Elrais and Issa Batarseh
Florida Power Electronics Center
Dept of ECE
University of Central Florida
Orlando, FL 32816
mohamed.elrais@knights.ucf.edu

Abstract—A three-port multilevel inverter with two DC ports and an AC port using Flying Capacitor Multilevel (FCML) design based on Gallium Nitride (GaN) switches is proposed in this paper. Recently, FCML inverter has shown a superior ability for power conversion with high power density, improved Total Harmonic Distortion (THD), and efficiency. The presented three-port multilevel inverter fits various applications such as battery and photovoltaic (PV) grid integration and standalone AC load. The proposed inverter is experimentally verified by building a 3-kW prototype using GaN switches which include two 4-level FCML converter paths, each share the same bus capacitor (C_{bus}), which links them together. One FCML path is 1 kW that incorporates an unfolder for the DC-to-AC conversion and has achieved a peak efficiency of 98.2% with AC voltage and current THDs of 1.26% and 1.23%, respectively. While the second FCML converter path is 2 kW used for the DC-to-DC conversion and has achieved a 99.43% peak efficiency.

Keywords—Three-port inverter, flying capacitor multilevel, Gallium Nitride (GaN) application, Phase shifted PWM (PSPWM), capacitors self-balancing.

I. INTRODUCTION

As reported in the open literature, wide-bandgap power devices such as silicon carbide (SiC) and gallium-nitride (GaN) devices have significantly impacted the re-design of power electronics converters to achieve higher efficiency, higher power density with higher operating temperature and speed. Coupled with the attractive features of multilevel topologies of handling higher power with significant weight and size reduction and improved THD, new research opportunities arise to expand applications where multi functionalities and integration opportunities can be developed. Moreover, numerous multiport converters that fit different applications were reported in the literature [1], [2]. The flying capacitor multilevel (FCML) converter has been gaining increased attention since its first introduction in [3], where only a fraction of the voltage is applied across each switching device to generate output with highly compact power stages. The FCML converter topology has several attractive features, including the capability to naturally balance its capacitor voltages to the desired values using Phase shifted PWM (PSPWM) modulation, and the power switches need only to block a fraction of the input voltage which enables the use of low voltage rating switches in high voltage applications. In addition, FCML processes power with high quality output voltage and current [3]. The need for converters with lower weight and smaller size and keeping high power density and efficiency is on the rise, especially in transportation and PV applications. Recent research proved that this need could be met by utilizing FCML topology [4]–[7]. The wide application of FCML made it possible to be successfully designed as DC-AC [3], [4], [7], as AC-DC [8]–[11], as an

interleaved bidirectional AC-DC and inverter [12]–[14], and as DC-DC [3], [5], [15], [16].

In this work, the attractive FCML topology has been used to develop, for the first time, a GaN-based three-port multilevel inverter. The three-port design is based on the idea of sharing a common bus capacitor for the three ports and deploying two 4-level FCML DC-DC and DC-AC energy conversion paths. The DC-AC conversion path incorporates the well-known unfolding circuit technique for AC voltage generation. The sections of this paper are as follows: section II presents the proposed inverter design and principle of operation. Section III explains the hardware prototype details and components selection. The experimental results are presented in section IV, and lastly, the conclusion is provided in section V.

II. THE INVERTER DESIGN AND PRINCIPLE OF OPERATION

The proposed three-port multilevel converter uses two FCML converters based on GaN devices as power conversion paths. As shown in Fig. 1, there are three ports and two paths, where each path is a 4-level FCML converter. The DC-AC conversion path is 1 kW that incorporates a full-bridge unfolder technique to provide an AC voltage. The DC-DC conversion path is bidirectional and capable of processing a maximum power of 2 kW. Each path has two interfaces; one interface of each path and port-1 are connected to the bus capacitor (C_{bus}) and the other interfaces of each path are connected to a respective port. The port-1 voltage range is between $125 V_{DC}$ to $225 V_{DC}$. The range of port-2 voltage is between $85 V_{RMS}$ to $120 V_{RMS}$ and can support 50 Hz or 60 Hz line frequencies. Whereas the range of port-3 voltage is between 0 to $200 V_{DC}$. The voltage value of each port is chosen based on the application. One example application of this proposed three-port multilevel inverter is connecting PV, battery, and the AC-grid as shown in Fig. 1. Port-1 is $225 V_{DC}$ where the PV can be connected, and it is equal to the bus voltage (V_{bus}) across the bus capacitor. The AC grid is $120 V_{RMS}$ at port-2. The battery is $200 V_{DC}$ which can be connected at port-3. The proposed three-port inverter is designed to process a maximum power of 3 kW through a DC-AC path and a DC-DC path. The two paths and the bus capacitor allow the power to flow between the three ports. It should be mentioned that the three-port inverter is highly reliable because the operation is not impacted if one port source is not connected or fails since the three ports are decoupled.

The number of levels for each flying capacitor multilevel path in this design is chosen to be an even number equals to four. Because a FCML with an even number of levels inherently has higher immunity to capacitor voltage imbalance than a FCML with an odd number of levels,

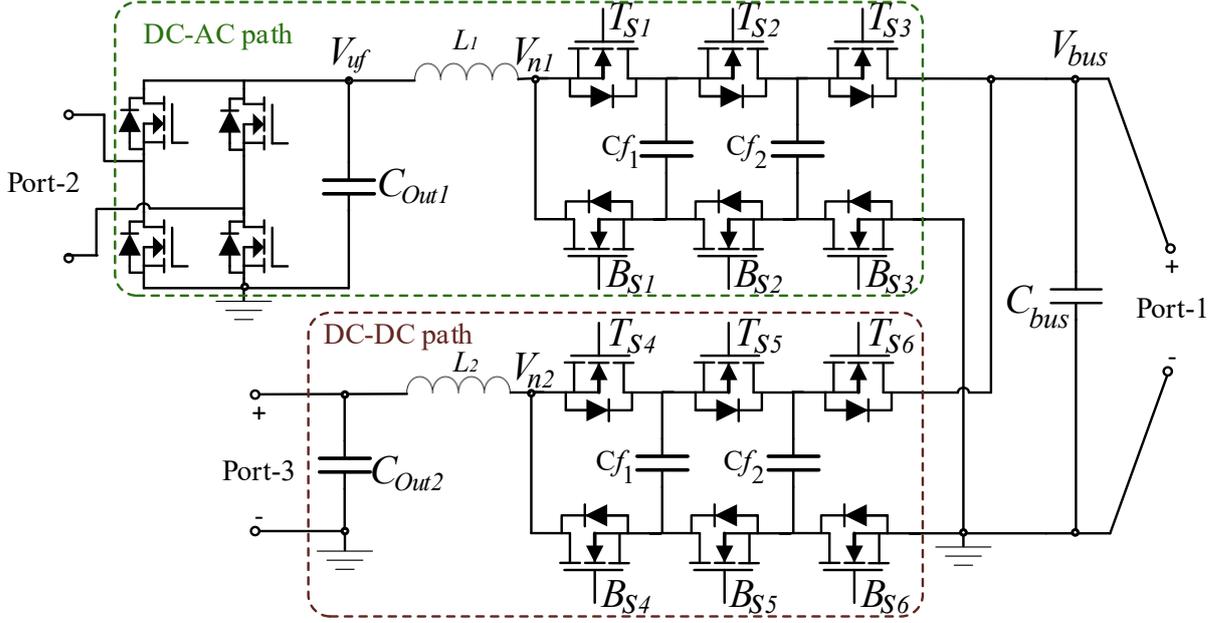


Fig. 1. The circuit diagram of the proposed Three-Port Multilevel inverter.

resulting in a better natural voltage balancing across the capacitors [16].

With m being the number of levels, in this design $m = 4$, each flying capacitor multilevel path has $2(m - 1) = 6$ switches. The nominal blocking voltage of each switch is a fraction of the bus voltage equals to $\frac{V_{bus}}{m-1}$. However, the switches should be designed to block a maximum voltage ($V_{M,block}$) as follow:

$$V_{M,block} = \frac{V_{bus}}{m-1} + \Delta V_{cf} \quad (1)$$

Where ΔV_{cf} is the flying capacitor voltage ripple that is also used as a design criterion to determine the values of the flying capacitors, and it is a percentage of $\frac{V_{bus}}{m-1}$ [4], [7]. ΔV_{cf} in this design is chosen to be 8% of $\left(\frac{V_{bus}}{m-1}\right)$. With $V_{bus} = 225$ V_{DC}, each switch maximum blocking voltage according to (1) is found to be $75V + 6V = 81V$.

Each FCML path has $(m - 2)$ flying capacitors. Therefore, for $m = 4$, each path has two flying capacitors with voltages across them equal to:

$$V_{cf_n} = \frac{nV_{bus}}{m-1} \quad (2)$$

Where V_{cf_n} is the voltage across the n^{th} flying capacitor and n equals 1 or 2. As a result, each flying capacitor has a voltage across it according to (2) as follow: $V_{cf_1} = \frac{V_{bus}}{m-1} = \frac{225}{4-1} = 75$ V, and $V_{cf_2} = \frac{2V_{bus}}{m-1} = \frac{2 \times 225}{4-1} = 150$ V as shown in Fig. 2; it is clear that the two flying capacitor voltages and the bus voltage are evenly spaced by a value of $\frac{V_{bus}}{m-1} = 75$ V and well balanced at their designed values.

As mentioned earlier, the flying capacitor voltage ripple is a design criterion that affects the value of the flying capacitor according to (3). The higher the ripple, the lower the flying capacitor's capacitance because more energy can be transferred in each switching cycle. However, the allowed

flying capacitor voltage ripple must be within the range of $0 \leq \Delta V_{cf} < \frac{V_{bus}}{m-1}$ to avoid an unwanted instant of V_{cf_1} exceeding V_{cf_2} resulting in the body diodes of the top and bottom switches between the capacitors (T_{S2} and B_{S2} in Fig. 1) to turn on and circulating current between the flying capacitors. [4], [7]:

$$Cf = \frac{i_{load}}{\Delta V_{cf} \cdot f_{sw} \cdot (m-1)} \quad (3)$$

The flying capacitor value is found to be 4.6 μ F according to (3) when the switching frequency, f_{sw} , is equal to 120 kHz, and the current of the load, i_{load} , is equal to 10 A.

The gate charge of the GaN switches is lower than that of the Silicon MOSFET. Therefore lower switching losses and higher switching speed can be achieved [17], enabling the use of 120 kHz switching frequency. Moreover, the power density of the converter is enhanced by using the GaN devices since their footprint is minimal.

The Phase Shifted Pulse Width Modulation (PSPWM) is applied to control the switches to self-balance the flying

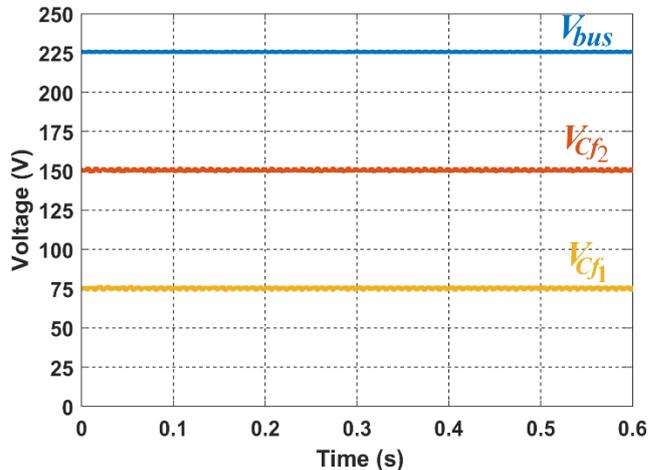


Fig. 2. The simulated bus and flying capacitor voltages of the DC-DC path.

capacitor voltages of the three-port multilevel inverter. In this control scheme, the top switches of each path are switching in a complementary fashion with the bottom switches. The top switches have a duty cycle equal to D , while the bottom ones have a duty cycle equal to $(1 - D)$. The PWM signals of any adjacent switches are shifted from each other by $\frac{360^\circ}{m-1}$. It should be noted that the average output voltage, V_{out} , of each path is given in (4), and therefore the gain of each FCML path operating in buck mode is the same as the two-level conventional buck converter [3], [4], [7].

$$V_{out} = D \cdot V_{bus} \quad (4)$$

The simulated node voltage V_{n2} of the DC-DC path (in Fig. 1) when stepping down a voltage of $225 V_{DC}$ at port-1 to $45 V_{DC}$ at port-3 is shown in the bottom subplot of Fig. 3. The PWM signals of the top switches (T_{S4} , T_{S5} , and T_{S6}) have a fixed duty cycle $D = 0.2$, and the signals of any adjacent switches are shifted $\frac{360^\circ}{m-1} = 120^\circ$ from each other. The PWM signals of the bottom switches (B_{S4} , B_{S5} , and B_{S6}) have a fixed duty cycle of $(1 - D) = 0.8$ as shown in the top subplot of Fig. 3. It can be seen that V_{n2} have three pulses in a single switching period $T_{sw} = 8.33 \mu s$ compared to a single pulse in each switch PWM signal, and that is why the actual frequency (f_{actual}) at the node voltage V_{n2} seen by the inductor is three times the switching frequency of each switch, which can be found as

$$f_{actual} = (m - 1)f_{sw} \quad (5)$$

It should be noted that in the DC-DC path of Fig. 1, to step down the bus voltage that is equal to $225 V_{DC}$ at port-1 to a $45 V_{DC}$ at port-3, just a fraction of the entire voltage of $\frac{V_{bus}}{m-1}$ at node voltage V_{n2} is chopped at the actual frequency (in case of $m = 4$, V_{n2} switches between 0 and $75 V_{DC}$ as shown in Fig. 3) with an actual duty cycle, D_{actual} , equal to 0.6, which is calculated according to (6) [7]. However, in the conventional buck converter, when stepping down an input voltage, the entire input voltage is chopped at the switching frequency with a specific duty cycle to get the output voltage; for example, to get $45 V_{DC}$ from an input voltage of $225 V_{DC}$, the voltage seen by the inductor is switching between 0 and

$225 V_{DC}$ at the switching frequency with a regular duty cycle $D = 0.2$.

$$D_{actual} = (m - 1)D - \text{floor}((m - 1)D) \quad (6)$$

Each FCML path deploys an inductor that is $(m - 1)^2 = 9$ smaller than that deployed for the conventional buck converter because of the frequency multiplication effect by a factor of $(m - 1)$ seen by the inductor and the voltage reduction across the inductor by a factor of $\frac{1}{m-1}$. As a result, the inductor is found to be [4], [7]:

$$L = \frac{0.25 V_{bus}}{\Delta_{iL} f_{sw} \cdot (m-1)^2} \quad (7)$$

Where Δ_{iL} is the inductor current ripple, which is in this design selected to be 1.55 A. the value of the inductor is calculated to be 33.6 μH ; this inductor value ensures that the inductor current ripple does not exceed its maximum value of 1.55 A.

The PSPWM is applied to control the switches of the DC-AC path as well. The PWM signals of the top three switches T_{S1} , T_{S2} , and T_{S3} have a dynamic and equal duty cycle D that follow a full-wave rectified sinusoidal reference to generate a four levels staircase rectified sinewave at node V_{n1} (annotated in Fig. 1) as shown in Fig. 4. The PWM signal of each switch is shifted $\frac{360^\circ}{m-1} = 120^\circ$ from its adjacent signals. The PWM signals of the bottom switches B_{S1} , B_{S2} and B_{S3} are complementary to the top ones with an equal duty cycle of $1 - D$. The pulse frequency of the staircase voltage is 360 kHz, which is three times the switching frequency of each switch, as seen in the zoomed-in portion of Fig. 4. A clean rectified sinusoidal voltage is obtained at node V_{uf} by filtering the four levels staircase voltage as illustrated in Fig. 4. Finally, unfold the node voltage V_{uf} via the full-bridge unfolder to generate the 60 Hz, $120 V_{RMS}$ output voltage[4], [14]. The charging and discharging actions of the flying capacitors using the PSPWM control occur every switching cycle, which is an advantage compared to the level-shifted PWM modulation [18], [19]. This advantage maintains the capacitor voltage ripples low, reduces the capacitors' energy storage requirement, and helps achieve better capacitor voltages balance.

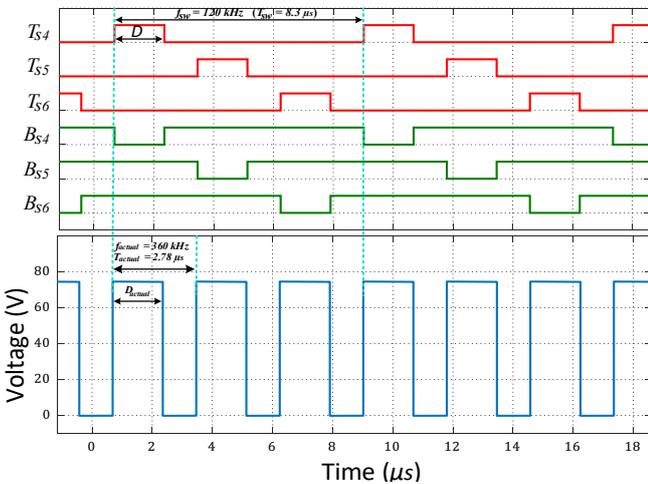


Fig. 3. The simulated PSPWM signals of the DC-DC path with a duty cycle of 0.2 (top) and the simulated node voltage V_{n2} (bottom).

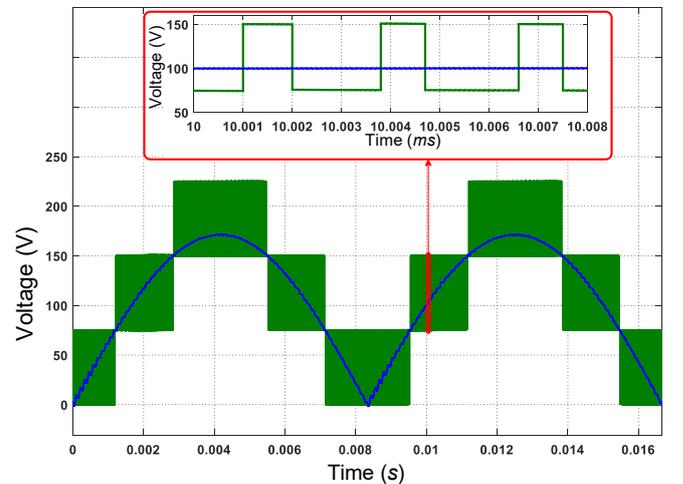


Fig. 4. The simulated voltages of nodes V_{n1} and V_{uf} (in Fig. 1) including a zoomed-in portion.

III. HARDWARE PROTOTYPE

A hardware prototype has been built to verify the design, and it is capable of processing a maximum power of 3 kW. Annotated photographs of the prototype's top, bottom, and profile views are shown in Fig. 5. The EPC 2034C GaN FETs have been used as the power switches and driven by Texas instrument, LM5114, Low-side gate drivers. GaN switches facilitate the used high switching frequency of 120 kHz. Fast transition between ON and OFF states is vital to reduce the overlapping losses when operating at such a high frequency. The drain-source voltage ringing, resulted from the fast transition and the parasitic inductance, is reduced by a careful layout of the PCB and using small decoupling capacitors, 47 nF TDK, C2012X7T2W473K125AE, that have low parasitic inductance placed as close as possible to the complementary switches in parallel with the main flying capacitors to minimize the commutation loop and parasitic inductance during switches ON/OFF transitions [4], [7], [9], [14]. The capacitors selected for the bus, output, and the flying

capacitors are TDK, C5750X6S2W225K250KA, multilayer ceramic capacitors for their high energy density, and placed on the bottom side of the PCB [4], [7]. The required isolated supplies for each gate driver are achieved via Analog Devices, ADUM5210, isolated dc-dc converters, and the PWM signals are isolated using Silicon Labs, SI8423BB-D-IS, digital isolator [4], [7], [12]. Coilcraft, XAL1510-333MED, 33 μ H inductors are used for each path. Since the switches of the full-bridge inverter are switching at the line frequency of 60 Hz, STMicroelectronics, STL57N65M, MOSFETs are used because they have sufficient switching speed and are driven by Fairchild, FAN73932MX, half-bridge gate drivers [4], [9], [14]. TI C2000 Microcontroller, TMS320F28379D LaunchPad was used to generate the PWM signals of all switches, including the inverter switches. The box volume of the hardware prototype is 11.6 in³, excluding the heatsink and the Microcontroller, resulted from box dimensions of 4.8 in \times 4.3 in \times 0.56 in. Table I summarize the complete components list of the prototype.

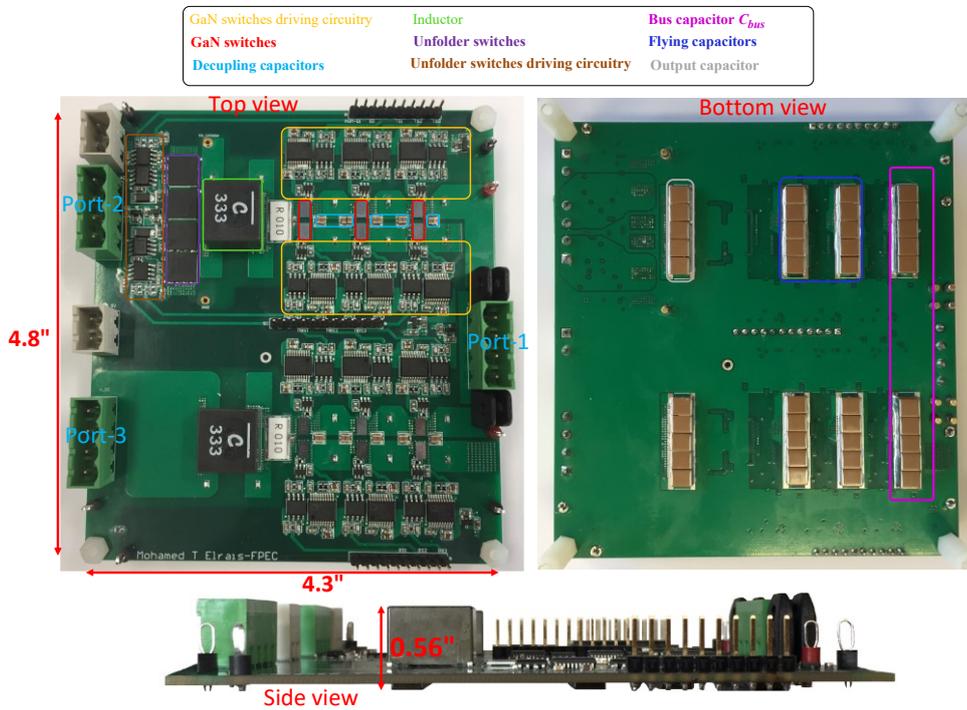


Fig. 5. photographs of the top, bottom, and profile views of the prototype.

TABLE I. THE COMPONENT LIST OF THE HARDWARE PROTOTYP.

Component	Part number	Specifications
GaN switches	EPC2034C	GANFET, N-Channel, 200 V, 48 A, 8 m Ω
GaN switches gate drivers	LM5114BMF/NOPB	
Decoupling Capacitors	C2012X7T2W473K125AE	47 nF, 450 V
Isolated dc-to-dc supplies	ADUM5210CRSZ	
Digital isolators	SI8423BB-D-IS	
Output and flying capacitors	C5750X6S2W225K250KA \times 5	2.2 μ F, 450 V
Bus capacitor	C5750X6S2W225K250KA \times 10	2.2 μ F, 450 V
Inductors	XAL1510-333MED	33 μ H, 16.7 A
Unfolder switches	STL57N65M	MOSFETs N-Channel 650 V, 22.5A, 69 m Ω
Unfolder switches gate drivers	FAN73932MX	
Microcontroller	TMS320F28379D	

IV. EXPERIMENTAL RESULTS

The three ports working simultaneously with the port-1 voltage of $225 V_{DC}$, the port-2 voltage of $120 V_{RMS}$, and the port-3 voltage of $200 V_{DC}$, are shown in Fig. 6.

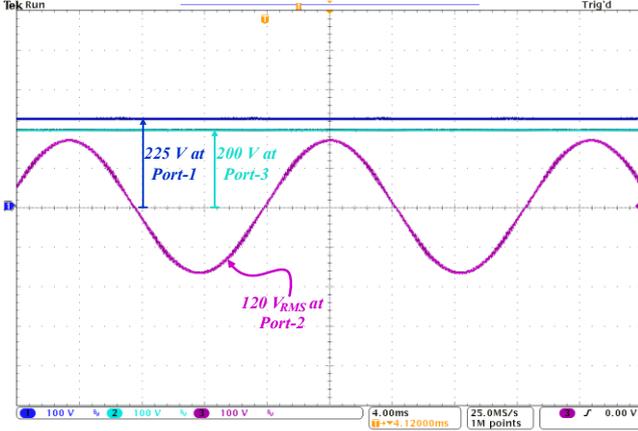


Fig. 6. The voltages of the three ports working simultaneously at Port-1 = $225 V_{DC}$, Port-2 = $120 V_{RMS}$, and Port-3 = $200 V_{DC}$.

The generation of the AC voltage is done by making the switches synthesize a four levels staircase rectified sinewave voltage at the node V_{n1} , annotated in Fig. 1. The pulse frequency of this staircase voltage is 360 kHz resulted from tripling the 120 kHz switching frequency because of the frequency multiplication effect of the 4-level FCML path. It should be noted that the 360 kHz is the frequency seen by the inductor. Moreover, the equal 75 V step increments of the staircase voltage waveform shown in Fig. 7 indicate well-balanced voltages across the flying capacitors in the DC-AC path. Then, a clean rectified sinewave with a peak voltage equal to $170 V_{peak}$ at node V_{uf} (annotated in Fig. 1) is obtained by filtering the high pulse frequency staircase voltage as shown in Fig. 7. Finally, the rectified sinewave is unfolded using the unfolder to get the required 60 Hz AC voltage at port-2.

To illustrate the bidirectional capability of the DC-DC path, a $36 V_{DC}$ supply is connected to port-3 with a 1 to 5 step-up conversion ratio to dispatch power to port-1. The bidirectionality is evident from the negative polarity of the inductor current (i_L) shown in Fig. 8. In addition, the node voltage V_{n2} (in Fig. 1.) is shown in Fig. 8 during stepping up $36 V_{DC}$ at port-3 to $180 V_{DC}$ at port-1. It is clear from the equal pulse heights of $\frac{180}{m-1} = 60 \text{ V}$ of the node voltage V_{n2} that the

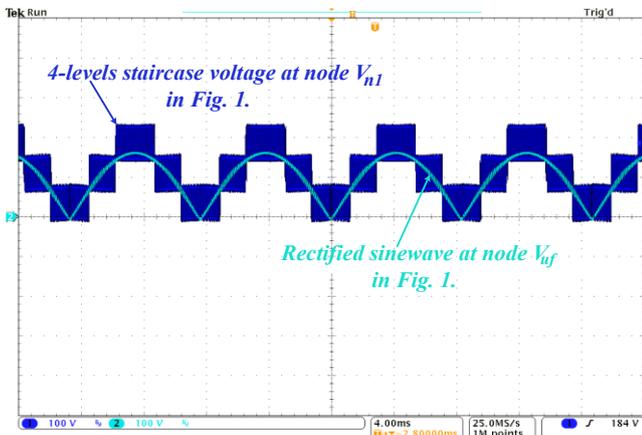


Fig. 7. The node voltages V_{n1} and V_{uf} (annotated in Fig. 1.).

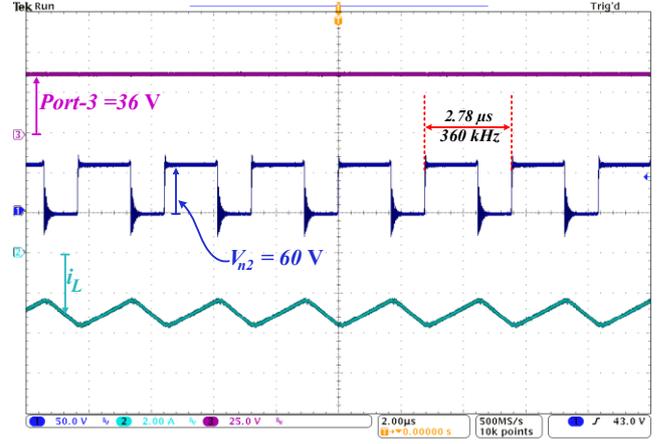


Fig. 8. Port-3 voltage, node voltage V_{n2} (annotated in Fig. 1.), and inductor current in the DC-DC path in a step-up operation of $36 V_{DC}$ to $180 V_{DC}$.

flying capacitors of the DC-DC path are well balanced at their desired voltage values. The actual frequency seen by the inductor in the DC-DC path is the frequency of the node voltage V_{n2} of 360 kHz .

The output voltage and current of port-2 at 1 kW received from port-1 is shown in Fig. 9. These output voltage and current of $120 V_{RMS}$ and $8.3 A_{RMS}$ have waveforms very close to a sinusoidal waveform with a Total Harmonic Distortion of 1.26% and 1.23% , respectively.

The YOKOGAWA PZ4000 power analyzer is used to measure the efficiency curves of the two conversion paths. The measured data is plotted in Fig. 10. It is clear from Fig. 10 that the DC-AC conversion path's peak efficiency, η_{12} , from port-1 to port-2, when their operating voltages are $225 V_{DC}$ and $120 V_{RMS}$ respectively, is 98.2% , which occurs at 500 W . The DC-DC conversion path's peak efficiency, η_{13} , from port-1 to port-3, when their operating voltages are $225 V_{DC}$ and $200 V_{DC}$ respectively, is 99.43% , which occurs at 990 W . The light load efficiencies at about 50 W are 90% for η_{12} and 93.1% for η_{13} without any light load control included.

The specifications of the three-port multilevel converter prototype are given in Table II. The inverter was tested at full load power by dispatching 3 kW from port-1 through the two paths where port-2 receives 1 kW and port-3 receives 2 kW . Therefore, using this tested power of 3 kW with the converter

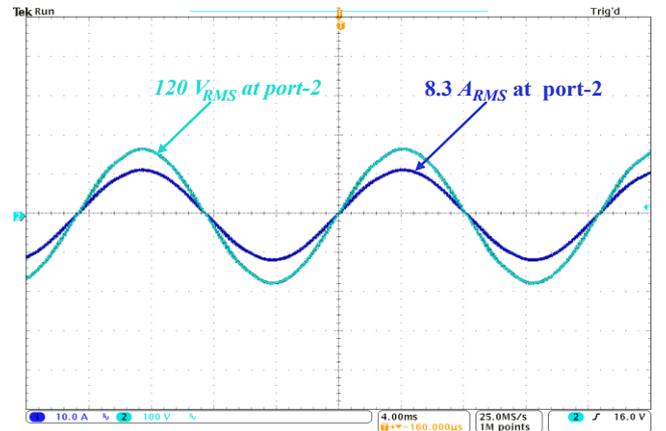


Fig. 9. The output voltage and current of $120 V_{RMS}$ and $8.3 A_{RMS}$ of port-2 at 1 kW received from port-1.

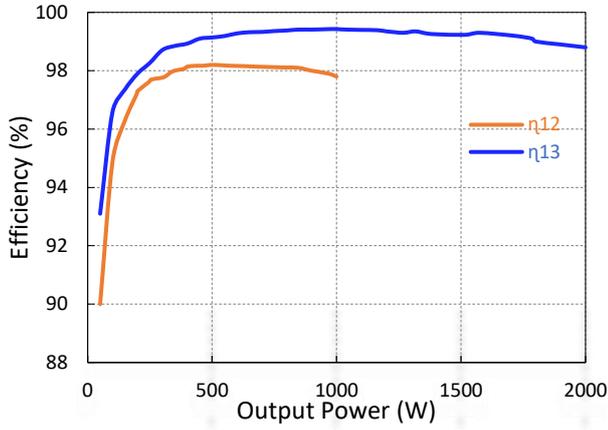


Fig. 10. Measured individual efficiency curves of both paths.

box dimensions of 4.8 in \times 4.3 in \times 0.56 in (12.2 cm \times 10.9 cm \times 1.44 cm), the tested power density is found to be 285.6 W/ in³ (15.7 W/ cm³), excluding the heatsink and the Microcontroller.

TABLE II. THE INVERTER SPECIFICATIONS.

Specifications	Tested Value
V_{bus}	225 V _{DC}
Port-1 voltage	225 V _{DC}
Port-2 voltage	120 V _{RMS}
Port-3 voltage	200 V _{DC}
Port-1 power	3 kW
DC-AC path / Port-2 power	1 kW
DC-DC path / Port-3 power	2 kW
Switching frequency	120 kHz
Actual frequency (seen by the inductors)	360 kHz
THD of Port-2 voltage	1.26 %
THD of Port-2 current	1.23 %
Peak DC-AC path efficiency, η_{12} at 500 W	98.2 %
Peak DC-DC path efficiency, η_{13} at 990 W	99.43 %
Inverter dimensions excluding heatsink and microcontroller	4.8 in \times 4.3 in \times 0.56 in (12.2 \times 10.9 \times 1.44) cm
Inverter box volume excluding heatsink and microcontroller	11.6 in ³ (191.5 cm ³)
Overall power density excluding heatsink and microcontroller	285.6 W/ in ³

V. CONCLUSION

A three-port multilevel inverter deploying Gallium Nitride devices, GaN, is presented in this work. The three-port inverter is based on the 4-level flying capacitor multilevel topology. A 3-kW experimental hardware prototype is built to verify the design. The prototype has a 1 kW DC-DC conversion path that includes a full-bridge unfolded for the AC generation that has achieved a peak conversion efficiency of 98.2 % occurred at 500 W and a 2 kW DC-DC conversion path that has achieved a peak efficiency of 99.43 % occurred at 990 W. The power is dispatched between the three ports through the two conversion paths. Finally, the prototype has achieved a power density of 285.6 W/ in³ (15.7 W/ cm³), excluding the heatsink and the Microcontroller.

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