Short-channel robustness from negative capacitance in 2D NC-FETs

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To date, the robustness of performance, including tolerance to channel-length scaling effects, in scaled transistors has become increasingly important. Negative capacitance (NC) field-effect transistors (FETs) have drawn considerable attention and many studies have revealed that the NC effect is beneficial for device scaling. However, there is a lack of experimental evidence of short-channel behavior in NC-FETs with two-dimensional (2D) semiconducting channels and theoretical studies are limited. Here, we experimentally study 2D MoS_2-based NC-FETs using MoS_2 with CMOS-compatible hafnium zirconium oxide ($HfZrO_2$ or HZO) as the ferroelectric (FE) and demonstrate remarkable short-channel behavior compared to similar 2D MoS_2 FETs. It was observed that the subthreshold switching improvement becomes increasingly significant at shorter channel lengths, down to 20 nm. From analysis of the capacitive network, we show that the NC effect is impacted by a larger magnitude of polarization in the ferroelectric, which enhances gate control and is beneficial to channel-length scaling.

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For decades, low-power digital technologies have been realized using silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs) that have followed Moore's law, enabling exponential increase in functionality by scaling down the transistor size to increase transistor density on a chip. However, decreasing the size of transistors has become increasingly difficult due to short-channel effects (SCEs) and increasing power consumption.[1, 2] These challenges can potentially be resolved by reducing the subthreshold swing (SS) in MOSFETs below the 60 mV/decade thermal limit at room temperature, thus enabling low-voltage operation. Negative capacitance field-effect transistors (NC-FETs)[3, 4] have the potential for reducing SS by adding a ferroelectric (FE), such as doped hafnium oxide,[5-7] to the gate stack of an otherwise traditional FET.[8-13]

The use of low-dimensional channel materials, including 2D transition metal dichalcogenides (TMDs, such as molybdenum disulfide (MoS_2)), can also enable miniaturization of transistors thanks to sub-nm thinness to enhance electrostatic control of the channel.[14,15] Bringing together the benefits of sub-thermal switching from the NC effect with the electrostatic scalability of 2D material-based channels offers a device of great potential significance for future technologies. NC-FETs with 2D channels (2D NC-FETs) were first demonstrated using a ferroelectric polymer in the gate stack,[16] but have since been studied with a variety of gate stacks based on doped hafnium oxide ferroelectric films.[17-20] To date, the behavior of long-channel 2D NC-FETs has been widely explored; however, the impact of NC on SCEs in 2D NC-FETs has received little attention. While all of the proper motivation is in place regarding the anticipated scalability of 2D NC-FETs, the complexity of the fields in such a capacitively dependent device suggests the need for more careful consideration of the impact of scaling.

Experimental evidence from Si-based NC-FETs confirmed that SS improvement becomes pronounced at shorter channel lengths.[21-23] Other studies propose NC-FET operation will be significantly impacted by the reduction of channel potential at short channel lengths,[24,25] which could have unique implications for ultrathin 2D channels. However, understanding of how the NC effect influences short-channel behavior in 2D NC-FETs has yet to be examined experimentally. Recently, a study experimentally reported that SS of a top-gated MoS_2 NC-FET with a polymeric FE drastically degraded with extreme channel length scaling.[26] Hence, further experimental studies are needed to ascertain if the NC effect can be beneficial for alleviating SCEs in the unique electrostatic environment of 2D NC-FETs.

In this work, we experimentally demonstrate 2D NC-FETs using MoS_2 with CMOS-compatible hafnium zirconium oxide (HZO) as the FE. With a bottom-gated structure, 2D FETs are directly compared with 2D NC-FETs having the exact same gate stack (without annealing to drive ferroelectricity in HZO for the 2D FETs) across gate lengths ranging from 80 nm down to 20 nm. The 2D NC-FETs not only exhibit more robustness when scaled to ~20 nm channel lengths, but they actually show marked improvement in SS and on/off-current ratio as the device is scaled – an unanticipated fallout of the unique fields in the NC-based device. The mechanisms behind this observed improvement in scaling behavior for 2D NC-FETs is discussed and analyzed, providing important forecasting for the potential of these devices in future scaled technologies.

The device structure of the 2D NC-FETs studied in this work is shown in Fig. 1(a), and includes a gate stack based on previous results,[18] which reported a more stable switching behavior under changing drain-source bias (V_{ds}) when using Al_2O_3 as the dielectric at an equal thicknesses of 10 nm with the FE HZO.[27] Gate stack characteristics were obtained using FE capacitors of 10 nm HZO / 10 nm Al_2O_3 grown using atomic layer deposition (ALD) on p++ Si wafers with top Pt electrodes, which were annealed at 550 °C for 30 s in an Ar ambient (Fig. 1(e)) to drive the crystal transition in the HZO that yields ferroelectric properties. Transistors were fabricated by transferring MoS_2 onto the wafer and forming source/drain contacts (20 nm Ni). Thicknesses of the MoS_2 flakes was 1-2 nm. Channel lengths (L_{ch}) were confirmed using scanning electron microscopy (SEM) imaging, from 20 - 80 nm (Fig. 1(b), (c)). The 2D FET devices fabricated for comparison followed the same process flow, including the same ALD-formed gate stack, but without the annealing so that the HZO film did not exhibit FE behavior (Fig. 1(e)).[28] All devices were electrically characterized using the same measurement conditions as previous publications in the field for consistency.[17]

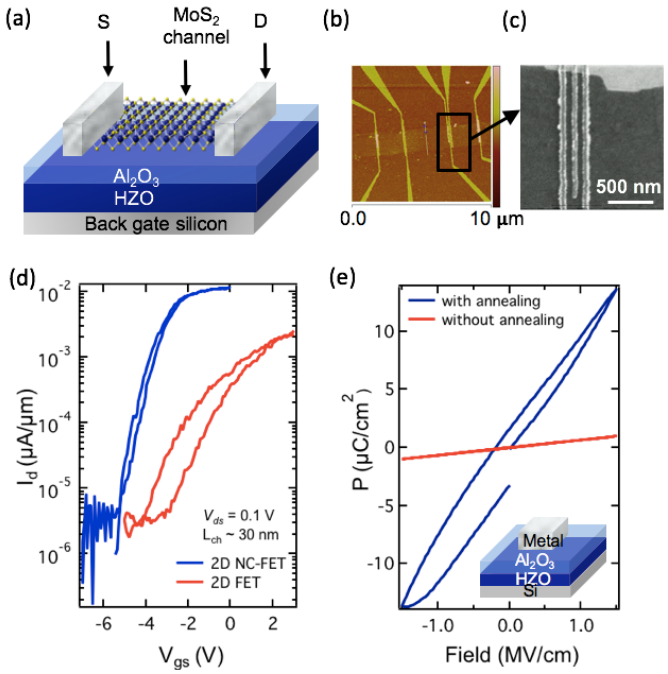

FIG. 1. Short-channel 2D NC-FET versus 2D FET. a) Schematic of back-gated MoS_2 device with 10 nm HZO and 10 nm Al_2O_3 as the gate stack (annealed for 2D NC-FET, not annealed for 2D FET). b) AFM and c) SEM images of the channel region showing channel lengths down to 20 nm. d) Subthreshold curves comparing a 2D NC-FET vs conventional 2D FET with channel lengths of ~30 nm. e) Polarization - electric field (P-E) curves before and after annealing the gate stack at 550 ◦C in RTA for 30 sec. The inset is the structure of the capacitors.

A comparison of the 2D NC-FET and 2D FET devices both at a short channel length of 30 nm reveals significant improvement in subthreshold behavior, including the SS and hysteresis, in the 2D NC-FET (see Fig. 1(d)). The steeper SS of the 2D NC-FET is attributed to the enhancement of capacitance through appropriate matching between the positive device capacitance ($C_{dev} > 0$) and the negative differential capacitance of the FE ($C_{FE} < 0$); however, this is analyzed further below. Particularly important in investigating the performance of NC-FETs is the capacitive network in the device, where an effective capacitance matching with the FE is an indication of better gate-control. To achieve stable sub-thermionic operation in NC-FETs, it is crucial that the gate stack capacitance is designed to be larger than C_{dev}, where the negative C_{FE} compensates the positive capacitances in the device.[29]

Regarding this comparison between the 2D NC-FET and 2D FET (where the only difference is an anneal performed on the HZO / Al_2O_3 gate stack for the NC-FET), it is acknowledged that there are several features these devices do not share in common. First and foremost, the anneal yielded ferroelectric behavior in the HZO compared to standard dielectric polarization in the unannealed stack. Second, and related to the first point, the HZO undergoes a crystalline transition to the orthorhombic phase, which is a

key aspect of yielding the ferroelectric behavior. Third, as a ferroelectric, the annealed HZO will exhibit a much higher relative permittivity compared to the unannealed HZO, which will by its very nature yield a gate stack with stronger gate coupling. Despite these differences, the comparison between these devices is still quite insightful as they share a common overall dimensional and design structure and material stack, minus the annealing step. What's more, it will be seen that the scalability of the 2D NC-FET actually defies conventional expectations, even with a higher permittivity gate stack, as the performance in terms of gate control actually improves with scaling of the gate length below 50 nm.

Polarization behavior of the annealed gate stack used in these 2D NC-FET devices (Fig. 1(e)) have been tested by using PUND (positive up negative down) method for excluding the impact of leakage current on the P-E curve. While testing, triangle waves of 1 kHz were applied. The P-E curve shows remnant polarizations $+P_r$ and $-P_r$ are 1.60 and -3.23 μC/cm^2, respectively, which is lower than other works in the field,[17] allowing for more effective match between the C_{FE} and the channel capacitance and resulting in lower hysteresis in these 2D NC-FETs. This phenomenon arises from the lower ferroelectric capacitance (low $|dP/dE|$ near $E = 0$) for a given FE thickness due to the absence of the interfacial metal layer.[19,30]

The effect of V_{ds} on the subthreshold behavior is shown in Fig. 2(a), which also shows a gate leakage current orders of magnitude less than the drain current (~ 10^{-11} A). An increase in V_{ds} from 0.1 V to 1 V causes the I_d-V_{gs} curve to shift in the negative direction—this is consistent with drain-induced-barrier-lowering (DIBL), widely observed in conventional n-type MOSFETs, where the threshold voltage (V_{th}) shifts negatively as V_{ds} increases. In some long-channel 2D NC-FETs, negative DIBL has been observed, which originates from the capacitance coupling from the drain to the interface between Al_2O_3 and HZO;[19] this phenomenon is explained by an interfacial potential reduction when increasing V_{ds}. In the case of these short-channel 2D NC-FETs, particularly that shown in Fig. 2(a), it's clear that the more traditional lowering of the energy barrier in the channel from an increased drain field is overwhelming the potential reduction at the dielectric/ferroelectric interface – this is not surprising considering the physical thickness of the gate stack (20 nm total thickness) compared to the channel length.

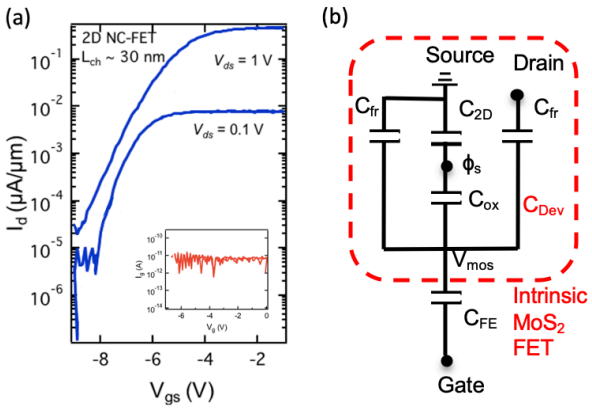

FIG. 2. Performance and capacitive network of a 2D NC-FET. a) The subthreshold curves of a 2D NC-FET at different V_{ds}, inset is the gate leakage current. b) Small-signal capacitance circuit of a 2D NC-FET.

Impact of the NC effect on MoS_2 device performance at scaled channel lengths is demonstrated by comparing the subthreshold curves of conventional 2D FETs with 2D NC-FETs at similar channel lengths (Fig. 3). The 2D NC-FETs clearly exhibit resilient scaling behavior compared to their 2D FET counterpart. As shown in Fig. 3(c), in 2D NC-FETs (where $\mathbf{\Delta}SS/SS_{LC}$ denotes the difference between SS at the current channel length to that of the longest channel device ($\mathbf{\Delta}SS$), divided by the SS of the longest channel device (SS_{LC})), the minimum SS achieved decreases as the channel length scales down; i.e., scaling actually improved the switching behavior of the 2D NC-FET. Compared to the device with channel length of 70 nm, the devices with channel length of 20 nm, 40 nm, and 50 nm have an SS that is 57 %, 42%, and 37% lower, respectively. Additionally, the on/off-current ratio (I_{ON}/I_{OFF}) increases by 1-2 orders of magnitude when scaling the channel length from 70 to 20 nm (Fig. 3(d)) (The on-current is defined as the value of the drain current at Vgs around 0 V and Vds of 0.1 V, while the off-current is at Vgs around -7 V and Vds of 0.1 V.). In contrast, the 2D FETs displayed a SS increase with shorter channel lengths, with the I_{ON}/I_{OFF} ratio decreasing by an order of magnitude when the channel length scaled from 80 nm to 30 nm. This phenomenon is most evident when scaling to extremely small channel lengths (~20 nm). Due to the SCEs, which are typically seen in conventional devices, and based on the thickness of our gate stack (hence, the electrostatics), the device performance deteriorates when scaling the channel length down to sub-20 nm.[31]

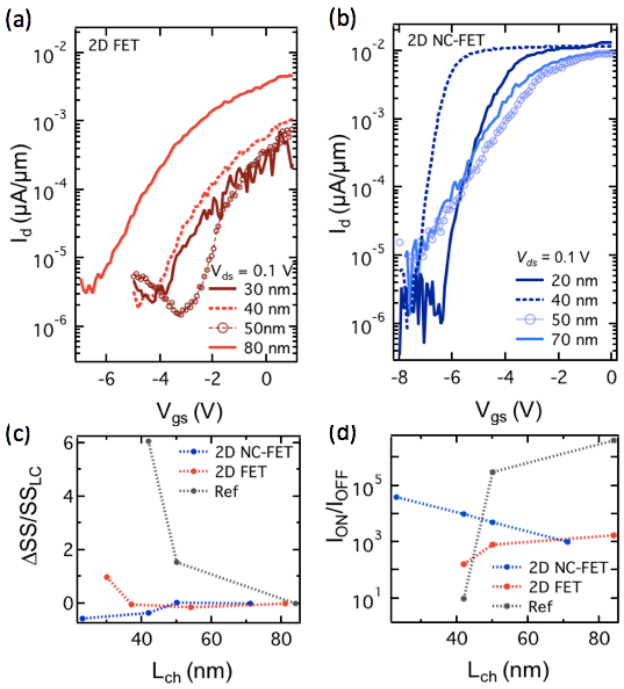

FIG. 3. Impact of NC effect on MoS_2 device performance at scaled channel lengths. Subthreshold curves of a) conventional 2D FETs and b) 2D NC-FETs. 2D NC-FETs exhibit robust scaling behavior compared to the 2D FETs. c) Impact of scaling on subthreshold swing; **Δ**SS/SS$_{LC}$ indicates the difference of SS at the current channel length compared to the SS of the longest channel device. d) Extracted I_{ON}/I_{OFF} ratio for different L_{ch} devices compared with top-gated 2D NC-FETs in the literature (denoted as the Ref [26]).

Implications from the capacitive network (Fig. 2(b)) in the devices may be contributing to the improved scaling capability of the 2D NC-FETs. The gate stack capacitance can be expressed as C_{stack},[22]

$$C_{stack} = \left(\frac{1}{C_{dev}} + \frac{1}{C_{FE}}\right)^{-1} \quad (1)$$

Accordingly, it can be derived from this equation that a lower negative C_{FE} results in a larger C_{stack}, which implies stronger gate control.

The small-signal capacitance circuit shows that a 2D NC-FET can be regarded as an intrinsic 2D FET in series with an HZO FE capacitor. The Landau-Khalatnikov (LK) equation describes the electrical behavior of the HZO FE capacitor,[32] and C_{FE} can be calculated using Landau coefficients:

$$C_{FE} = \left(\frac{1}{2\alpha t_{FE} + 12\beta t_{FE} Q_{av}^2 + 30\gamma t_{FE} Q_{av}^4}\right)$$

(2)

where α, β and γ are Landau coefficients, and t_{FE} is the ferroelectric thickness. For a stabilized FE material with first-order phase transition, α,β < 0 and γ > 0.[25,33] It has been reported that reducing the channel length results in an increased inner fringing field that induces a larger $|P_{FE}|$.[24,33] This leads to a decrease in $|C_{FE}|$ (C_{FE} being less negative) and increase in C_{stack} when β is negative.[34] Thus, as coupling of inner fringing fields to the FE increases with scaling, short-channel devices exhibit enhanced potential amplification and gate control. Note that the back-gated device structure is fully overlapped with S/D contacts, the coupling of inner fringing fields across the FE is expected to be fairly uniform comparing to devices without fully overlapped S/D structure. On a side note, the appearance of ferroelectricity in nanometer-size ferroelectrics generally stems from the emergence of multidomain states,[35,36] which can over-respond to an applied charge, hence impacting the NC effect.[37] Studies can be conducted in the future to take the multidomain states into account for the scaling behavior observed in this study.

The results we observed for the subthreshold behavior in 2D NC-FETs can also be explained by the design principles in its small-signal capacitance circuit.[19] The SS derived is,

$$SS = \frac{2.3k_BT}{q}\frac{1}{\frac{\partial \Phi_s}{\partial V_{gs}}} = \frac{2.3k_BT}{q}\left(1+\frac{C_{2D}}{C_{ox}}\right)\left(1-\frac{C_{dev}}{|C_{FE}|}\right) \quad (3)$$

where k_B is the Boltzmann constant, T is the temperature, q is the elementary electronic charge, Φ_s is the surface potential in the channel, C_{2D} is the 2D semiconductor channel capacitance, C_{ox} is the dielectric capacitance. As the channel length scales down, SS decreases with the reduction of $|C_{FE}|$. The improvement in subthreshold behavior we demonstrated for short-channel 2D NC-FETs is consistent with the above derivation from the small-signal capacitance circuit.

Comparing the performance of the short-channel devices in this work to that of a previously reported top-gated MoS_2 NC-FET with HfO_2 (4 nm)/P(VDF-TrFE) (26 nm) gate stack layers highlights the pronounced improvement from this work.[26] In the top-gated devices, the transfer characteristics of channel lengths ranging from 42 to 130 nm were measured; however, as the channel length scaled, the SS became drastically larger and the on/off-current ratio degraded. The authors pointed out that the SS changes only

slightly when the channel length is greater than 60 nm, indicating the source of the degradation to be from SCEs. In contrast, the back-gated 2D NC-FETs with HZO from this work show promising scaling behavior. While there remains some debate regarding which device structure is most favorable for NC-FETs, our results make it clear that the NC effect provides more favorable scalability when properly implemented.

In summary, we experimentally demonstrated 2D NC-FETs using MoS_2 with CMOS-compatible HZO as the FE to achieve remarkable robustness to channel length scaling. From a bottom-gated structure, we compared 2D FETs with 2D NC-FETs having exactly the same gate stack (with or without an anneal) to investigate the NC impact on the operation and performance of the devices across many gate lengths. Finally, we revealed unconventional behavior when scaling down to 20 nm, including stronger gate control and preferential performance from the 2D NC-FET. Based on these experimental results, and analysis of the capacitive network, we find that the NC effect is beneficial to channel length scaling and enhances gate control as length is scaled.

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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