International Journal of Heat and Mass Transfer 184 (2022) 122287

Contents lists available at ScienceDirect

International Journal of Heat and Mass Transfer

journal homepage: www.elsevier.com/locate/hmt

Multi-objective optimization of 3D printed liquid cooled heat sink with guide vanes for targeting hotspots in high heat flux electronics

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ARTICLE INFO

Article history:
Received 2 August 2021
Revised 23 October 2021
Accepted 18 November 2021
Available online 3 December 2021

Keywords:
Hotspot-targeted cooling
Electronics liquid cooling
Multi-objective optimization
CFD modeling
3D printed heat sink
Compute
AI
Neural network

ABSTRACT

The data center industry is currently faced with surging energy demands and a growing carbon footprint. Beside these, the industry is also faced with increasing chip power densities and thermal stresses, which can be attributed to the integration of multiple cores into a single chip. This paper presents a novel hot spot targeted cooling approach, the goal of which is to reduce both the cooling device's thermal resistance and chip thermal stresses while also lowering the pressure drop and pumping power required to cool the chip. The approach allows for the temperature of the liquid leaving the chip to be maximized, which can enable different heat recovery potentials. Multiple techniques were used to improve the heat sink's thermohydraulic performance, including a direct chip-attached heat sink, distributed water jet impingement inlets, and embedded guide vanes. A multi-objective optimization study was conducted to minimize the chip's temperature non-uniformity, thermal resistance, and pumping power. For optimization, a Bayesian-based learning technique was coupled with a genetic algorithm, which was then employed. The results show that the optimal design was comprised of variable fin density and profile in the hot spot and background regions of the chip. The optimized design showed a benchmark thermal resistance of 0.036 °C/W and a chip non-uniformity index as low as 0.81 °C. It outperforms the other hot spot targeted heat sinks that have been presented in previous literature, meanwhile also consuming relatively low pumping power.

1. Introduction

Thermal management has become a bottleneck to the development of many industries [1–5], such as the electronics industry [6–12]. Many issues with thermal management are attributed to the increase in waste heat dissipated by Information Technology Equipment (ITE), which is driven by technological advancement and the rising demand for digital services [13]. Data Centers (DC), which represent the backbone of today's digital world, house large groups of networked ITE. Therefore, the level of demand for DC services has surged dramatically. Furthermore, the projected applications of artificial intelligence promise to increase the demand even further [14]. Consequently, DC energy consumption has grown substantially. It is well known that DCs are energy-intensive buildings. DC energy consumption accounts for approximately 1.3% of the total worldwide electricity consumption [15], with their cooling systems responsible for 30–50% of their total energy consumed [16].

Increased demand for DC services will increase not only the energy consumed, but also the heat dissipated by ITE [17], which necessitates the employment of high capacity cooling systems. Air-cooling technologies, which are the most widely adopted type of cooling system in data centers, suffer from low heat transfer coefficients, energy inefficiencies, and noise problems. This has prompted a shift away from air cooling and toward alternative technologies like single-phase liquid cooling and two-phase cooling. According to the literature [18–20], single-phase on chip liquid cooling techniques have proven to be an effective, feasible, and energy efficient solution to cooling high heat flux electronics. Hence, single-phase liquid cooling has attracted the attention of many researchers as a potential substitution for conventional air-cooling.

Bayraka et al. [21] compared the thermal-hydraulic performance of a microchannel heat sink with various geometric struc-

Abbreviations: COI, coefficient of improvement; COP, coefficient of performance; DC, data center; E, error; GA, genetic algorithm; ITE, information technology equipment; RANS, Reynolds averaged Navier-Stokes.

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https://doi.org/10.1016/j.ijheatmasstransfer.2021.122287
0017-9310/

Nomenclature

$C_{1\varepsilon}$, $C_{2\varepsilon}$, C_{μ}	coefficients in Eqs. (5) and (6)
F	body forces
G	generation of turbulent kinetic energy
h	heat transfer coefficient Kinetic energy
k	thermal conductivity
ṁ	mass flow rate
P	pressure
q	heat flux
Q	volume flow rate
R^2	coefficient of determination
R_{th}	thermal resistance
S	volumetric heat generation
S_k, S_ε	source terms
T	temperature
u	velocity
Y_M	fluctuating dilation incompressible turbulence
α, β	regularization parameters
ε	rate of turbulent kinetic energy dissipation
μ	dynamic viscosity
μ_t	turbulent viscosity
ρ	fluid density
σ_k,σ_ε	turbulent Prandtl numbers
τ_{ij}	stress tensor
Φ	dissipation function
ψ	chip uniformity index

Subscripts

B	buoyancy force
bg	background
ch	channel
Eff	effective
f	fins
hs	hot spot

tures. Naphon et al. [22] experimentally investigated the thermal characteristics of jet impinging TiO2 nanofluids in a micro-channel heat sink. Their results showed that suspending nanofluids with a 0.015% concentration in de-ionized water increased the convective heat transfer by 18.56%. In a later study [23], they extended their investigation to multiple configurations using artificial neural networks and CFD models. Vajdiet al. [24] investigated the thermo-hydraulic characteristics of a microchannel heat sink made from a ZrB2 ceramic. Lee et al. [25] proposed a cylindrical pin fin heat sink model with variable pin pitch and performed a topology optimization. Xiao et al. [26] applied inclined parallelepiped ribs in a microchannel heat sink to realize the optimized flow pattern. Awais and Man-Hoe Kim [27] performed a numerical and experimental study on the impact of header geometry on heat sink performance. They found that using the optimized geometry of the header resulted in a 17% increase in the overall heat transfer coefficient and a 43% decrease in the pressure drop. All of these studies investigated heat sources with a uniform heat flux to imitate chips.

In the real world, it has become commonplace for multiple cores to be fabricated onto a single chip to improve its performance. This results in a non-uniform heat flux within the chip, as opposed to the uniform heat flux considered in the aforementioned studies. Without adopting the appropriate thermal management solution, significant temperature gradients will be observed within the package, thereby increasing the chip's thermal stresses. This can produce circuit imbalances in Complementary Metal–Oxide–Semiconductor (CMOS) devices and inevitably presents reliability concerns [28]. Only a relatively small portion of the existing studies have focused on investigating chips with a non-uniform heat flux. Kumar and Singh [29] introduced an approach to managing temperature non-uniformity of a chip by using intentional flow maldistribution within a mini-channel heat sink. Ansari and Kim [30] presented a microchannel-pinfin hybrid heat sink for cooling microprocessors with heterogeneous power distributions. Lorenzini et al. [31] studied the use of embedded micro gaps with variable pin fin clustering for cooling non-uniform heat sources. Feng et al. [32] investigated of a 3D chip with non-uniform cooling heat flux by implementing annular-cavity micro-pin fins. Yan et al. [33] proposed using thermo-responsive shrinkage hydrogels to regulate mass flow rate by driving more coolant to the hot spot. This year, a comprehensive literature review that discussed the temperature uniformity enhancement of electronic devices was introduced by Yan et al. [33].

In this work, a new concept for targeting hotspots inside chips is introduced. This novel concept proposes building guide vanes inside the heat sinks to drive the coolant directly from the heat sink manifold to the hot spots. Consequently, this ensures delivery of a significant portion of coolant with the lowest possible temperature directly to the hot spot. For the purpose of this study, the guides were intended to guide the fluid to the hot spot, enhance fluid penetration, and reduce caloric resistance within the heat sink. Note, there are other benefits to using them as well. To further enhance the thermal performance, 3D laser printing is used to build the guide vanes within the heat sink and print the heat sink directly onto the chip surface. This is possible because 3D printing eliminates the need for thermal interface materials and can overcome the geometrical restrictions associated with the manufacturing processes of conventional cold plate heat sinks [34]. However, 3D printing heat sinks directly onto the chip is a new research field to be explored, with only a few research articles have discussed the potential of 3D printed heat sinks [35–37]. Based on the above, this work will make a significant contribution to the body of literature. A third technique, which is jet impingement, is utilized in this concept to improve the heat sink's performance. Jet impingement is a widely adopted approach for improving heat transfer in heat sinks [23]. This is because jet impingement has a high heat transfer coefficient, especially at the stagnation region [38]. One drawback of impingement cooling is that it exhibits a relatively small heat transfer area [39]. Thus, by using multiple inlet jets, the overall heat transfer area can be increased. Consequently, the gross heat transfer improves and the pressure drop across the heat sink will decrease. Jet impingement can conquer the typical design limitations of a parallel flow heat sink, which are a significant pressure drop and a large difference in the inlet and outlet fluid temperature.

This study proposes a new concept for targeting hot spots and introduces a new heat sink designing methodology. The concept allows for the design of a cold plate heat sink with minimum thermal resistance and maximum chip temperature uniformity, especially for high heat and non-uniform heat flux applications. The merit of adopting this concept is not limited to improving a heat sink's thermal performance but also includes providing a practical solution that can be implemented for various chip heat maps. Beside introducing a new 3D printed hot spot targeted design, this study also benchmarks the thermal performance of a liquid-cooled hot spot targeted heat sink by achieving the lowest possible chip temperature non-uniformity. To facilitate a comparison of the thermal performance of different designs, a new index, which is called the Coefficient of Improvement (COI), is introduced. This index measures the amount of improvement that various designs can achieve compared to the baseline.

Another primary objective of this study is to perform a robust multi-objective optimization to identify designs that can provide an optimal fin design compared to the baseline cases considered. Compared to previous work conducted in the literature, this

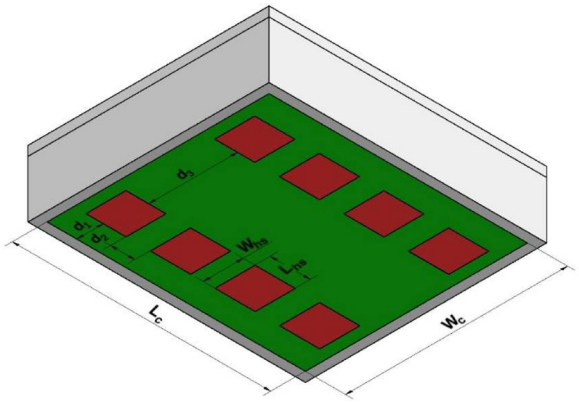


Fig. 1. A schematic diagram of the heat map distribution.

Table 1
Geometrical parameters of the heat map.

Parameter	Symbol	Value
Chip width (mm)	W_C	23.2
Chip length (mm)	L_C	27
Chip thickness (mm)	H_C	0.525
Hot spot width (mm)	W_{hs}	4.181
Hot spot length (mm)	L_{hs}	4.197
Distance 1(mm)	d_1	2.779
Distance 2 (mm)	d_2	2.553
Distance 3 (mm)	d_3	9.28
Chip material	-	Silicon
Background heat flux (W/cm^2)	-	20
Hot spot heat flux (W/cm^2)	-	150

study's optimal heat sink design achieved a better response than the prior performance of other studies in terms of the thermal resistance and pressure drop.

2. Numerical model and hot spot targeted concept

2.1. Heat map details

A highly non-uniform heat map for a typical multicore chip is adopted from a previous study [5] to explore the proposed concept of targeting hot spots. This heat map consists of 8 dies fabricated onto a single chip. Thus, the chip is divided into hot spots zones that represent the cores and the background zone. The heat dissipation rate in the hot spots is uniform for all hot spots and is specified to be 150 W/cm^2, while the background dissipates heat at a lower rate of 20 W/cm^2. The total area of each chip is 626.4 mm^2, and the hot spots occupy around 140.4 mm^2 out of the entire chip area. Accordingly, the total power dissipated by each chip equals 307.78 W. Seeing as it is made of silicon, this chip's thermal conductivity is 149 W/m °C. Fig. 1 illustrates the distribution of the hot spots within the selected chip. The hot spots are shown in red and the background is shown in green. The heat dissipation rate, properties, and geometrical parameters of the chips and mainboard (including those shown in Fig. 1) are summarized in Table 1.

2.2. Baseline design

The objective of this study is to introduce a new concept that targets hot spots inside chips. Hence, it would be convenient to compare the proposed concept to a baseline design thereby emphasizing the advantages of using the proposed concept. The baseline was chosen from the literature, given that similar designs were adopted in a reasonable number of studies [23,40,41]. The general idea of this design is to have a single impingement inlet at the center of the heat sink and four outlets at its sides, as illustrated in Fig. 2. The values of the geometrical parameters shown in Fig. 2 are provided in Table 2.

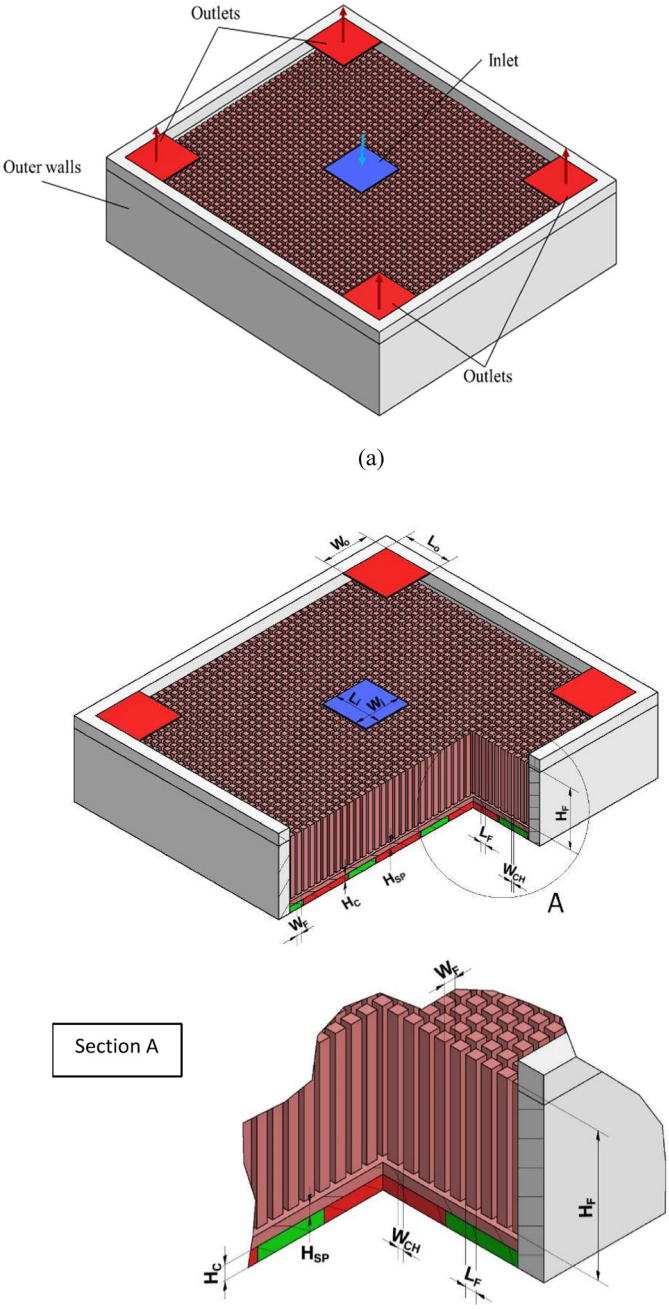


Fig. 2. Schematic view of the baseline design with detailed geometric parameters.

2.3. Hotspot targeted heat sink concept description

The hotspot targeted cooling concept proposed in this work utilizes multi-jet impingement and pin fin heat sink architecture. The coolant inlets are positioned on top of the heat sink, as shown in Fig. 3(a), while the outlets are located in the corners and in the middle of the top surface. There are many advantages to using multiple inlets and outlets in this configuration. Two such advantages are the capacity to deliver the maximum amount of coolant directly to the hot spots and reduce the pressure drop throughout the heat sink. To take full advantage of the distributed inlet configuration, guide vanes are built within the heat sink fins around the

Table 2
Geometrical parameters of the baseline design.

Parameter	Symbol	Value
Inlet width (mm)	W_i	4
Inlet length (mm)	L_i	4
Outlet width (mm)	W_O	4
Outlet length (mm)	L_O	4
Fin width (mm)	W_F	0.4
Fin length (mm)	L_F	0.4
Fin height (mm)	H_F	5
Printed spreader height (mm)	H_{sp}	0.2
Distance between fins (mm)	W_{ch}	0.2

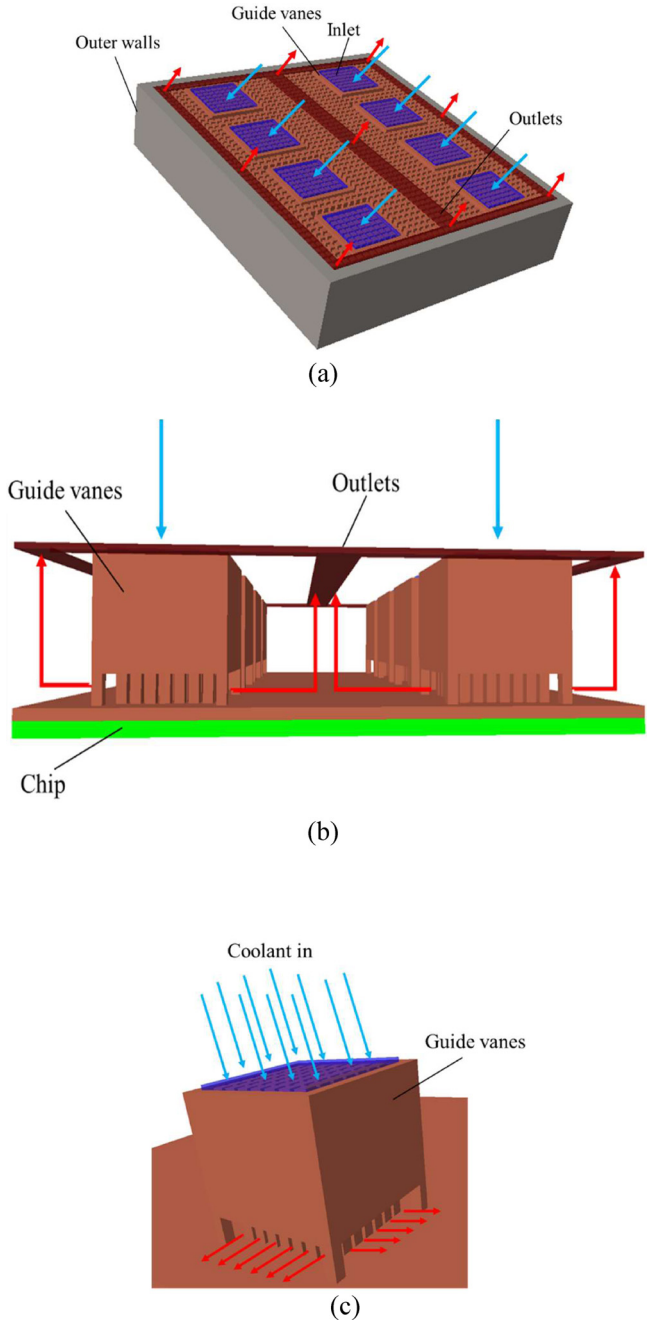


Fig. 3. Schematic view of the hotspot targeted design with multiple inlets and fluid guide vanes.

hot spots. These guide vanes form walls with small openings at the bottom, as shown in Fig. 3(b). 3D printing is used to create the guide vanes while also making the heat sink fins from the same material. By printing these guide vanes, the coolant is guaranteed to go directly the hot spot and the penetration of the coolant through the pen fins is assured. Fig. 3(c) demonstrates how the proposed hot spot targeted design passively distributes the coolant to the hot spots in the heat sink and how the coolant then leaves the heat sink.

2.4. Heat sink model and grid generation

In this study, the simulation domain was reduced to only a quarter of the original heat sink domain. This reduction was possible because of the inherent symmetry of the heat map and geometry of the heat sink in the domain, as shown in Fig. 4(a) & (b). Therein, the planes of symmetry are marked by dashed black lines. As a result, the computational cost of the simulation was significantly reduced while still fully capturing the physics inside the cold plate heat sink. Fig. 4(c) depicts the heat sink domain after its reduction.

Following are the boundary conditions applied for the computational domain:

- Outer walls and heat sink cover are adiabatic
- Constant flow rate at inlets
- Constant pressure at outlets
- Symmetrical walls along lines of symmetry
- Constant heat flux at the different chip regions

When developing a CFD model, an appropriate grid must be generated in order to ensure the model's reliability. In the model for this study, a hexahedral structured grid was deployed over the solution domain. The advantage of using this type of cell is that it assures a high-quality grid will be generated. Also, it can overcome the typical issues associated with other types of cells, like skewness and aspect ratio [42]. For the same quantity of cells, a hexahedral grid will produce the most accurate results among other grid types, such as tetrahedral, pyramid, and triangular.

Another factor to consider for grid quality is the number of cells. A relatively low number of cells can result in large errors in the solution, while a relatively large number of cells can increase the computational cost of simulation significantly. To that end, a grid independence study was performed to find a compromise between the results' accuracy and the computational cost. The grid independence study was executed considering the pressure drop across the heat sink and the maximum chip temperature recorded at the hot spots. The results of the grid independence study are illustrated in Fig. 5.

Since a CFD analysis will find a numerical based solution, the results will vary according to the number of grid cells used. For this study, a broad range of grids was considered before the optimal number of grids (4.3–43.8 million) was identified. For the baseline scenario, the grid independence study results varied only slightly when the number of grid cells went above 12 million. From there, the number of cells was further increased to see its impact on the results. When the number of grid cells went above 19.9 million, the maximum chip temperature and pressure drop varied by less than 3%.

With this in mind, 19.9 million grid cells were used to execute all of the analyses for this geometry. However, throughout the study, the number of grid cells was modified to accommodate various heat sink geometries. Finally, it is worth mentioning that higher grid concentration was considered in the regions with high gradients while generating the grid.

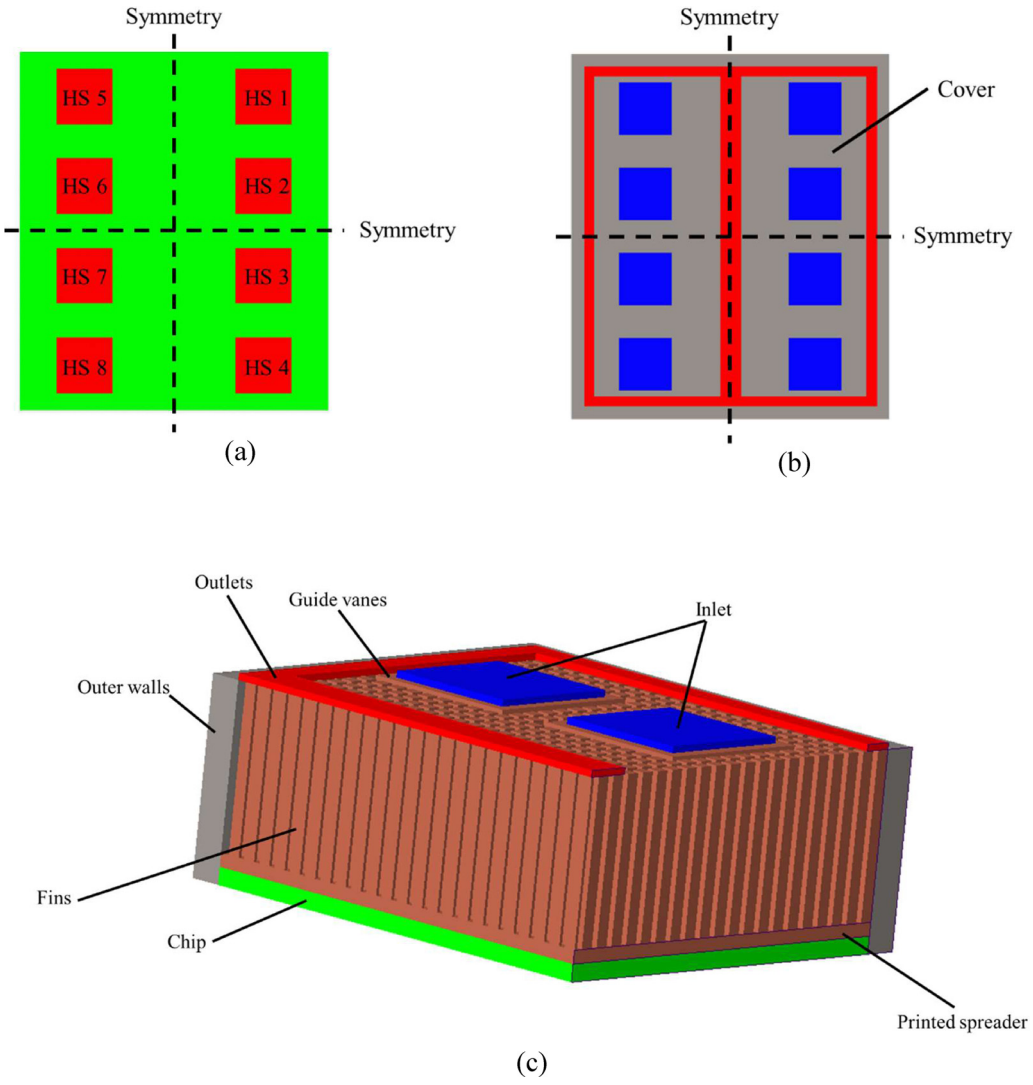


Fig. 4. Schematic view of the symmetry boundary conditions and the resultant solution domain (a) heat map (b) heat sink (c) solution domain.

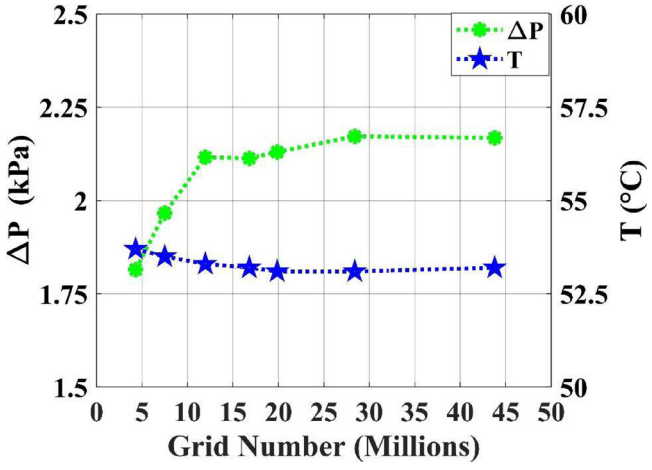


Fig. 5. Grid sensitivity analyses.

2.5. Assumptions and governing equations

6SigmaET CFD code was adopted for conducting all the simulations in this study. This finite volume code is designed specifically for simulating electronic cooling devices. Hence, it is capable of developing precise models of electronic cooling equipment such as heat sinks. The following are the assumptions applied while solving the numerical models:

- Steady state is attained
- Incompressible flow
- Adiabatic outer walls
- Wall roughness and gravity effects are negligible
- Small Brinkman number (Br = Pr × Ec) value is maintained i.e. negligible heat generation due to viscous friction
- Constant thermo-physical properties in the solid and liquid domains
- The coolant flow rate is uniformly distributed to the multiple inlets
- Radiative heat transfer has negligible impact.

Accordingly, the governing equations used for solving the numerical model are given below.

Continuity equation:

$$\nabla \cdot \vec{u} = 0 \tag{1}$$

Momentum equation:

$$\rho_f \ (\vec{u}.\nabla) \ \vec{u} = -\nabla P + \mu_f \nabla^2 \vec{u} \tag{2}$$

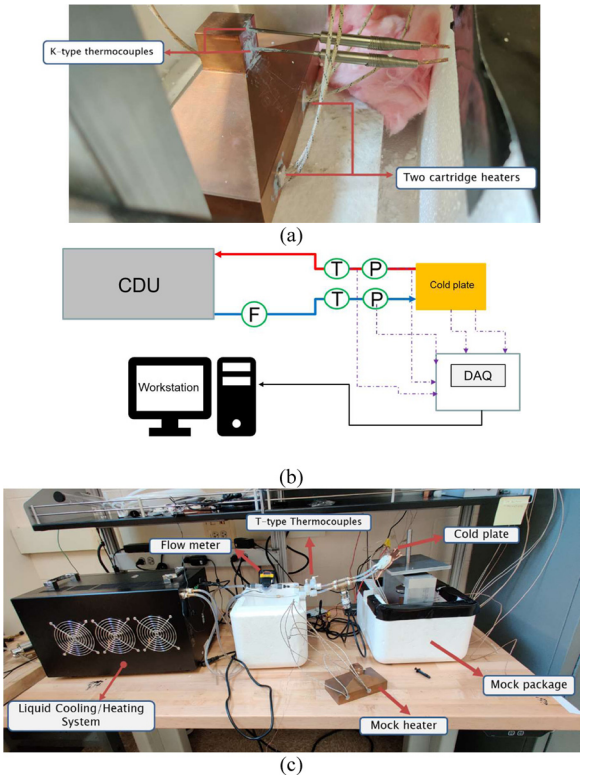


Fig. 6. Schematic and actual view of the bench top experimental setup for single cold plate characterization (a) mock heater (b) schematic of the experimental setup (c) experimental setup.

Table 3
Specifications of instrumentation used in the experimental apparatus.

Instrument	Specifications
Flow sensor	Omega FTB314D (full scale accuracy: ± 6%)
Thermocouple	T-type (accuracy: ± 1 °C)
Pressure transducer	Omega PX309050A5V (accuracy ± 0.8 kPa)
Cooling distribution unit	ALH-2000 (cooling capacity 2000 W)

Energy equation in the liquid domain:

$$\rho_f \; c_{\rho_f} \; (\vec{u}.\nabla) \; T_f \; \vec{u} = K_f \; \nabla^2 T_f \tag{3}$$

Energy equation in the solid domain:

$$\nabla^2 T_S = 0 \tag{4}$$

Reynolds Averaged Navier-Stokes (RANS) was utilized to account for the fluid flow dynamics inside the heat sink. A standard k-ε turbulence model is coupled with the continuity, momentum, and energy equations for simulating the solution domain. The standard k-ε turbulence model governing equations are shown below [43–45]:

Turbulent kinetic energy k equation:

$$\rho\vec{u}.\;\nabla k = \nabla.\left(\left(\mu + \rho\frac{c_\mu\;k^2}{\sigma_k\varepsilon}\right)\nabla k\right) + \;\rho\; c_\mu\frac{k^2}{\varepsilon}\left(\nabla\vec{u} + (\nabla\vec{u})^T\right)^2 - \rho\varepsilon \tag{5}$$

Rate of dissipation of the turbulent kinetic energy ε equation:

$$\rho\vec{u}.\nabla\varepsilon = \nabla.\left(\left(\mu + \rho\frac{c_\mu\;k^2}{\sigma_\varepsilon\varepsilon}\right)\nabla\varepsilon\right) + \;\rho\; c_{\varepsilon1}c_\mu k\left(\nabla\vec{u} + (\nabla\vec{u})^T\right)^2 - \rho\; C_{\varepsilon2}\frac{k^2}{\varepsilon} \tag{6}$$

Finally, a standard wall treatment was implemented with the standard k-ε. This wall treatment assumes that the grid near the wall lies within the region where the logarithmic law of the wall applies. This assumption is valid since those calculations showed that the y^+(a dimensionless parameter that accounts for the wall coordinate) value falls between 30 and 300 [46].

2.6. Performance evaluation parameters

The key performance parameters for evaluating heat sink designs are the pressure drop and thermal resistance. In addition to these performance parameters, the uniformity index, Coefficient of Improvement (COI), and Coefficient of Performance (COP) were introduced. The purpose of using these parameters was to evaluate the impact of using different heat sink designs on chip temperature uniformity and to carry out a fair comparison between other hot spot targeted designs. The thermal resistance can be calculated considering the maximum chip temperature and the total chip power using the following equation [47]:

$$R_{th} = \frac{T_{C,max} - T_\infty}{q_{bg+}\sum q_{hs,i}} \tag{7}$$

As mentioned before, using conventional heat sink designs can result in overcooling regions with low heat dissipation and undercooling regions with high heat dissipation.

To compare various designs in terms of reducing chip non-uniformity, it is essential to develop a parameter for assessing their impact on chip temperature uniformity. Previous studies adopted correlations that calculated the temperature uniformity using the maximum and minimum chip temperature without considering the different regions of heat dissipation. These correlations cannot provide adequate comparison of different heat sink designs

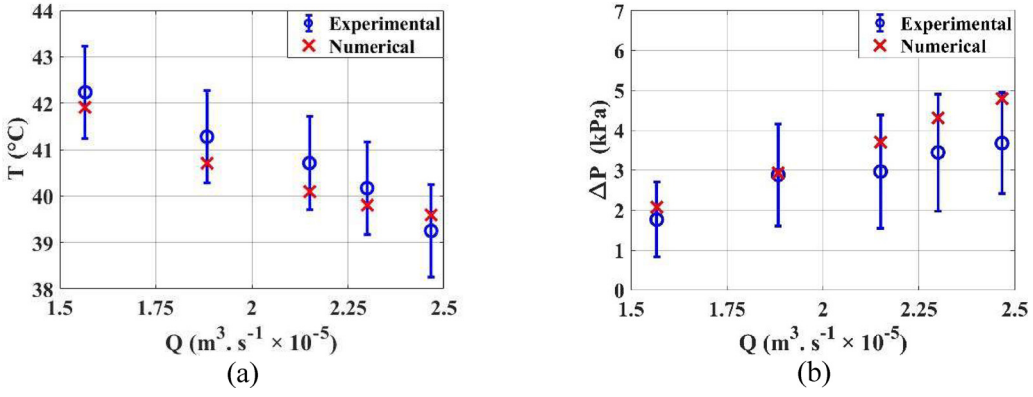


Fig. 7. Validation of numerical model with experimental results (a) temperature (b) pressure drop.

Table 4
Calculated performance parameters for the baseline, hot spot targeted designs without guide vanes, and hot spot targeted designs with guide vanes.

Design	Flow rate ($m^3/s \times 10^{-5}$)	$T_{max,\ c}$ (°C)	R_{th} (°C /W)	ψ (°C)	COI	ΔP (kPa)	COP ($\times 10^3$)
Baseline	3.33	53.2	0.059	2.25	-	1.9	4.7
Hot spot targeted without guide vanes	3.33	50.5	0.051	1.2	2.2	0.517	17.8
Hot spot targeted with guide vanes	3.33	49.4	0.047	0.93	3.04	0.8	11.5

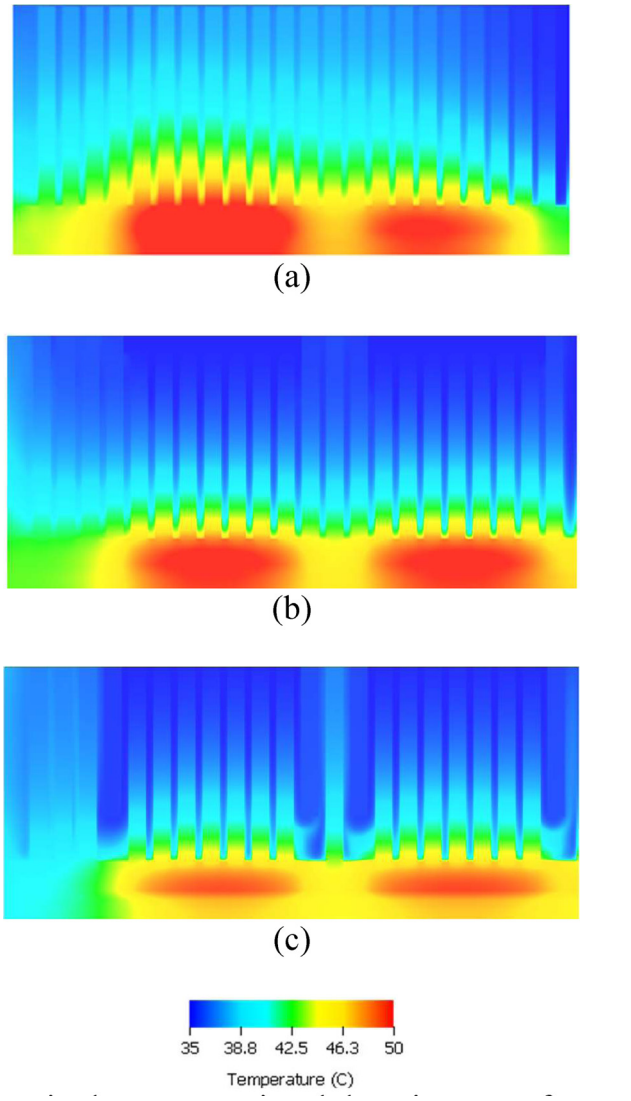


Fig. 8. Temperature contours in the computational domain center for (a) baseline design (b) hot spot targeted without guide vanes (c) hot spot targeted design.

because different chips will have different heat dissipation maps. Based on this, a chip uniformity index was defined as follows:

$$\psi = \frac{T_{hs,\ max} - T_{bg,\ min}}{q_{hs}/q_{bg}} \tag{8}$$

Since the objective of heat sink design is to reduce thermal resistance and temperature non-uniformity, COI can be defined by the equation below, which estimates the overall thermal performance improvement by comparing the modified design with the baseline design.

$$COI = \frac{R_{th,old} \cdot \psi_{old}}{R_{th,new} \cdot \psi_{new}} \tag{9}$$

Finally, COP, a thermo-hydraulic performance parameter, was introduced to account for the pressure drop through the heat sink and the associated pumping power. The COP also correlates the pumping power to the heat picked up by the heat sink i.e., the chip power. Thereby, the COP can be used to evaluate the thermo-hydraulic efficiency of various heat sinks attached to various chips. It can be calculated using:

$$COP = \frac{\dot{m} c_p \left(T_c^o - T_c^i\right)}{\Delta P \cdot Q} \tag{10}$$

2.7. Validation

Validation was carried out to ensure the viability of the numerical code, assumptions, and boundary conditions. Having validated the numerical approach, when is used to investigate new thermal management technologies and new heat sink designs its results will be accurate. Indeed, CFD numerical techniques have demonstrated predictability and accuracy in a wide range of applications [48–50]. With this in mind, the authors determined its feasibility for use in this study.

A test apparatus was built to validate the aforementioned numerical modeling methodology. The validation experiment was performed using a mock heater with the commercially available cold plate. This is because of the unavailability of non uniform heat flux (similar to what exists in the actual chips) and the heat sinks 3D printing tools. However, these tools exist and are well defined in the literature [51,52].

The mock heater surface area was approximately the same as the proposed chip. This mock heater was designed to assure a uniform surface temperature and to accurately measure the heat transferred from the heater to the heat sink. The latter was done by placing it in a box filled with fiberglass insulation material and installing two thermocouples below the cold plate, as shown in Fig. 6(a). These thermocouples measured the longitudinal temperature difference over a specified distance. Thus, it can be used to calculate the amount of heat transferred to the heat sink using Fourier's law. The experimental setup schematic is shown in Fig. 6(b), while the details of the instruments are provided in Table 3.

The validation experiment was conducted considering the thermal resistance of the heat sink at different coolant flow rates, as shown in Fig. 7. The coolant chosen for this work was deionized water, which has superior thermophysical properties and a high boiling point [53].

Comparing the numerical results to the experimental ones reveals that the largest discrepancy for the maximum case temperature was observed when the flow rate was equal to 2.15 $m^3/s \times 10^{-5}$ (1.29 LPM), which was lower than the thermocouple's accuracy. The numerical results fell within one standard deviation of the experimental ones for the pressure drop values. Considering this, the numerical results show good agreement with the experimental data. Now, with the reliability of the numerical model validated, various heat geometries can be investigated.

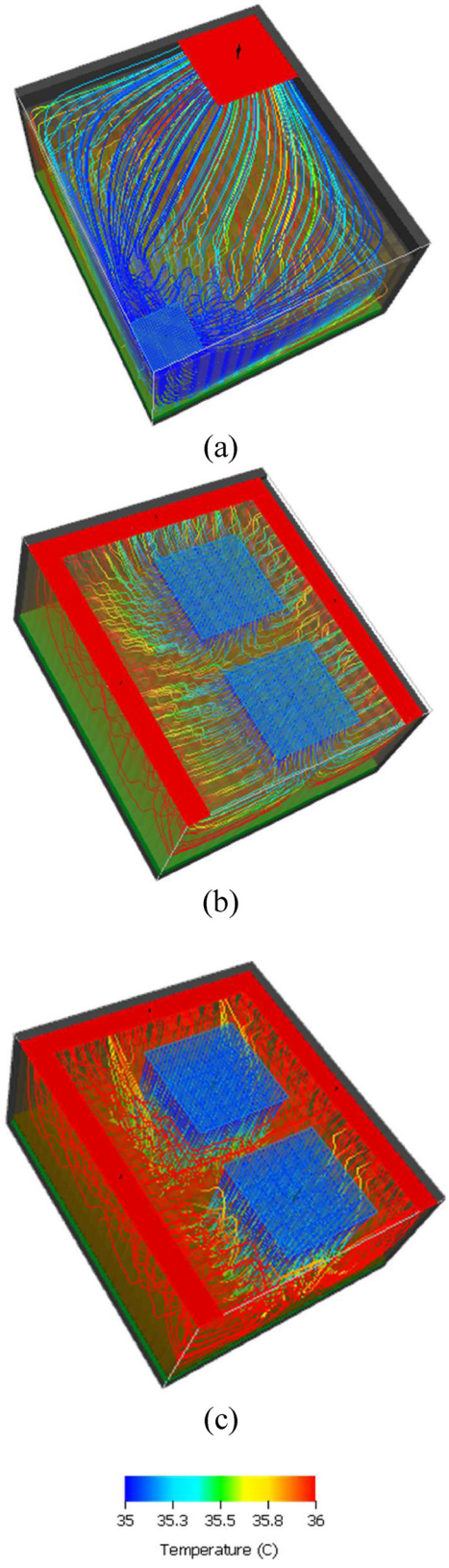


Fig. 9. Coolant flow streamlines colored based on temperature for (a) baseline design (b) multiple inlets design (c) hot spot targeted design.

3. Results and discussion

3.1. Baseline case vs proposed concept

To recognize the merit of adopting the distributed inlets and guide vanes designs over the baseline design, a comprehensive comparison was executed. In this comparative study, three different designs were considered. The first design was the baseline design. The second design was similar to the hot spot targeted design, but without the presence of guide vanes. This case was made to demonstrate how the absence of the guide vanes would affect the heat sink's thermal resistance. The third design was the hot spot targeted design, which included both the distributed inlets and guide vanes. For a fair comparison, the same operating conditions and geometrical parameters were maintained throughout the simulations. The results of the comparative study, including the thermo-hydraulic performance parameters, are summarized in Table 4.

From the results, it can be observed that using multiple inlets improved the heat sink's thermal performance and reduced its pressure drop. Furthermore, the guide vanes were found to reduce the heat sink's thermal resistance and chip non-uniformity in both the second and third designs. However, the pressure drop slightly increased with the use of guide vanes in design three. Although both a low thermal resistance and pressure drop are preferable, improving the thermal performance at the expense of a slight increase in pressure drop is acceptable.

Comparing the baseline design with the hot spot targeted design reveals that the proposed hot spot targeted concept significantly improved the heat sink's thermal and hydraulic performance. When the delivered flow rate was 3.33 $m^3/s \times 10^{-5}$ (2 LPM), the thermal resistance of the heat sink decreased from 0.059 to 0.047 (°C/W) while the chip uniformity index decreased from 2.25 to 0.93. This means that the maximum chip temperature was reduced and the temperature gradient inside the chip was also reduced. The total improvement in the heat sink's thermal performance at this flow rate, represented by the COI, was calculated to be 3.04. The pressure drop was reduced by 1.1 kPa. This indicates that energy can be saved through a reduction of pumping power consumption.

Side views of the temperature contours for all three designs are shown in Fig. 8. From the figure it can be noted that HS 2 exhibits a lower temperature than HS 1 in the baseline design. This occurred because a larger amount of coolant was delivered to HS 2, which was closer to the inlet. With the use of multiple inlets, the variation in temperature between the hot spots was reduced because each received the same amount of coolant. The figure also illustrates that the guide vanes reduced the XX temperature values, which resulted in better chip temperature uniformity.

Fig. 9 further illustrates the flow distribution inside the heat sink. This figure depicts the coolant streamlines inside the heat sink for all three designs. As expected, when the flow was not guided and the inlet was located at the chip's center, a small portion of the coolant was delivered to HS 1 and a larger portion was delivered to HS 2. The streamlines also show that a considerable portion of the coolant bypassed both hot spots, indicating that it experienced a negligible amount of heat transfer. For the multiple inlet design without guide vanes, the flow was almost equally distributed across the hot spots but the fluid penetration was not ideal. This indicates that a large portion of coolant received only a small amount of heat while passing through the heat sink, which reduced the heat sink's thermal performance.

For the multiple inlet design with guide vanes, the streamlines show that the coolant absorbed a considerable amount of heat while it passed over the hot spots and through the heat sink. This is also illustrated by the heat transfer rate, which is affected by

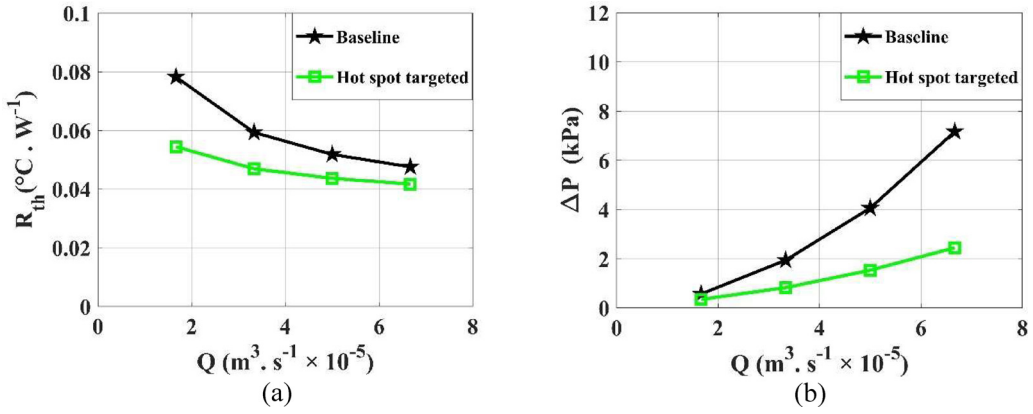


Fig. 10. (a) Thermal resistance (b) pressure drop variation with flow rate for the baseline design, and the hot spot targeted design.

the temperature gradient. Thus, the maximum heat transfer occurs near the hot spots since they exhibit the highest temperatures in the heat sink. The hot spot targeted design assured coolant penetration throughout the heat sink and enhanced heat transfer, thus the hot spot temperatures were reduced and the overall chip temperature uniformity improved.

As for the hydraulic performance, the multiple inlet designs reduced the pressure drop across the heat sink for two main reasons. First, distributing the flow into multiple inlets rather than one inlet remarkably reduced the flow speed in these inlets, thereby reducing the turbulence intensity. Second, this configuration shortened the path between the inlets and outlets, reducing the total distance traveled by the coolant inside the heat sink.

To explore the impact of flow rate variation on the baseline and hot spot targeted designs, the behavior of these two heat sinks was studied over the flow rate range of 1.67–6.67 $m^3/s \times 10^{-5}$ (1–4 LPMs). Fig. 10 shows the P-Q and R-Q curves for the baseline design and the hot spot targeted design. The hot spot targeted design appeared to have a superior performance in terms of pressure drop and thermal resistance over the baseline design for all of the investigated flow rates. The results showed that the baseline design was more sensitive to flow rate variation than the hot spot targeted design. At low flow rates, there was a significant difference in the thermal resistance of each design. However, as the flow rate increased the difference in the thermal resistance for each design decreased. This observation can be linked with one previously made about how some hot spots received a smaller portion of the coolant. Considering this, an increase in the flow rate guaranteed that more coolant was delivered to the hot spots, which lowered the thermal resistance. Since the hot spot targeted design already delivered sufficient coolant to the hot spots, an increase in the flow rate did not significantly improve the calculated thermal resistance. As for pressure drop, it was observed that the difference in the calculated pressure drop for each design tended to increase as the flow rate increased. This was expected, seeing as the coolant velocity in the baseline design was equal to that in the multiple inlet design.

Finally, Fig. 11 illustrates the change in the chip uniformity index, COI, and the COP of both designs with a changing flow rate. In addition to the analyses of pressure drop and temperature, the COI and COP provide meaningful information about the overall performance of the heat sink. The chip uniformity index shows that increasing the coolant flow rate resulted in a similar thermal resistance for both designs. Note, the baseline design still overcooled some regions within the chip, particularly at the center. For this reason, the COI indicates that the thermal performance of the hot spot targeted design was considerably better than that of the baseline design. As for the COP, it shows a sizeable difference in the pumping power of the two designs at a high flow rate, because pumping power is dependent on both the flow rate and pressure drop.

3.2. Identifying the design alternatives

To build upon the proposed hot spot targeted concept, several different pin geometries were investigated. These alternative fin geometries were only applied inside the guide vanes on top of the hot spots. To goal behind examining various fin geometries was to improve the convective heat transfer in the hot spot region. This can be accomplished by efficiently increasing the heat transfer area while maintaining reasonable pressure drop levels across the heat sink. A total of three fin geometry designs were considered A, B, and C. The first two geometries both utilized wide fin shapes, placed vertically (A) and horizontally (B). The third geometry design for C utilized crossed fins with small openings at the bottom to allow the fluid to flow through. The crossed fin geometry was used to magnify the convective heat transfer by increasing the contact surface area between the fins and coolant. Fig. 12 presents the alternative fin geometry designs. The results for adopting these designs are summarized in Table 5. It is worth mentioning that the expected cost of these different designs should be similar, as they will be 3D laser printed directly on top of the chip surface.

A comparison of the results for the alternative fin geometries and the original fin geometry is provided in Table 5. Note, there was a considerable reduction in the thermal resistance value for the alternative designs. For design C, the chip temperature uniformity index decreased. For designs A and B, there was an overall enhancement in thermal performance. The pressure drop value increased for all of the alternative designs. As previously mentioned, a compromise between the thermal resistance and pressure drop should be made when considering different designs. Having a reduced thermal resistance while still maintaining an appropriate pressure drop value in the heat sink is desirable. Table 5 also demonstrates that design A has an inferior thermal performance compared with the other designs. This is attributed to its coolant flow path, since its vertical fin design directed the coolant leaving the guided vane in each hot spot region to the adjacent hot spot. Hence, the interaction of these opposing flow paths caused the temperature in the hot spots to rise. As a consequence, the thermal resistance increased.

Design C showed the best thermal performance of all the considered designs. This was due to its increased area of heat transfer, which resulted in an increase of the convective heat transfer between the fins and coolant in the hot spot regions. Since design C had the best thermal performance among all the alternative designs, it has a higher potential for performance improvement. Ac-

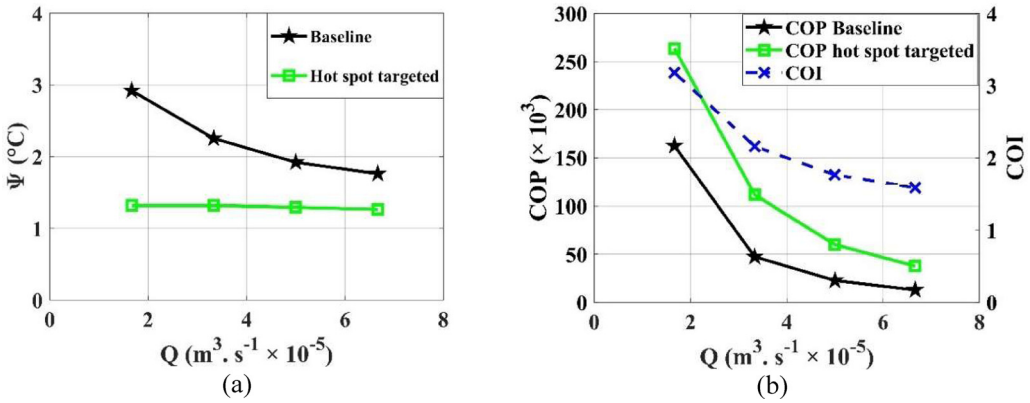


Fig. 11. (a) Chip uniformity index and (b) COP and COI variation with flow rate for the baseline design and the hot spot targeted design and the resultant coefficient of improvement.

Table 5
Calculated performance parameters for the baseline design and the alternative fins geometries designs at the hot spot region.

Flow rate ($m^3/s \times 10^{-5}$)	Design	$T_{max,\ c}$ (°C)	R_{th} (°C /W)	ψ (°C)	COI	ΔP (kPa)	COP ($\times 10^3$)
3.33	Hot spot targeted	49.4	0.047	0.93	3.04	0.8	11.5
	Design A	47.4	0.04	1.11	2.99	1.82	5.1
	Design B	46.6	0.038	0.96	3.68	1.83	5
	Design C	46	0.036	0.87	4.3	3.1	3

Table 6
Resultant response parameters from the geometrical parametric study.

Cases	$H_{f,hs}$ (mm)	$W_{f,hs}$ (mm)	$W_{ch,hs}$ (mm)	$H_{f,\ bg}$ (mm)	$W_{f,\ bg}$ (mm)	$W_{ch,bg}$ (mm)	T_{min} (°C)	$T_{max,\ c}$ (°C)	R_{th} (°C /W)	ψ (°C)	COI	ΔP (kPa)	COP ($\times 10^3$)
1 (Design C)	5	0.4	0.2	5	0.4	0.2	38.8	46	0.036	0.87	4.3	3.1	3
2	3	0.4	0.2	5	0.4	0.2	39.6	46.6	0.038	0.93	3.79	2	4.6
3	2	0.4	0.2	5	0.4	0.2	39.6	47.1	0.039	1	3.39	1.1	8.4
4	1	0.4	0.2	5	0.4	0.2	39.9	50.4	0.05	1.4	1.9	1.1	8.4
5	5	0.5	0.15	5	0.4	0.2	39.5	45.9	0.036	0.88	4.2	4	2.3
6	5	0.3	0.25	5	0.4	0.2	39.6	46.9	0.039	0.97	3.54	1.5	6.1
7	5	0.2	0.3	5	0.4	0.2	39.7	47.8	0.042	1.08	2.97	1.2	7.7
8	5	0.4	0.2	4	0.4	0.2	39.5	46	0.036	0.87	4.3	2.9	3.2
9	5	0.4	0.2	3	0.4	0.2	39.5	46	0.036	0.87	4.3	2.8	3.3
10	5	0.4	0.2	2	0.4	0.2	39.6	46	0.036	0.85	4.37	2.8	3.3
11	5	0.4	0.2	5	0.5	0.15	39.1	45.9	0.036	0.91	4.14	4.1	2.2
12	5	0.4	0.2	5	0.3	0.25	39.7	46	0.036	0.84	4.43	3	3.1
13	5	0.4	0.2	5	0.2	0.3	40.3	46.1	0.036	0.76	4.86	2.9	3.2
14	4	0.2	0.1	5	0.4	0.2	39.5	45.5	0.035	0.81	4.72	3.3	2.8
15	4	0.2	0.05	5	0.4	0.2	39.3	46.9	0.039	1.01	3.39	6.8	1.4

cordingly, it was used to carry out the optimization study in the following section.

3.3. Optimization

3.3.1. Parametric study

A multi-objective optimization study was performed to minimize the heat sink's thermal resistance and pressure drop. This was achieved by varying the geometrical parameters of fin height, fin thickness, and channel width. The following ranges were considered for the parametric study: 0–5 mm, 0.2–0.5 mm, and 0.1–0.3 mm for the fin height, fin thickness, and channel width, respectively. In this study, the background and the hot spot regions were treated separately, where different fin shapes and sizes are to be printed in each region. Table 6 shows the response parameters calculated for various heat sink geometries.

The two operational constraints that were considered in this study were maintaining the chip junction (maximum temperature) below 70 °C and having a pressure drop across the heat sink lower than 20 kPa [54]. Except for the cases when the fins were removed, either from the hot spot region, background region, or both, all of the results provided by the table are lower than the operational constraint. Hence, these constraints do not indicate any significant limitations to the optimization process.

From the table it can be observed that fin geometry in the hot spot region had the highest impact on the thermal resistance. This is expected, since the highest temperatures usually exist in hot spots due to the high heat flux in these regions. An exception to this is Case 14, where the fins were placed in the background region. Unlike the thermal resistance, the chip nonuniformity index depends on the minimum chip temperature. Accordingly, to reduce the chip nonuniformity and the impact of thermal stresses, the chip maximum temperature needs to be reduced and the chip minimum temperature needs to be increased. Thus, the table indicates that decreasing the fins size in the background region improved the chip uniformity. A robust learning algorithm coupled with optimization was required to find the global optimal solution. To that end, the objective function of the optimization study was derived from a Bayesian-based learning technique.

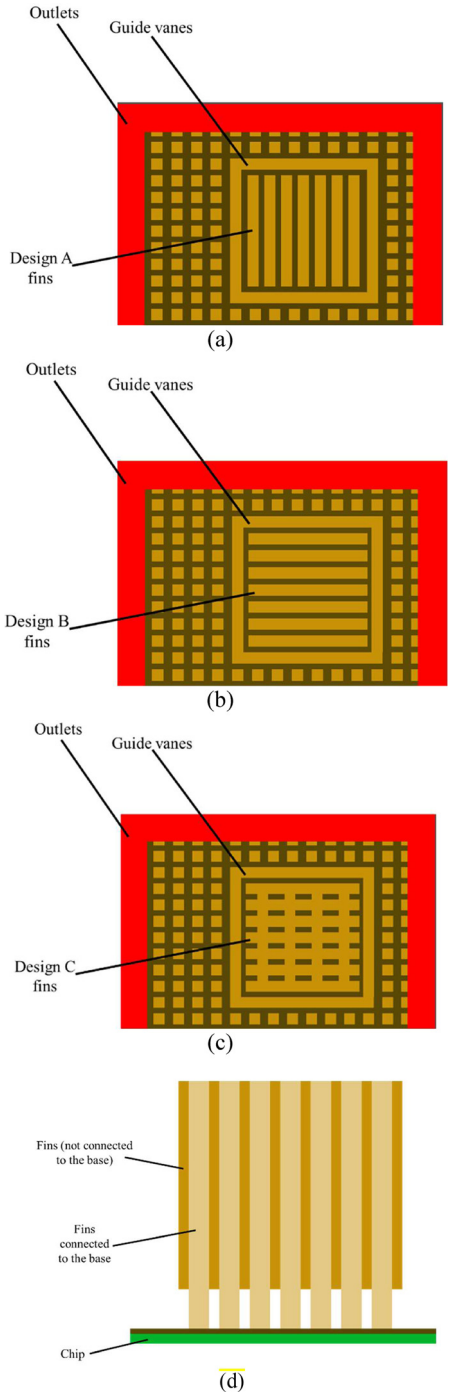


Fig. 12. Top and side view of the alternative fins geometries designs at the hot spot region (a) design A (b) design B (c) design C (d) design C side view.

3.3.2. Physics driven Bayesian regularization-based learning

The objective function for the optimization study was derived using the physics informed (supervised learning) Bayesian regularization-based learning network [55]. The objective of the Bayesian regularization method [56] is to minimize the combined error function and weight function, unlike traditional methods that only try to minimize the error function.

$$F = Min\ (\beta\ E_D + \ \alpha\ E_w) \tag{11}$$

Where E_D is the error between the data and the network output, E_w is the error of the weight function, and α and β are the regularization parameters. The Bayesian regularization-based learning network tries to determine the optimal values of the learning parameters that minimize function F. This process is termed the regularization technique. Regularization is achieved through the Levenberg-Marquardt technique by minimizing the gradient of the Hessian matrix containing the Jacobians. The architecture of the Bayesian regularization-based neural network is shown in Fig. 13.

The neural network consists of three layers: the input layer, hidden layer, and output layer. As seen from Fig. 13, the number of input neurons and output neurons are decided by the number of input and output variables, respectively. For this study, only one hidden layer was chosen. However, the number of hidden neurons in the hidden layer plays a significant role in the learning process. Furthermore, the number of hidden neurons decides the size of the weight matrix (W_{ij} and W_{jk}). A minimum number of hidden neurons is desirable for reducing the computation complexity (overfitting) and size of the weight matrix.

While testing, 70% of the data from the physics-based model was employed for training purposes. Initialization of the weights was carried out using the Nguyen-Widrow method [56]. The results from the neuron independence study are shown in Fig. 14. From the results, it is evident that the Bayesian regularization was able to achieve the best coefficient of determination (R^2) value with a number of hidden neurons equal to 3. This is an indication that the size of the weight matrix was thereby reduced, leading to more robust fitting and smoothing functions. The objective function should be devoid of non-convex regions to achieve a smooth/continuous Pareto optimal curve. This will be demonstrated in the latter part of this section.

For the analysis, a network with three hidden neurons was employed. To test robustness, a few points were chosen from the data set that were not part of training. The results of the Parity plot are shown in Fig. 15(a) and (b). The results from the Parity plot ensure that the learning network is robust, and this can be further employed for the optimization study.

3.3.3. Multi-objective optimization

The optimization problem can be stated mathematically as:

Maximize Rth = f(hotspot fin geometry, background fin geometry)

Minimize ΔP = f(hotspot fin geometry, background fin geometry)

For multi-objective optimization, the non-dominated sorting genetic algorithm-II was employed (NSGA-II) [57]. The applicability of NSGA-II to a wide variety of heat transfer problems was demonstrated by Srikanth et al. [58–60]. The primary advantage of the algorithm is the diversity in the obtained solution and closeness to the true Pareto optimal solutions. NSGA-II is a stochastic search-based optimization algorithm that requires an evaluation of the objective function in each iteration. Therefore, the algorithm requires a more robust objective function to achieve high efficiency. The NSGA-II algorithm is inspired by biological evolution and is similar to the traditional Genetic algorithm (GA). However, the preservation of elitism and diversity in the solution are two major points that distinguish NSGA-II from GA. The readers can find the methodology and the working of NSGA-II from Srikanth and Balaji [58] for solving conflicting multi-objective heat transfer problems. NSGA-II is sensitive to optimization parameters such as the probability of mutation and the probability of cross-over. A detailed sensitivity analysis was performed, and it was determined that Pc = 0.6 and Pm = 0.1 gave more robust results.

The results of the Pareto optimal solution are shown in Fig. 16. The results show that continuous and diverse solutions were obtained. Heat sink designers will be interested in different regions of the Pareto optimal curve depending on their heat transfer and hydraulic objectives. The solution to the top left (Design P1) of the

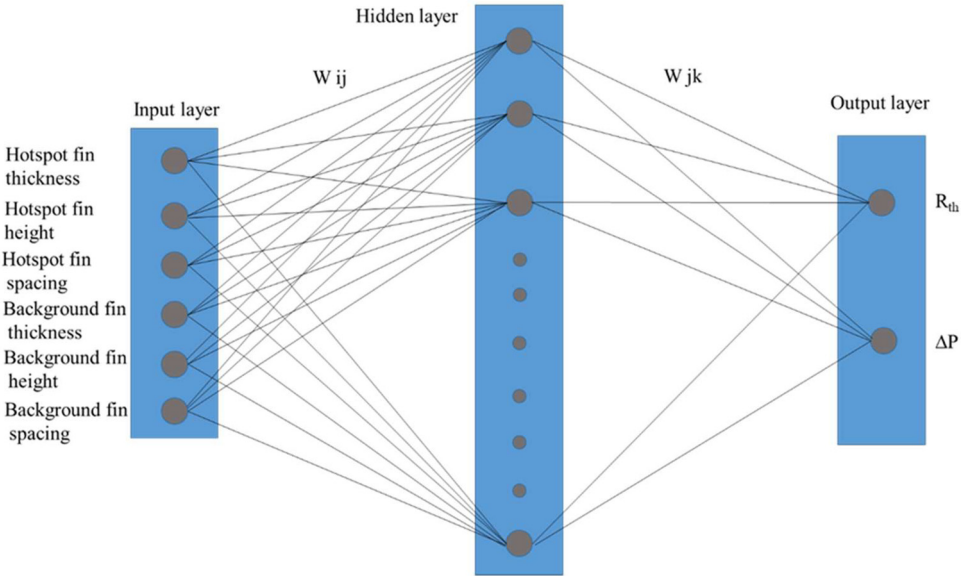


Fig. 13. Schematic of the architecture of the Bayesian regularization-based learning Artificial Neural network.

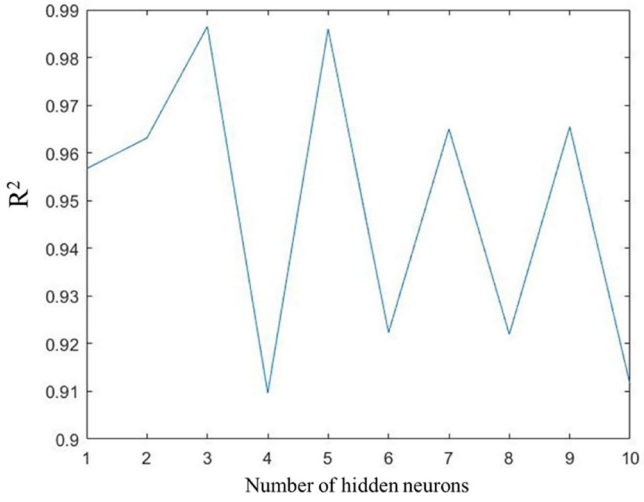
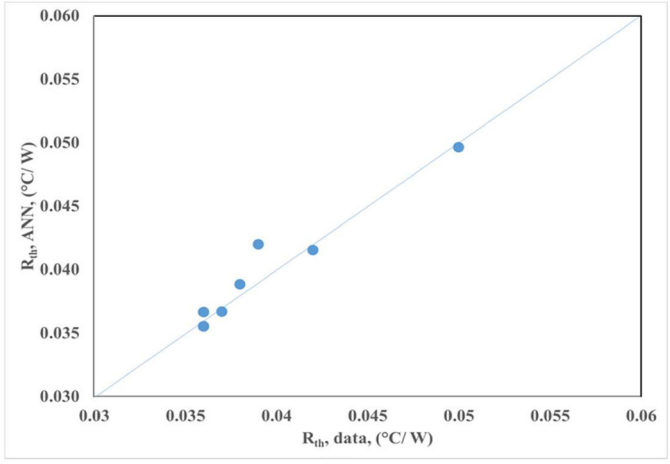


Fig. 14. Results of the neuron independence study.



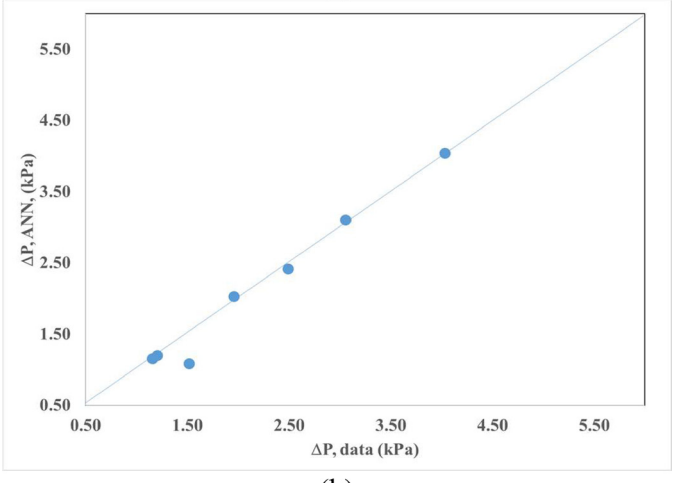


Fig. 15. Parity plot for the randomly tested data excluded from the training data set for (a) Thermal resistance (b) Pressure drop. Testing R2 = 0.99.

figure had the least pressure drop and the highest thermal resistance (or maximum temperature). It is also worth mentioning that design P1 had minor complexity with manufacturing/fabrication since there was uniform pin fin distribution throughout the chip surface. Similarly, the solution to the bottom right P4 had the least thermal resistance and maximum pressure drop. Overall, the pressure drop was well within the limits (20 kPa) prescribed in the literature. However, if both objectives are to be given equal weightage, the designer can choose the design P2. Overall, it is also seen that the background fin parameters contributed the least to the optimal performance of the heat sink. The fin design parameters corresponding to each design are marked in Fig. 16. The nomenclature for the markings can be found in the figure caption.

The most striking observation that can be made about the Pareto optimal solution is how well it aligns with the physics of the problem considered. This is an advantage of coupling a robust physics driven network with an NSGA-II algorithm. Additionally, the figure shows that from design P1 to P3 the thermal resistance decreased monotonically as the height of the fins in the hot spot increased. Consequently, the pressure drop increased mono-

Table 7
Comparison of the proposed optimized design with the literature's hot spot targeted designs.

Reference	q_{hs} (W/cm²)	q_{bg} (W/cm²)	ΔP (kPa)	R_{th} (°C.cm²/W)	ψ (°C)
Hetsroni et al. [61]	3.6	3.6	5	10.8	4.5
Rubio-Jimenez et al. [62]	100	100	20	0.25	5.7
Lee and Garimella [63]	200	100	10	0.26	11.6
Brunschwiler et al. [64]	140	40	25	0.74	7.43
Lee et al. [65]	400	85	130	0.45	6.93
	300	85	140	0.33	8.5
Ansari and Jeong [66]	100	20	-	1.36	5.2
Hadad et al. [67]	145.5	18.1	10.11	0.6	1.41
Current optimized design (P3)	150	20	2.1	0.23	0.81

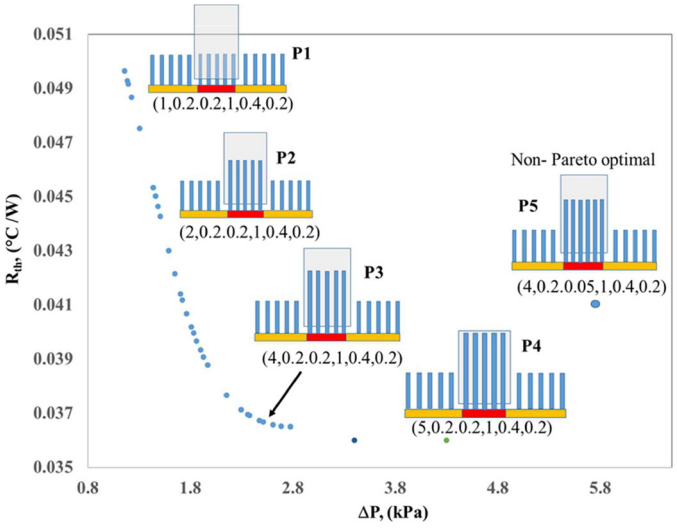


Fig. 16. Pareto optimal solutions obtained from the optimization study. The values displayed within parenthesis under each design point is in the form of (Hotspot fin height, hotspot fin thickness, hotspot fin spacing, Background fin height, Background fin thickness, Background fin spacing).

tonically. From design P2 to P3, as the height of the fins in the hot spot increased the thermal resistance decreased negligiby and the pressure drop increased. This particular result illustrates that beyond design P3 the fin height became ineffective.

The figure also shows non-Pareto optimal design P5, which had reduced fin spacing at the hot spot for the optimal fin height and thickness. This design led to an increase in both the pressure drop and thermal resistance, meaning it was not included in the non-dominated solution. From the physics driven model (from simulations), we learned that the background fin parameters (channel width and fin thickness) had a negligible effect on the thermal performance (Table 6). This is because the thermal performance is quantified using thermal resistance calculated based on the maximum temperature of the chip that always occurs at the hotspot. However, there was an effect on the hydraulic performance (pressure drop). In addition to Table 6, we ran a few other simulations to confirm this (similar to points 11, 12, 13). Henceforth, this information from the physics model becomes inherent in the training process of the Artificial Neural Network (ANN).

When the ANN is coupled with the NSGA-II the Pareto curve is identified for the best possible points concerning both thermal resistance and pressure drop. For a given thermal resistance, the best pressure drop is captured. There could be other pressure drop values for similar thermal resistance corresponding to different fin configurations in the background. However, they become a part of the non-Pareto region (dominated solutions). These solutions are no longer optimal. We have indicated one non-Pareto point in Fig. 16 (Design P5) corresponding to a different fin configuration at the hotspot. However, the non-Pareto points corresponding to different background fin configurations become less critical for the designer.

Lastly, the optimized design's (P3) performance was assessed by comparing it to proposed hot spot targeted solutions from the literature. Table 7 provides a comparison of the performance parameters from the Pareto optimized design to those of existing hot spot targeted heat sinks. The performance parameters in this table were back calculated using the available information. Also, the chip area multiplied the thermal resistance values to conduct a fair comparison between the different heat sinks. According to the table, the design proposed in this work is superior to all existing hot spot targeted designs, both in terms of its thermal performance and for having obtained the lowest pressure drop across the heat sink.

4. Conclusions

Surging chip power densities, increasing chip thermal stresses, and non-uniform heat fluxes are major challenges that restrict further development in the electronic industry. In this study, a novel hot spot targeted concept was introduced to reduce the chip temperature nonuniformity and minimize the heat sink's thermal resistance while achieving low-pressure drop values across the heat sink. First, a simple pin fin heat sink with central jet impingement was proposed as the baseline design. The thermal resistance, chip nonuniformity index, and pressure drop calculated using the numerical model were 0.059 °C/W, 2.25 °C, and 1.9 kPa, respectively. Employing the hot spot targeted concept for the same chip resulted in a 20.3%, 58.7%, and 57.9% reduction in the thermal resistance, chip non-uniformity index, and pressure drop, respectively. After that, an alternative hot spot targeted design that considered different fin geometries at the hot spot region was investigated. One of the alternatives (design C) showed a remarkable reduction in the maximum chip temperature, achieving a thermal resistance of 0.036 °C/W. A robust learning algorithm using physics-based data successfully served as the objective function for the multi-objective optimization study. The results from the learning algorithm revealed that superior learning was achieved with less complexity in the algorithm. Finally, multi-objective optimization was conducted by integrating the Bayesian regularization-based learning network with the non-dominated sorting genetic algorithm-II (NSGA-II). This optimized design compromises the thermal and hydraulic performance of the heat sink. The thermal resistance, chip non-uniformity index, and pressure drop were found to be equal to 0.23 °C- cm^2/W, 0.81 K, and 2.1 kPa, respectively. The results indicate that the optimized design is superior to all other existing hot spot targeted designs in terms of its thermal performance.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

CRediT authorship contribution statement

Yaman"Mohammad Ali" Manaserh: Conceptualization, Methodology, Writing – review & editing, Writing – original draft, Investigation, Software, Data curation, Formal analysis, Validation, Visualization. **Ahmad R. Gharaibeh:** Writing – review & editing, Writing – original draft, Software, Investigation, Data curation, Formal analysis, Validation, Visualization. **Mohammad I. Tradat:** Writing – review & editing, Writing – original draft, Software, Data curation, Formal analysis, Validation, Investigation, Visualization. **Srikanth Rangarajan:** Writing – review & editing, Writing – original draft, Visualization, Data curation, Formal analysis, Investigation. **Bahgat G. Sammakia:** Supervision, Investigation, Writing – review & editing. **Husam A. Alissa:** Supervision, Investigation, Writing – review & editing.

Acknowledgments

We would like to acknowledge Future Facilities Ltd. We would also like to thank the ES2 Partner Universities for their support and advice. This work is supported by NSF IUCRC Award No. IIP-1738793 and MRI Award No. CNS1040666.

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