

Role of Defects and Power Dissipation on Ferroelectric Memristive Switching

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Advancement of information technology requires low power, high speed, and large capacity non-volatile memory. Memristors have potential applications for not only information storage but also neuromorphic computation. Memristive devices are mostly focused on the use of binary oxides as the resistive switching materials. On the other hand, polarization assisted memristive devices based on ternary ferroelectric oxides are attracting more attention due to their unique switching properties. However, the underlying switching mechanisms and the current-voltage rotation direction are still not fully understood yet. By comparing stoichiometric BaTiO₃, BiFeO₃, and Bi_{1-x}FeO_{3- δ} ferroelectric memristors with different cation stoichiometry, it is found that off-stoichiometry-induced traps can play a critical role in controlling the ferroelectric memristive switching behavior. Ferroelectrics with slight off-stoichiometry show greatly enhanced switching properties, and the switching on/off ratio is mainly determined by the trap energy levels and concentrations. The rotation direction of current-voltage hysteresis loop is affected by the defects, which can be controlled by synthesis and power dissipation. These findings provide insight in understanding the role of defects in ferroelectric memristors and offer guidance to design ferroelectric memristors with enhanced performance.

1. Introduction

Voltage-driven modulation of the electrical resistance in a metal/metal oxide/metal (MIM) structure has attracted wide attention due to its potential impact on the developments of next generation ultrahigh density nonvolatile random access

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memory and neuromorphic computing. The simple device architecture, high resistive switching (RS) on/off ratio, low power operation, and scalability are especially attractive for the future generation memory devices.^[1-3] Different materials such as metal oxides, chalcogenides^[4-6] and carbon based materials^[7-9] have been investigated as the resistive switching layer both experimentally and theoretically.^[10] Metal oxides are found to be the very promising candidate materials for such applications. Binary oxides such as $TaO_{xy}^{[11]}$ HfO_{xy}^[12] NiO,^[13,14] TiO₂^[2,15] and Cu_vO,^[16] as well as perovskite oxides such as Cr/Fe-doped SrTiO₃,^[17,18] Co-doped BaTiO₃ (BTO),^[19] Cr-doped SrZrO₃,^[20] and Pr_{0.7}Ca_{0.3}MnO₃^[21] have been studied as the resistance switching materials. The broadly reported RS mechanisms in oxides are related to the formation of conducting filaments. In filament-type memristors, migration of defects (metal ions and/or oxygen vacancies, OVs) plays a pivotal role in the fila-

ment formation. Depending on the nature of the defects and the formation of conducting filaments, three different types of switching behaviors are generally categorized for filament-type memristors, namely the electrochemical metallization (ECM), the thermochemical memory (TCM) and the valence change memory (VCM).^[22] Figure 1 shows schematically different types of resistive switching mechanisms

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Figure 1. Schematic illustration of different types of resistive switching mechanisms observed in memristors using oxide materials as RS layers. From left to right shows filament-type and interface-type switching with different types of *I*–*V* characteristics along with the possible switching mechanisms.

observed in memristors using oxide materials as RS layers. Compared to literature defined counter figure-eight and figure eight rotation directions, Figure 1 shows two more rotation directions. Here we use current rotation direction at first Quadrant and the third Quadrant in linear I-V plot as a new way to define *I*–*V* rotation direction. The figure-eight is equivalent to counterclockwise-clockwise (CC-C) and counter-figure-eight corresponds to clockwise-counterclockwise (C-CC). In ECM, for example, the migration of metal ions from active electrodes such as Ag and Cu form the conducting filament. Figures 1a and 1g correspond to the I-V and mechanism illustration, respectively. In TCM, electroforming generates large amount of OVs due to Joule heating. The diffusion of OVs, perpendicular to the electric field (E), in and out of the filament region determines the on/off ratio of the TCM. Figures 1b and 1h are the *I–V* and mechanism illustration, respectively. In the VCM, the electroforming creates filaments in the bulk part of the film, and a redox reaction related to OV migration (drift along E field direction) modulates Schottky barrier height (SBH) and produces on and off states. It is noted that this SBH modulation often occurs locally near the filament. In other words, the VCM under such circumstances is an interface-type but confined to filament regions. Figures 1c,d and 1i are the I-V and mechanism illustration, respectively. All above mentioned filamenttype memristors often require an electroforming process.

Recent work has shown that the filament can change from cycle to cycle.^[23] The stochastic nature of the filament leads to variability of the RS behavior. Interface-type non-filamentary memristors, on the other hand, are often electroforming-free. They offer the advantage of superior stability, non-linear current with self-rectification characteristics, and area scalability.^[24,25] Interface-type switching is related to the physical or chemical

phenomena occurring at the oxide/electrode interface. The most observable feature of such a switching process is the scaling of the device resistance with the electrode area. In the case of interface-type RS devices, three switching mechanisms are often considered: i) electronic and/or electrostatic effect, ii) polarization-induced barrier modification, and iii) change of valence state of cations resulting from OV migration. The most common RS processes related to electronic and electrostatic mechanisms are charge (electrons) trapping/ detrapping^[26] and tunneling at the interface.^[27] The dynamics of space-charges resulted from trapping/detrapping of carriers can modulate SBH and lead to a hysteresis current versus voltage (*I–V*) characteristic, as observed in Pt/Nb:SrTiO₃/Pt structure.^[27]

Ferroelectric materials, which also give rise to interfacetype switching, have been explored for potential applications in ReRAM in two ways: a) ferroelectric diodes (FeDs), where the spontaneous polarization can be switched by applying an E field of opposite polarity and such a polarization switching can modulate the SBH^[28] and therefore the conduction, and b) ferroelectric tunnel junction, where the tunnel junction barrier can be modified.^[29] The I-V and switching mechanisms for FeDs are shown in Figures 1e,f and 1l. In addition to polarization, it is also possible that the OV drift occurs under the whole area of the contact electrode in these insulating oxides based MIM and Figure 1j shows the illustrated mechanism. Different from the polarization mechanisms (electronic effect), OV drift is an ionic effect. Such two effects can produce similar I-V curves with counterclockwise-counterclockwise (CC-CC) rotation direction (Figure 1e) as reported in defect engineered BFO and porous silicon films.^[30] However, the ionic and electronic nature of these two effects can be distinguished by time response of the reading/writing steps.[31] Regardless of the



switching mechanisms, FeDs can be used as the building block for memristors. Different switching mechanisms have been classified broadly and are schematically shown in Figure 1.

The role of defects in filament type resistive switching is widely investigated but it is less clear for interface-type FeDbased memristors.^[32,33] For example, the interplay between defects and polarization and their effect on current injection as well as RS behavior has not been fully understood yet. Therefore, it is imperative to systematically investigate the coupling between defects and polarization on RS phenomena in FeD-based memristors. In addition, as shown in Figure 1, filament-type and interface-type memristors can exhibit different type of I-V curves with distinct rotation direction of hysteresis loops. The investigation of the correlation between these two types could shine light on the reported puzzle about the rotation direction of I-V hysteresis loops.^[34] In this work, we have systematically investigated the switching properties of BaTiO₃ (BTO), BiFeO₃ (BFO) and $Bi_{1-x}FeO_{3-\delta}$ thin film-based memristors. Our results indicate that not only the polarization but also the cation off-stoichiometry-induced defects play critical roles in determining the I-V switching mechanisms such as the rotation direction of the I-V hysteresis loops and switching properties. For instance, the on/off ratio is correlated with the trap concentration and energy level. In addition, the interface-type memristors based on FeDs can be irreversibly switched into filament-type memristors by increasing the power dissipation, where the rotation direction of I-V hysteresis loops is also altered. It is noted that we have used BTO and BiFeO₃ (BFO) as the model systems since such materials are ferroelectric and have been intensively studied due to their potential device applications. The principles discovered here are applicable to other (non)ferroelectric materials.

2. Experimental Section

Pulsed laser deposition (PLD, KrF excimer laser, $\lambda = 248$ nm) was employed to grow both BFO and BTO films on SrRuO3 (SRO) buffered SrTiO₃ (STO) (001) substrates. Four BFO targets with different Bi/Fe ratios were used to deposit BFO films with different Bi/Fe ratios (or different defect concentrations). Four BFO targets were made by sintering Bi₂O₃ and Fe₂O₃ powder. The Bi/Fe molar ratio in the raw materials are 0.95:1, 1.0:1.0, 1.05:1.0, and 1.1:1.0, respectively. These four targets were named as Bi0.95FeO3, Bi1.0FeO3, Bi1.05FeO3, Bi1.1FeO3 and the films grown by these four targets were defined as BFO (0.95), BFO (1.00), BFO (1.05), and BFO (1.10), respectively. The substrate temperature was initially optimized and maintained at 680 °C for both SRO and BFO deposition. SRO bottom electrodes (≈18 nm) were deposited under 100 mTorr oxygen and 2 Hz laser repetition rate. BFO films with a thickness of ≈150 nm were grown under 10 Hz and an oxygen pressure of 20 mTorr. After deposition, the BFO/SRO/STO stacks were in situ annealed at 400 °C and one atm. oxygen for one hour before cooling down to room temperature at a cooling rate of 5 °C min⁻¹. For the growth of BTO/SRO/STO (001) heterostructures, the detailed experimental conditions have been reported elsewhere.^[35] Briefly, an optimized substrate temperature of 700 °C was employed for the growth of both SRO and BTO layers. After deposition, the stack was in situ annealed in



pure oxygen environment (1atm) at 600 °C for one hour before cooling down to room temperature at a rate of 5 °C min⁻¹. Circular Au (~100 nm thick) top electrodes with a diameter of 350 µm defined by a shadow mask were deposited by magnetron sputtering at room temperature. One BFO/Nb:STO film synthesized by the sol-gel method was purchased from MTI to compare with BFO/SRO/STO and BTO/SRO/STO. The Bi/Fe ratio of the BFO films made by such a solution method was determined to be 1.17. This sample is defined as s-BFO. The ferroelectric hysteresis loop of the devices was tested by a TF Analyzer 1000 at 1 kHz. An Agilent E4980A precision LCR meter was used to measure electrical field (*E*)/Voltage (*V*) dependent capacitance (*C*), dielectric loss (tan ϑ), and current (*I*) of the devices. The current is defined as positive when the positive bias voltage is applied on the top Au electrode.

3. Results and Discussion

Electrical properties of Au/(BFO or BTO)/SRO and sol-gel made BFO/Nb:STO (s-BFO) were fully investigated by measuring both the ferroelectric/dielectric and the I-V characteristics of the devices. Figure 2 shows the typical *P*–*E*, capacitance C-E, tan δ -E, and I-E of three devices with BTO, s-BFO, and BFO (1.05), as the switching layers, respectively. As can be seen from Figure 2a-c, the polarization of BTO layer saturated at 27 μ C cm⁻² with increasing bias field, indicating a typical ferroelectric behavior (Figure 2a). A saturation polarization of \approx 70 µC cm⁻² and a coercive field of \approx 200 kV cm⁻¹ (Figure 2b) were measured for the s-BFO film, which is similar to values reported in the literature,^[36,37] indicating that the BFO film exhibits normal ferroelectric behavior. For BFO (1.05), the polarization and coercive fields keep increasing with applied bias field without saturation, indicating deviation from the normal ferroelectric behavior (Figure 2c). The polarization value at maximum *E* field is much lower than that reported in literature.^[38,39] The round shape of *P*–*E* loop at maximum field indicates that the leakage current makes a significant contribution to the measured results.

In the BFO (1.05) films, defects such as Bi vacancy and oxygen vacancy and a mixed valence of Fe ion likely contribute to the high leakage current and the deviation from normal ferroelectric behaviors.^[40-42] The chemical formula of BFO (1.05) should be $Bi_{1-x}FeO_{3-\delta}$ while that of s-BFO is $Bi_{1.17}FeO_{3+\nu}$. The *C*–*E*, dielectric tan δ –*E*, and *I*–*E* behaviors of these devices are shown in Figure 2d–i. The C–E and tan δ –E curves of BTO (Figures 2d and 2g) and s-BFO (Figures 2e and 2h) samples show a typical ferroelectric behavior. The BFO (1.05) sample also shows a butterfly-like shape in C-E loops. However, the capacitance tunability, defined as $(C_0 - C_\nu)/C_0$, is much smaller for BFO (1.05) since charges leak through the film (Figures 2f and 2i), where C_0 and C_{ν} are the capacitance at zero bias and a given bias, respectively. The tan δ -*E* plots show that the dielectric loss increases significantly with bias voltage, confirming the existence of large leakage in BFO (1.05) (Figure 2i). It should be noted that *P*–*E* loops in our experiment have been measured by a voltage-ramp technique (≈1 ms per data point). To reveal DC leakage currents, a voltage-step technique with longer charging and discharging time was used (≈250 ms per data point).^[43] The







Figure 2. Electrical properties of a-c) *P*–*E* loops; d–f) *C*–*E*; g–i) tan δ –*E*; and j–l) *I*–*E* for BTO, s-BFO, and Bi_{1-x}FeO_{3- δ} thin films. The *P*–*E* loop in (a) is reproduced with permission.^[35] Copyright 2013, American Institute of Physics.

I-E loops, shown in Figure 2j–l, were measured at longer time scales for BTO, s-BFO, and BFO (1.05) films, respectively. In the BTO and s-BFO films, the current-bump at location 1 and 3 is due to the polarization current as the leakage current is low. On the other hand, we do not see the polarization current-bump in the BFO (1.05) film, because the leakage current dominates the overall I-E characteristics.

It is interesting that the rotation direction of *I*–*E* hysteresis loops changes from clockwise–clockwise (C–C) in BTO and BFO to counterclockwise–counterclockwise (CC–CC) in Bi_{1-x}FeO_{3- δ} (see Figure S1, Supporting Information). In addition, the overall leakage current follows $I_{BTO} < I_{BFO} < I_{Bi1-xFeO3-\delta}$. The C–C type RS has been often seen in memristors where ferroelectric materials such as (Pb,Zr)TiO₃,^[44] BTO, and BFO (≤213 K)^[45] are used as the RS layer. The current-bump in the C–C type hysteresis is due to the transient displacement current from polarization switching. This feature is frequency dependent.^[46] Therefore, the CC–CC type *I*–*V* hysteresis in ${\rm Bi}_{1-x}{\rm FeO}_{3-\delta}$ (defect-engineered BFO) should have a different physical origin.

To investigate the role of defects on the I-V hysteresis loop with a CC–CC type rotation direction, devices using BFO RS layers deposited from BFO targets with different Bi compositions were studied. As BFO (0.90) is highly defective, it acts as a pure resistor. Devices fabricated using higher Bi compositions are less defective with less Bi vacancies and hence are resistive enough to enable polarization measurements (Figure S2, Supporting Information). We note that Bi vacancies introduce deep levels in the bandgap of the material, and such deep level traps influence the overall transport properties of the devices, depending on the energy level and concentration of the traps.

The *I*–*V* curves of these ferroelectric memristors are shown in **Figure 3**a. It can be seen that all these samples have the CC–CC type *I*–*V* characteristics. The switching mechanism, band structure and *I*–*V* curve fitting have been previously reported.^[47] It







Figure 3. a) *I–V* characteristics of three different Au/BFO/SRO devices with different Bi concentration. b) The Log (*I*) versus Log (*V*) of Au/BFO/SRO devices, where m = 2 in the ramp-down region indicates that traps are all filled. Slope in the TFL region is equal to 6, 17, 8 in the TFL regime, respectively, for BFO (1.00), BFO (1.05), and BFO (1.10) samples.

was reported that the I-V curves can be fitted into three segments on the positive bias. The first segment is polarization modulated Schottky barrier conduction, which corresponds to the high resistance state (HRS). After the Schottky interface becomes a non-blocking interface because of the induced polarization, the current is then controlled by space charge limited conduction (SCLC) of deep-level trap filling. At the second segment, the current can be described by $I \approx V^m$ (m > 2). During the voltage ramp-down (corresponding to low resistance state, LRS), the polarization coupled SCLC current is given by $I \approx V^n$ $(m > n \ge 2)$.^[47] A large opening of the hysteresis is observed for the voltage ramp-up and -down due to different current transport mechanisms. The on/off ratio, strongly depending on the Bi concentration, increases from ≈ 10 in the BFO (1.00) sample to $\approx 10^3$ in the BFO (1.05) sample, then drops to $\approx 10^2$ in the BFO (1.10) sample (Figure 3a). The I-V curves of all samples are analyzed, according to the conduction mechanism discussed in ref. [47] as shown in Figure 3b. They exhibit similar slopes $(n \approx 2)$ during the voltage ramp-down. It indicates that the deep traps are screened by polarization charges. The trap filling limit (TFL) region can be linearly fitted. The slopes for BFO (1.00), BFO (1.05), and BFO (1.10) are 6, 17, and 8, respectively. If we define the on/off ratio, r, as the ratio of the currents in the thermally activated region versus the trap-free region, then, this ratio can be calculated from.^[48]

$$r = e^{E_t/k_{\rm B}T} \tag{1}$$

where E_t is the energy difference between the conduction band bottom and the trap energy level, *T* is the temperature, and k_B is the Boltzmann constant. Therefore, the on/off ratio of a ferroelectric memristor is controlled by the trap energy level. A deeper energy level often indicates a larger on/off ratio.

Figure S3, Supporting Information shows the RBS results of BFO (1.0) film. The Bi/Fe ratio of 0.91 indicates Bi vacancies could be the source of traps. We speculate the following scenario to explain on/off ratio in these BFO samples. A BFO (1.0) sample exhibits a small on/off ratio (\approx 10) due to the existence of a larger amount of shallow level Bi vacancies, that is, smaller E_t . The shallow traps contribute to thermally activated free carriers, which is consistent with the smaller resistance at HRS (green curve). A slightly increasing Bi content will increase E_t . Therefore, the BFO (1.05) sample shows a larger on/off ratio (\approx 10³). A further increase in Bi content,

Table 1. Physical parameters for traps and dopants in different BFO memristors, where a single discrete energy level is assumed for the deep-level traps. The trap energy level is referenced from the conduction band.

Target for PLD growth	BFO (1.00)	BFO (1.05)	BFO (1.10)
Slope (m)	6	17	8
V _{TFL1} (V)	2.56	2.67	1.35
V _{TFL2} (V)	3.96	4.06	3.06
N _t (cm ⁻³)	1.93×10^{18}	1.98×10^{18}	1.49×10^{18}
N _d (cm ⁻³)	6.84×10^{17}	6.8×10^{17}	8.36×10^{17}
N _{eff} (cm ⁻³)	1.25×10^{18}	1.30×10^{18}	0.65×10^{18}
Trap energy level <i>E</i> t (eV)	0.07	0.2	0.17
RS on/off ratio at 0.9V	≈10 ¹	≈10 ³	≈10 ²

as shown in the BFO (1.10) sample, the decrease of the on/ off ratio could be due to the decrease of deep-level traps concentration. Therefore, to achieve a large on/off ratio in ferroelectric memristors, it is important to achieve an optimized concentration of deep-level traps (and limit shallow traps). Therefore, tuning cation-related deep level traps and energy levels, whether these traps be cation vacancies, as in this work, or cation substitution in others (e.g., Sm and Ni codoped BFO polycrystalline films give on/off ratios of $\approx 10^4$),^[49] is a feasible approach to achieving high performance ferroelectric memristors.

It is interesting to estimate the trap energy level and concentrations in BFO films. Zhang et al. pointed out that the interplay between dopants and traps can be the dominating factor for the slant of the vertical current rise in an insulator with a single and discrete trap level.^[48] The deep level traps density can be described as $N_t = 2\varepsilon_0 \varepsilon_{st} \frac{V_{\text{TFL2}}}{el^2}$, where *l* is the film thickness, ε_0 is the permittivity of vacuum, ε_{st} is the static low frequency dielectric constant, and $V_{\rm TFL2}$ can be obtained from Figure 3a. The dopant density, $N_d^+ = 2\varepsilon_0\varepsilon_{st} \frac{V_{\text{TFL2}} - V_{\text{TFL1}}}{el^2}$, and the V_{TFL1} can be obtained from Figure 3a. Table 1 summarizes the key parameters based on above discussion, where N_{eff} is defined as $N_{eff} = N_t - N_d^+$. The calculated parameters are consistent with the on/off ratio discussed above. For example, the E_t of a BFO (1.00) memristor is 0.07 eV, while the value is as large as 0.2 eV for BFO (1.05). Although BFO (1.05) and BFO (1.10) have similar trap energy levels, the N_{eff} of BFO (1.05) is twice of that in BFO (1.10). It is worth to mention that trap energy states in the material can be measured by photothermal deflection spectroscopy^[50,51] and deep-level transient spectroscopy.^[52]

Above discussion outlines that the rotation direction of I-V hysteresis loops and current switching levels of defect-engineered BFO film are much different from normal FeDs-based memristors. Now, let's study the I-V hysteresis loops in BTO films. In the case of wide-bandgap BTO films with limited traps, the I-V characteristic is quite different. The I-V of an Au/BTO/SRO device shown in **Figure 4**a can be fitted with Equation (2) which describes the current through the reverse biased Schottky contact^[53] with built-in field far less than applied field *V*,







Figure 4. Resistive Switching of Au/BTO/SRO devices. a) The Log (*I*) versus $V^{1/4}$ of Au/BTO/SRO. b) The Log (*I*) versus Log (V) curves cycled for 200×. c) The reading of pulse measurements. The solid circles represent the reading pulses at +1 V after +6 and -6 V writing pulses.

$$I = A^* A T^2 \exp\left(-\beta \left(\phi_b - \sqrt{\frac{q}{4\pi\varepsilon_0\varepsilon_{st}}} \sqrt[4]{\frac{2qN_{eff}}{\varepsilon_0\varepsilon_{st}}} V\right)\right) \left(1 - e^{-\beta V}\right)$$
(2)

where *q* is electron charge, $\beta = q/kT$, *T* is the temperature, *A* is the area, ϕ_b is built in potential, ϵ_0 and ϵ_{st} are the dielectric permittivity of vacuum and the medium respectively, N_{eff} is the effective charge density and A^* is the Richardson's constant. The *I*–*V* can be clearly described by $\ln(I) \approx \sqrt[4]{V}$. It is also found that stoichiometric BFO can be fitted by Equation (2), as shown in Figure S1, Supporting Information.

These results indicate that the I-V characteristics of stoichiometric BFO and BTO are governed by the interfacial effect. Figure 4b shows I-V hysteresis loops of BTO films cycled 200×. It shows that the BTO based device exhibits the C–C type resistive switching (Figure S1, Supporting Information). It can be also seen that the loops are overlapped, indicating good retention. The on/off ratio is \approx 50 at -0.5 and 1.0 V. It should be noted that the operation current in the C–C type is in the nA range, while that of CC–CC device is in the μ A range with the same electrode size (Figure S1, Supporting Information).

The pulse measurement of BTO memristors is shown in Figure 4c. A –6 V is applied to set the device to LRS. The reading pulses (+1 V, red) read out a positive current, consistent with Figure S1b, Supporting Information. On the other hand, when a +6 V is applied to reset the device to the HRS, then the reading pulses (+1 V, blue) read out a negative current. This is related to the depolarization field. Another interesting feature is that there is a strong decay of the reading current/resistance, as shown in Figure 4c. This might be due to the non-linear decay in the depolarization field when the voltage drops from ± 6 to 1 V.

Defect-engineered BFO (1.05) FeDs based memristors show completely different characteristics in pulsed measurements. Figure 5a shows the pulse measurements at a reading voltage of



Figure 5. Pulse measurements of Au/BFO (1.05)/SRO devices. a) Pulse reading at a reading voltage of 0.9 V. b) Zoom in of pulse measurements in (a). c) The writing and reading for pulse measurements. The solid squares represent the writing pulses and the solid circles represent the reading pulses. d,e) The pulsed measurements at a reading voltage of 2 and 2.5 V, respectively.





Figure 6. a) *I*–*V* characteristic in log scale of Au/BTO/SRO device before and after electroforming by applying 20 V bias and b) the linear plot of the *I*–*V* curve after electroforming. c) *I*–*V* curves in log scale of Au/BFO (1.05)/SRO device before and after electroforming and d) the linear plots of the *I*–*V* curves.

0.9 V (well below the BFO coercive field), confirming the high on/off ratio of $\approx 10^3$, which is consistent with the *I*–V hysteresis loop (Figure 3a). Figure 5b shows details of the reading at 0.9 V from Figure 5a. The reading stabilizes after 4-5 reading pulses, which may be related with the filling of traps. One significant difference is that the on/off ratio in reading (below coercive field) is quite stable in defect-engineered BFO. Figure 5c shows the pulse measurement configuration. A +4.5 V writing pulse is applied on Au/BFO to SET the device into LRS. Reading pulses (e.g., +0.9 V, +2 V) are applied to read out the states. A -5 V writing pulse is then applied to RESET the device into HRS, followed by subsequent reading pulses. The HRS reading at 2 and 2.5 V displays an obvious aging effect while LRS reading is constant (Figures 5d and 5e). After a -5 V RESET, a reading voltage of 2-2.5 V, close to the coercive field, affects the RESET status by changing the ferroelectric domains and thus aging is observed. The reading of LRS is quite stable. This is because LRS is controlled by polarization coupled SCLC.

The above results have demonstrated that the characteristics of FeDs-based interface-type bipolar RS (BRS) memristors can show both CC-CC and C-C I-V hysteresis loops. The coupling between polarization and deep traps is the underlying mechanism for the CC-CC type rotation direction in defectengineered FeDs. However, the connection between the interface-type and filament-type switching, as shown in Figure 1, is largely unknown. Next, we will demonstrate that the power dissipation on the devices can be used to manipulate defects and alter switching behavior by applying a large forming voltage. Figure 6a shows the I-V curves of the Au/BTO/SRO device before and after electroforming. We observe that the switching current increases two orders of magnitude. Figure 6b shows 200 hysteresis loops in linear scale with the CC-C rotation direction after electroforming. It shows excellent repeatability. The dielectric loss, C-V and polarization of Au/BTO/SRO sample before and after electroforming are shown in Figure S4, Supporting Information. The dielectric loss of the BTO film increases more



than two orders of magnitude after electroforming, consistent with the increase of leakage current from the filament. P-Eloops after electroforming have a banana shape and the C-Vcurves are also altered. These results indicate that an appropriate forming voltage can generate structural defects which can irreversibly make the highly resistive ferroelectric BTO into a leaky dielectric and can modulate the switching characteristics. During the forming process, a large bias of +20 V is applied on the top interface. The forward condition means most of the bias will be applied on the BTO film, which causes a breakdown. It is commonly believed that such a high forming voltage will generate a large amount of OVs and result in filament formation in the BTO film. This process corresponds to the VCM mechanism and the illustrations are shown in Figures 1d,j. This process should be similar to forming process reported in non-ferroelectric oxides.^[58-60] Once forming is finished, ferroelectric polarization will have limited contribution to the I-V characteristic due to the conducting filament formation. Since the LRS and HRS after electroforming show strong nonlinearity, the interface still plays an important role in the switching process. For VCM mechanism, it is often believed that the filament is not fully penetrated through the Schottky interface, where the working Schottky interface still results in the nonlinearity in *I*–V.

Figure 6c shows a typical I-V curve of a BFO (1.05) memristor before and after electroforming. It is very clear that the rotation direction of the I-V hysteresis loop changes from $1 \rightarrow 2 \rightarrow 3 \rightarrow 4$ (CC-CC) to $1 \rightarrow 2' \rightarrow 3' \rightarrow 4$ (CC-C). The linear plot of Figure 6c is shown in Figure 6d, which shows the change of rotation direction of I-V hysteresis loop after electroforming. A counterclockwise I-V curve with m = 1 by sweeping voltage from 4 to -4 V suggests the formation of conducting filaments in the BFO layer (the resistance of devices are around ≈10 k Ω after forming filaments as shown in Figure S5, Supporting Information). Therefore, high power dissipation such as an electroforming process switches the BRS behavior from CC-CC and C-C type to CC-C. Since the LRS after electroforming shows a linear characteristic, this indicates that the switching is controlled by filaments, not the Schottky interface. The filaments likely penetrate through the top/bottom interfaces. Different from the VCM mechanism in formed BTO films, the BFO films show TCM mechanism (Figures 1b,h) after forming.

Figure 7 summarizes that the rotation direction of *I*–*V* hysteresis loops (of the types shown in Figure 1) and switching current can be controlled by defect engineering and power dissipation. Such defect engineering can be achieved via changing stoichiometry during growth (to influence the concentration of deep traps, in our case cation vacancies) and/or by formation of a filament via an electroforming process. Interface-type FeDs-based memristors using near-stoichiometric BTO and s-BFO (Bi excess) as the switching layer often show low switching current (nA range) with C–C type *I*–*V* hysteresis loop (green curve of Figure 7). There are at least three scenarios which can modify the *I*–*V* characteristics:

a) The first one is related to defects such as vacancies generated during synthesis. When the Bi vacancies are introduced during growth, a C–C type *I–V* hysteresis loop (green curve of Figure 7) can be switched to a CC–CC type (blue curve of Figure 7) with slightly increased switching current (μA range). This is consistent with previous results.^[46] These





Figure 7. Transformation among different switching types by changing defects and power dissipation. The interface-type with C–C and CC–CC *I–V* hysteresis loop can be transformed into filament-type switching with CC–C or C–CC *I–V* hysteresis loop by controlling the power dissipation. The C–C *I–V* hysteresis loop can be also transformed into CC–CC type by controlling defects during synthesis and temperature can make reversible change between CC–CC and C–C.

two types of I-V hysteresis loops correspond to BRS with nonlinear I-V at both HRS/LRS with extremely low power dissipation, as shown in Figure 1. *I*–*V* hysteresis loops of both systems are controlled by interface. Interestingly, some of devices can have CC-C type rotation direction by combining C-C and CC-CC together. For example, Lee et al. reported CC-CC type *I*-V hysteresis loop in BFO films grown by a stoichiometric BFO target while CC-C type I-V hysteresis loop in BFO films grown by a 10% Bi excess BFO target.^[61] This is consistent with another report.^[46] It is critical to mention that the underlying mechanisms governing the CC-C type *I*–*V* in insulating BFO films grown by Bi excess target are completely different from filament controlled CC-C type *I*–*V* in relative leaky samples. The switching current in such "C" rotation *I*–V curves (Quadrant 3) is orders of magnitude lower than that in filament dominated I-V curves. This is because that I-V curves for above BFO films are controlled by bulk ferroelectric and polarization modulated Schottky interface. The current magnitude or current density is a key parameter to distinguish them. It should be noted that some reported BFO films also show filament dominated CC-C type I-V.^[62] In this case, the ferroelectricity is not a dominating mechanism and BFO can be treated as a regular semiconducting oxide.

- b) The second parameter is temperature. For example, changing temperature can switch the *I*–*V* hysteresis loop between C–C type and CC–CC type in BFO films.^[45] This is because at higher temperatures some defects are thermally activated and interface states and traps become active.
- c) When filaments are introduced by increasing the power dissipation during the measurement, the C–C type *I*–V hysteresis loop can be switched into a filament-type BRS with a CC–C type hysteresis loop (red curve of Figure 7) and mA switching current. In addition, by increasing the power dissipation,



interface-type FeDs-based memristors using a defect-engineered BFO layer as the switching layer can also be transferred into filament-type BRS with CC–C type hysteresis loop and mA switching current. These results indicate that both interface-type switching with both C–C type and CC–CC type *I*–*V* hysteresis loops can be irreversibly switched to filamenttype BRS with CC–C type *I*–*V* hysteresis loops.

I-V curves with CC-CC rotation direction can be observed in FeDs via an electronic effect. Ideally, such I-V curves with CC-CC rotation direction should also exist in non-ferroelectric systems via an ionic effect.^[30] However, they have a completely different time response. We argue that such CC-CC I-V hysteresis loops can be achieved by polarization (via an electronic effect, see Figure 1l) and/or charged species (positively charged OV via an ionic effect, see Figure 1j) and deep traps. Such I-V loops are controlled by interface and bulk conduction and should be area dependent. Applying a large field or engineering more defects will convert this into a filament type switching in general. Therefore, the change of I-V characteristics in Figure 7 is a general mechanism which is also suitable for non-ferroelectric materials. Overall, our experimental results clearly indicate that it is plausible to manipulate the defects in the RS layer during the growth process as well as post-growth to control the conduction mechanism and I-V characteristics of ferroelectric memristors.

4. Conclusion

Using ferroelectric oxides as the resistive switching materials, we have investigated the role of defects and power dissipation on the RS properties in FeDs-based memristors. BTO systems with negligible traps as the RS layers exhibit *I*–*V* characteristics with the C-C I-V hysteresis loop as expected for FeDs. BFO systems with deep traps exhibit greatly enhanced RS properties, where the on/off ratio is related to trap energy level and concentration. Such defect engineered BFO FeDs show CC-CC type *I–V* hysteresis loop. By controlling the power dissipation during forming process, interface-type switching in FeDs-based memristors can be switched to filament-type RS with changes in both switching current and rotation direction of I-V hysteresis loop. Our experimental results clearly indicate that defect control during synthesis and post-synthesis via forming play important roles in determining the switching mechanisms and I-V hysteresis loops. These findings provide insight for understanding RS in ferroelectric memristors and demonstrate unique approaches for controling *I–V* hysteresis loops in memristors.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

defects, electrical properties, ferroelectric memristors, resistive switching, thin films

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