Changes in Band Offsets of NiO/β-GaN With Annealing Temperature

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ABSTRACT

The band alignment of sputtered NiO on c-plane GaN was measured by X-ray Photoelectron Spectroscopy for post-deposition annealing temperatures up to 600°C. The band alignment is type II, staggered gap in all cases, with the magnitude of the conduction and valence band offsets increasing monotonically with annealing temperature. For the as-deposited heterojunction, ΔE_V=-0.9 eV and ΔE_C= 0.2 eV, while after 600°C annealing the corresponding values are ΔE_V=-3.0 eV and ΔE_C= 2.12 eV. The bandgap of the NiO was reduced from 3.90 eV as-deposited to 3.72 eV after 600°C annealing, which accounts for most of the absolute change in ΔE_V-ΔE_C. Differences in thermal budget may be at least partially responsible for the large spread in band offsets reported in the literature for this heterojunction. Other reasons could include interfacial disorder and contamination. Differential charging, which could shift peaks by different amounts and could potentially be a large source of error, was not observed in our samples.

Keywords: Ga_2O_3, band offsets, heterojunctions, wide bandgap semiconductor

1. Introduction

There is considerable interest in developing Ga_2O_3 power electronics because of the lower resistive losses and higher energy conversion efficiency relative to Si power device switching [1-10]. Critical breakdown fields in lateral β-Ga_2O_3 transistors larger than the theoretical limits of SiC and GaN have been achieved [5]. There is particular interest in vertical Ga_2O_3 devices because of their larger conducting areas [11-30] and recently breakdown voltages of ~6kV have been reported for β-Ga_2O_3 vertical rectifiers with edge termination consisting of a deep trench of SiO_2 [31]. For these unipolar devices, a number of variants have emerged. FinFETs require that the surface potential in the channel region be tunable to enable accumulation and depletion, whereas planar rectifiers require that the surface region be depleted to avoid surface-related breakdown [2,4,7,9,17,21]. Additionally, the latter benefit from narrow trenches and wide mesas/fins in order to achieve high device current density, whereas FinFETs need narrow fins to obtain enhancement mode (normally-off) behavior. These create entirely different requirements on the dielectric-semiconductor interface and the geometry of the fins [2,3].

To overcome the absence of conventional p-type dopants for β-Ga_2O_3 and access the advantages of p-n junction devices, including higher breakdown voltage and flexibility in designing junction termination extension and p-type guard rings, a variety of p-type oxides have been integrated with n-type Ga_2O_3. These include SnO_2, Cu_2O, CuI and NiO for vertical p–n heterojunction power diodes [13-37]. These typically show smaller leakage current than conventional planar rectifiers and also have larger turn-on voltages [20-25]. The minority carrier nature of these devices should allow lower on-resistances and better on-state performance. In particular the focus has been on use of sputtered NiO [16, 19-28]. The highest reported breakdown voltages for these heterojunctions are a static V_B of 2.41 kV [32], with specific on-resistance of

1.12 mΩ.cm^2, producing a Baliga's figure of merit (FOM) of 5.18 GW.cm^2 [25]. Large area devices (1 × 1 mm ^{2}) exhibited a forward current of 5A and breakdown voltage 700 V (FOM 64 MW/cm^2) [28] and a 9-mm^2 heterojunction rectifier, a surge current of 45 A was recorded in a 10-ms surge transient [21].

A point of contention in the literature has been the large spread in values reported for band offsets of NiO on Ga_2O_3. Gong et al. [23] reported a staggered type II alignment with a valence band offset of -3.74 eV and a conduction band offset of 2.54 eV, determined from a combination of Ni2p$_{3/2}$, Ga2p$^{3/2}$ and O 1s and valence band maxima. Ghosh et al.[37] reported a staggered type II alignment, with ΔE_V=-1.6 eV and ΔE_C= 0.3 eV. By contrast, Lu et al. [16] reported a type II alignment with ΔE_V=-2.3 eV and ΔE_C= 1.2 eV, while Zhang et al. [29] reported ΔE_V=-2.1 eV and ΔE_C= 0.9 eV. While it not unusual to see significant differences in valence band offsets for nominally similar deposition conditions in the same heterostructure, the spread in values for NiO/Ga_2O_3 needs further evaluation. It has been established previously in other dielectric/ semiconductor systems that the biggest contributor to variability in reported conduction band offsets is the uncertainty in band gap of the dielectrics due to differences in measurement protocols and stoichiometry resulting from different deposition methods, chemistry and contamination [38,39]. In terms of variations in valence band offset values, factors such as strain, defects/vacancies, stoichiometry, chemical bonding and interfacial contamination may play a role [39]. One other possible factor is the role of thermal budget. The thermal stability of NiO/Ga_2O_3 heterointerfaces is also of interest from the viewpoint that the metallurgical and electrical junctions are separated, whereas they coincide in a Schottky rectifier and should make the pn junction less sensitive to thermal degradation.

In this paper we report measurements of the band alignment as a function of post-deposition annealing temperature up to 600°C and see a monotonic increase in the values of the staggered band offsets with annealing temperature.

2. Experimental

We used vertical rectifier structures for the measurement of band alignments. These consisted of a 10 µm thick, lightly Si doped epitaxial layer grown by halide vapor phase epitaxy (HVPE) with carrier concentration $2x10^{16}$ cm^{-3}, on a (001) surface orientation Sn-doped β-Ga_2O_3 single crystal (Novel Crystal Technology, Japan).

The band gaps of NiO for as-deposited films and those after annealing at different temperatures were obtained using UV-Vis (Perkin-Elmer Lambda 800 UV/Vis spectrometer). These films were 60nm thick and were sputtered on quartz. The absorbance spectrum were collected and Tauc plots were used to calculate the bandgap of the NiO.

The band alignments were obtained using the X-Ray Photoelectron Spectroscopy (XPS) based technique initially developed by Kraut et al.[40] This requires preparation of three samples. In the first, the core levels and valence band maxima (VBM) positions are measured from a thick NiO layer and in the epitaxial Ga_2O_3. These same core level locations were re-measured in a NiO/Ga_2O_3 heterojunction consisting of 5nm NiO sputtered on Ga_2O_3. The shift of the core level binding energy locations (ΔECL) within the heterostructure determines the valence band offset (ΔE_V) from [38,39]

$$\Delta E_V = \Delta \text{ ECL} + (E_{Core} - E_{VBM})_{Ref.\ NiO} - (E_{Core} - E_{VBM})_{Ref.\ Ga_2O_3}$$

NiO was deposited by magnetron sputtering at 3mTorr and 100W of 13.56 MHz power using two targets to achieve a deposition rate around 0.2 Å.sec^{-1}. The Ar/O_2 ratio was used to control the doping in the NiO in the range $2x10^{18}$- 3 $x10^{19}$ cm^{-3}, with mobility < 1 $cm^2 \cdot V^{-1}$ s^{-1}.

The temperature of the sample during deposition was monitored by temperature-sensitive alloys placed next to the Ga_2O_3 and was <100°C throughout. A representative cross-sectional transmission electron microscopy (TEM) image is shown in Figure 1, in this case of a structure subsequently used for device measurements and consisting of a bilayer of NiO on the Ga_2O_3. There is a small amount of near-surface damage in the top 10 nm of the Ga_2O_3 layer, which is likely due to sputtering-induced disorder during deposition of the NiO. However, the interface is atomically abrupt with no extended defects.

3. Results and Discussion

To obtain the conduction band offsets, we also need to measure the bandgaps of the constituent layers within the heterojunction. This was done for separate layers of NiO annealed for 5 min at temperatures from 300-600°C under an O_2 ambient using Rapid Thermal Annealing (RTA). Figure 2(a) shows Ultraviolet-Visible Spectroscopy (UV-Vis) absorption data, while the corresponding Tauc plots are shown in Figure 2(b). The extracted bandgap decreased with annealing temperature, from 3.90 eV for as-deposited films to 3.72 eV for those annealed at 600°C, as tabulated in Table 1.

The high resolution XPS spectra for the vacuum-core delta regions of Ga_2O_3 are shown in Figure 3 for samples annealed at different temperatures up to 600°C. The ΔE_V values are then extracted from the shift of the core levels for the heterojunction samples with the thin NiO overlayers [38,39]. The XPS spectra from which we extracted the core energy differences to VBM for thick NiO layers after different annealing temperatures are shown in Figure 4. The corresponding VBMs are shown in Table 1. The error bars in the different binding energies were combined in a root sum square relationship to determine the overall error bars in the valence band offsets [33]. Note that sample charging is not an issue when determining band offsets since

we only need peak core shift deltas, which will shift all binding energies by the same amount. We also did not observe any differential charging, which could shift peaks by different amounts and could potentially be a large source of error.

Figure 5 shows the band alignment of NiO on Ga_2O_3 after the different annealing temperatures. The valence band offsets were 0.90± 0.20 eV for the as-deposited heterojunction, 2.10± 0.30 eV after annealing at 300°C, 2.60 ± 0.30 eV after annealing at 400°C and 2.90 ± 0.35 eV for annealing at 500°C and 3.0± 0.35 eV for annealing at 600°C. The respective conduction band offsets are then 0.20 eV (as-deposited), 1.34 eV (300°C), 1.76 eV (400°C), 2.04 eV (500°C) and 2.12 eV (600°C). The band alignment is staggered, type II in all cases. It has been shown that for dielectrics with type II band alignment with a negative ΔE_V, high temperatures and/or illumination can cause holes from Ga_2O_3 to move into the metal, greatly increasing the leakage current [41,42]. Note that the band offsets increase monotonically with annealing temperature and will not provide any barrier to electrons moving into the Ga_2O, suggesting that NiO may not be an optimum choice as a guard-ring material on rectifiers, although Gong et al. [23] noted that in addition to the band offset, there was an additional built-in potential of 0.78 V at the interface due to the charge transfer across the p-n-junction. The entire NiO/Ga_2O_3 heterojunction also does not display thermal stability beyond 300°C.

Our band offsets are only in general agreement with these of Gong et al. [23] for the samples annealed at 600°C, although they did not indicate any annealing of their samples. Similarly, the valence band offsets reported by Ghosh et al. [37], Zhang et al [29] and Lu et al. [16] would fall between a temperature cycle in the range ~275-325°C, judging from our data, if thermally-induced changes were the only cause. The fact that the sputter rate of NiO is slow does allow for significant opportunity for sample heating during the deposition. Hays et al.[39] also

summarized other possible reasons for variations in band offsets between nominally similar systems, including different strain, interfacial disorder and contamination, stoichiometry and chemical bonding variations. At this stage, the exact cause cannot be isolated and awaits more experiments where deposition conditions are carefully controlled.

4. Conclusions

There is still additional work that must be done to better understand carrier transport across the NiO/Ga_2O_3 interface and how this varies with doping level in the NiO and annealing temperature. The large reported variations in band offsets in this system requires examination of less energetic deposition methods than sputtering. The NiO/Ga_2O_3 heterojunction is showing much promise for enhancing the capability of Ga_2O_3 power devices, but must be optimized to obtain reproducible benefits.

5. Conflicts of interest

There are no competing financial interests in this paper.

6. Data Availability

All data that support the findings of this study are included within the article.

7. Acknowledgments

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Table 1. (top) NiO bandgap measured by UV-vis and valence band offsets measured by XPS data as a function of post-deposition annealing temperature.

Anneal T(°C)	**E_G (eV)**	**ΔE_V (eV)**
As-deposited	3.90	2.39
300	3.84	2.87
400	3.76	2.87
500	3.74	3.05
600	3.72	2.88

Summary of measured core levels (eV) for NiO, and a heterostructure of NiO deposited on GaN as a function of post-deposition annealing temperature.

	Bulk NiO			**NiO/GaN heterojunction**		
Anneal T(°C)	**VBM**	**Core Level Peak (Ni 2p)**	**Core-VBM**	**Core Level Peak (Ga 3d)**	**Core Level Peak (Ni 2p)**	**△Core level**
As-deposited	-0.6	853.4	854.0	18.27	852.48	834.21
300	-1.8	853.2	855.0	17.72	852.45	834.73
400	-1.9	853.1	855.0	17.71	852.44	834.73
500	-1.9	853.4	855.3	17.7	852.55	834.85
600	-1.7	853.7	855.4	17.37	852.49	835.12

Figure Captions

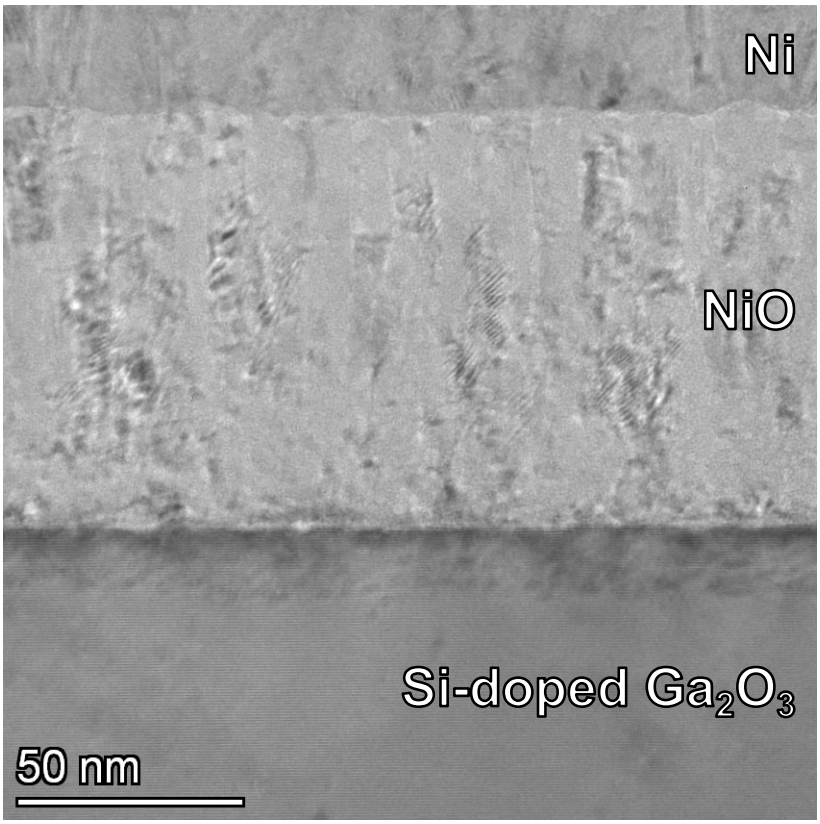
Figure 1. High-resolution TEM image of the NiO/ GaN heterojunction.

Figure 2.ΔCore level calculations for interfaces of thin NiO/GaN as-deposited and annealed at different temperatures.

Figure 3. High resolution XPS spectra for the vacuum-core delta region of reference GaN sample.

Figure 4. Core-VBM calculations for thick NiO film as-deposited and annealed at different temperatures.

Figure 5. Schematic of band alignments for NiO/GaN as a function of post-deposition annealing temperature.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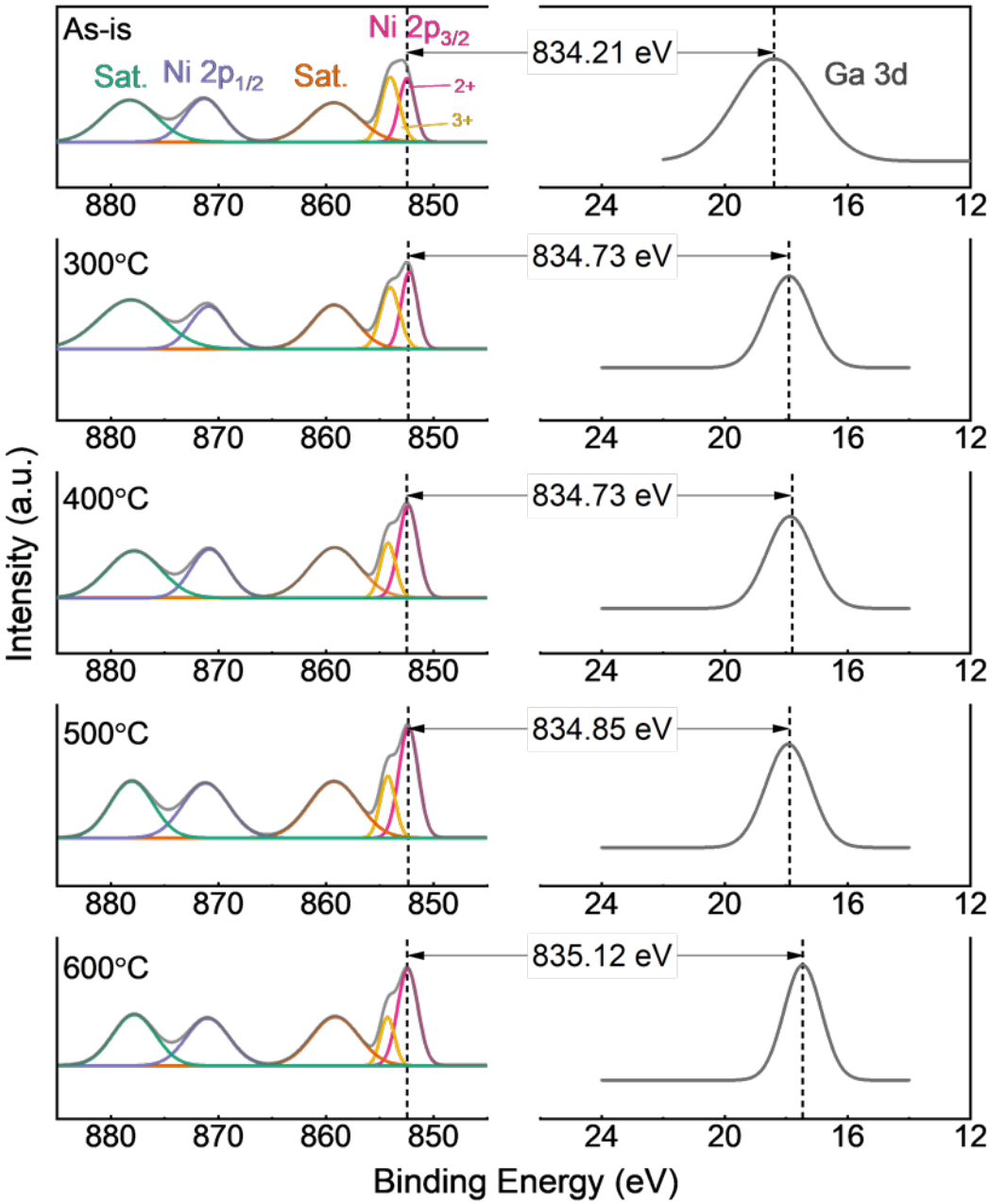
NiO
Si-doped Ga_2O_3
50 nm


As-is
Sat.
Ni 2p1/2
Sat.
Ni 2p3/2
2+
3+
834.21 eV
Ga 3d
300°C
834.73 eV
400°C
834.73 eV
500°C
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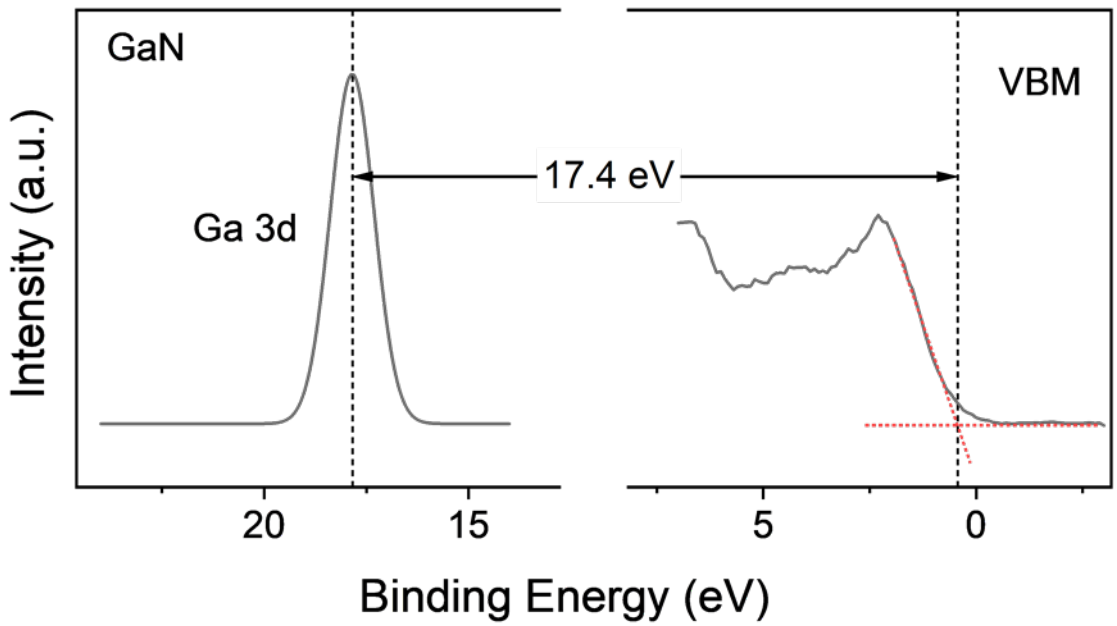
16
12
Intensity (a.u.)
Binding Energy (eV)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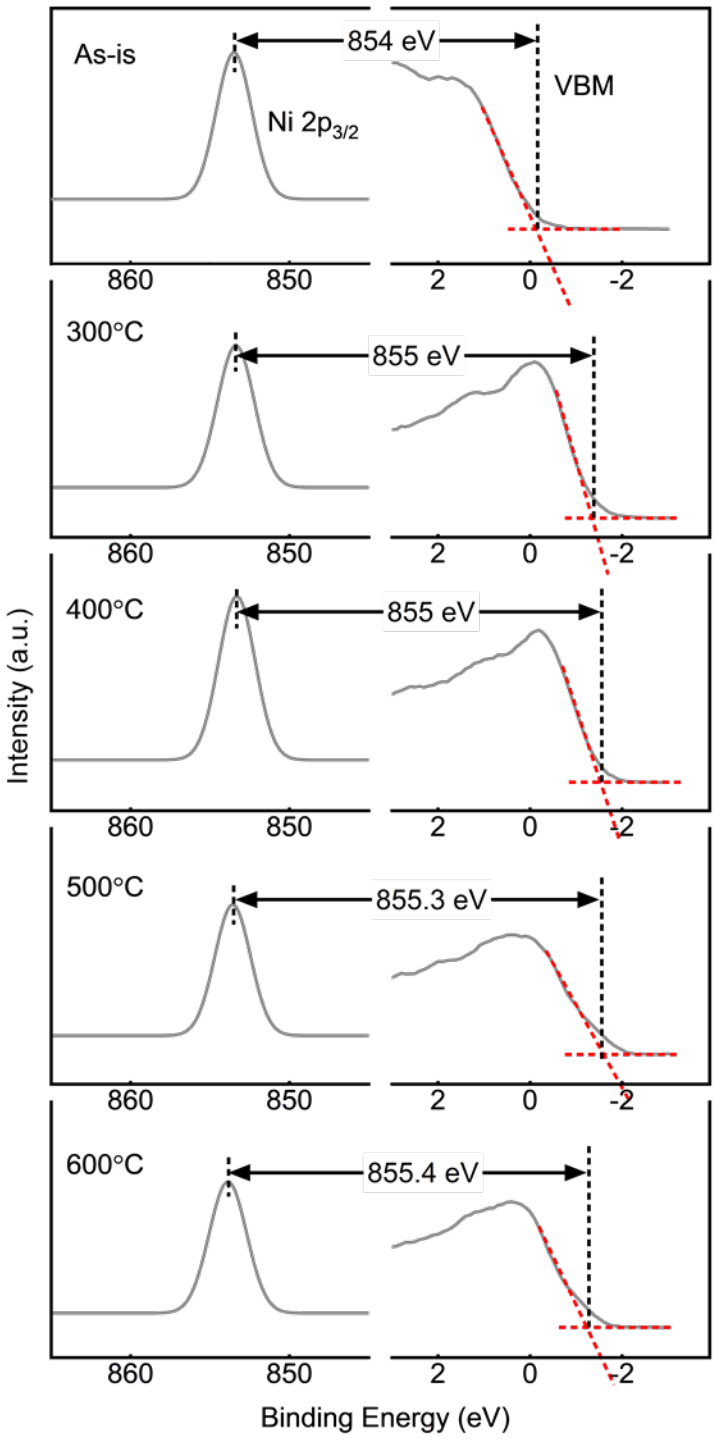
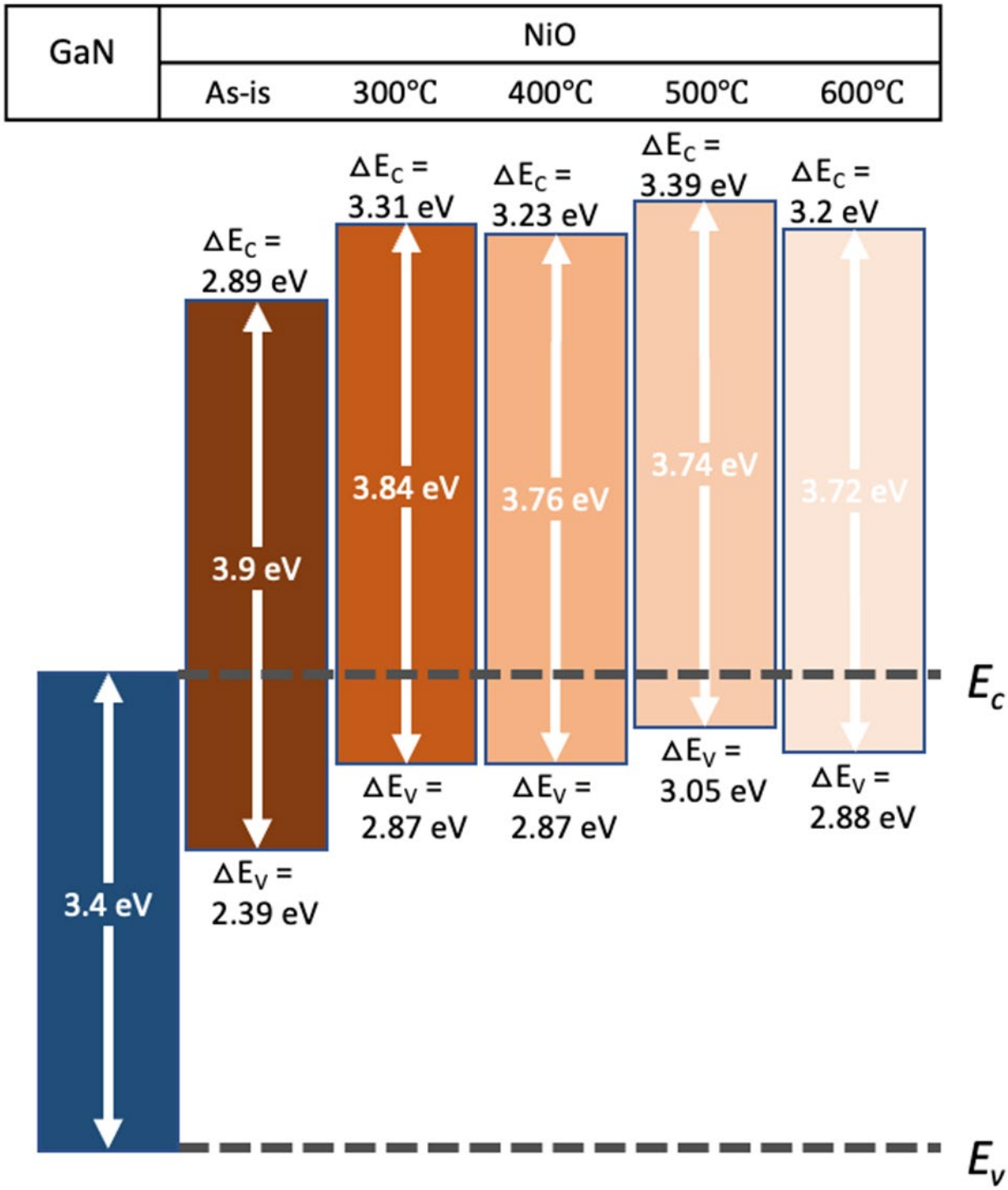
Ga 3d
17.4 eV
VBM
Intensity (a.u.)
20
15
5
0
Binding Energy (eV)


As-is
854 eV
VBM
Ni 2p3/2
860
850
2
0
-2
300°C
855 eV
400°C
855 eV
500°C
855.3 eV
600°C
855.4 eV
Intensity (a.u.)
Binding Energy (eV)


GaN
NiO
As-is
300°C
400°C
500°C
600°C
ΔE_C = 2.89 eV
ΔE_C = 3.31 eV
ΔE_C = 3.23 eV
ΔE_C = 3.39 eV
ΔE_C = 3.2 eV
3.9 eV
3.84 eV
3.76 eV
3.74 eV
3.72 eV
E_c
ΔE_V = 2.39 eV
ΔE_V = 2.87 eV
ΔE_V = 2.87 eV
ΔE_V = 3.05 eV
ΔE_V = 2.88 eV
3.4 eV
E_v