β-$(Al_{0.18}Ga_{0.82})_2O_3/Ga_2O_3$ Double Heterojunction Transistor With Average Field of 5.5 MV/cm

Nidhin Kurian Kalarickal, Zhanbo Xia, *Member, IEEE*, Hsien-Lien Huang, Wyatt Moore, Yumo Liu, Mark Brenner, Jinwoo Hwang, and Siddharth Rajan

***Abstract*— Maintaining high average fields between the gate and drain is imperative in achieving near theoretical performance in ultra-wide band gap semiconductors like β-Ga_2O_3. In this letter we report on a field management strategy to reduce the peak electric field at the drain side corner of the gate by using a composite dielectric layer consisting of an extreme permittivity dielectric like $BaTiO_3$ and a low-κ dielectric like SiO_2 overlapped over the gate electrode. Using this strategy in β-$(Al_{0.18}Ga_{0.82})_2O_3$/ Ga_2O_3 double heterojunction field effect transistor, we achieved a record average breakdown field of 5.5 MV/cm at a gate-drain spacing of 1.15 μm along with an improved power figure of merit of 408 MW/cm^2. The reported works shows the effectiveness of integrating extreme dielectric materials with ultra-wide band gap semiconductors in significantly improving breakdown performance.**

***Index Terms*— Gallium oxide, perovskite oxide, barium titanate, power figure of merit, breakdown.**

I. Introduction

ULTRA-WIDE bandgap semiconductors like β-Ga_2O_3 and AlGaN offer the next avenue for improved performance in power switching devices [1]–[3]. The promise in these materials stem from the much larger breakdown field strength [4]–[6], offering improved theoretical performance in power devices as described by the Baliga's figure of merit (V_{br}^2/R_{ON}) [7]. Among the ultra-wide band gap materials, β-Ga_2O_3 stands out mainly due to the availability of bulk substrates that can be grown from melt [8]–[13]. Therefore, if the theoretical breakdown field and transport properties can be achieved, β-Ga_2O_3 power switching devices with better performance will be available at lower cost.

The absence of p type doping and availability of dielectrics that can sustain electric field significantly higher than 8 MV/cm makes achieving the theoretical breakdown field strength challenging. Integration of extreme-κ ($\epsilon > 100$) gate dielectrics with ultra-wide band gap materials is one approach to solving this problem especially in lateral field effect transistors, [6], [14] where the presence of extreme-κ gate dielectric has been shown to result in improved uniformity in the electric field profile [15]. The large dielectric constant also ensures that the vertical component of the electric field seen at the gate is significantly reduced. But, as will be shown in section II, the lateral component of the electric field still leads to a significant peak electric field at the gate corner.

In this letter, we show using 2D device simulation followed by experimental demonstration, a field management strategy utilizing a composite extreme-κ/low-κ dielectric overlapping the gate, to reduce the peak electric field at the gate corner, resulting in improved breakdown performance.

II. Device Design and Fabrication

Consider the β-$(AlGa)_2O_3/Ga_2O_3$ thin spacer (1 nm) modulation doped double heterojunction transistor with a 2D electron gas density of 1×10^{13} cm^{-2} as shown in Fig.1 (a) (transistor A) [16], [17]. Transistor A has a bilayer gate dielectric stack consisting of a low-κ dielectric (dielectric 1-Al_2O_3) and an extreme-κ dielectric ($BaTiO_3$, $\epsilon_b = 203$) of thickness t_{b1}. Fig.1 (c) shows the 2-D distribution of electric field between the gate and drain terminals of transistor A at a reverse bias of 800 V (average field = 4 MV/cm). The plot in Fig.1 (c) shows the electric field profile along the cutline A-A'. We see that the presence of extreme-κ dielectric leads to significant uniformity of electric field within the gate-drain region as has been reported earlier [18], but at the gate corner this uniformity is lost resulting in a high peak field of ~9 MV/cm. The large dielectric discontinuity present in the y direction results in partial screening of the negative charges on the gate. But due to absence of polarization charges along the vertical edge of the gate (Fig.1 (a)), the negative charges are not fully screened, resulting in a significant peak electric field at the corner. This is detrimental since most of the extreme-κ dielectrics like $BaTiO_3$ and $SrTiO_3$ have breakdown fields similar to β-Ga_2O_3 [19].

Fig. 1 (b) shows a transistor design (transistor B) with a field management structure that consists of an extreme-κ/low-κ composite dielectric deposited over the gate electrode of

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Nidhin Kurian Kalarickal, Zhanbo Xia, Wyatt Moore, and Mark Brenner are with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210 USA (e-mail: kalarickal.1@osu.edu).

Hsien-Lien Huang, Yumo Liu, and Jinwoo Hwang are with the Department of Material Science and Engineering, The Ohio State University, Columbus, OH 43210 USA.

Siddharth Rajan is with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210 USA, and also with the Department of Material Science and Engineering, The Ohio State University, Columbus, OH 43210 USA.

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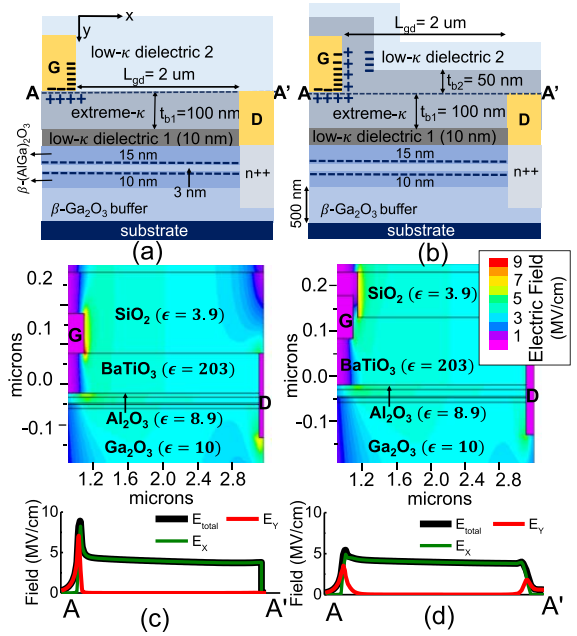

Fig. 1. (a) Transistor design A (gate-drain region). (b) Transistor design B (gate-drain region). (c) Simulated electric field contour profile in transistor A at a reverse bias of 800 V. (d) simulated electric field contour profile in transistor B at a reverse bias of 800 V. The plots in (c) and (d) show the electric field profile along the cutline A-A' as shown.

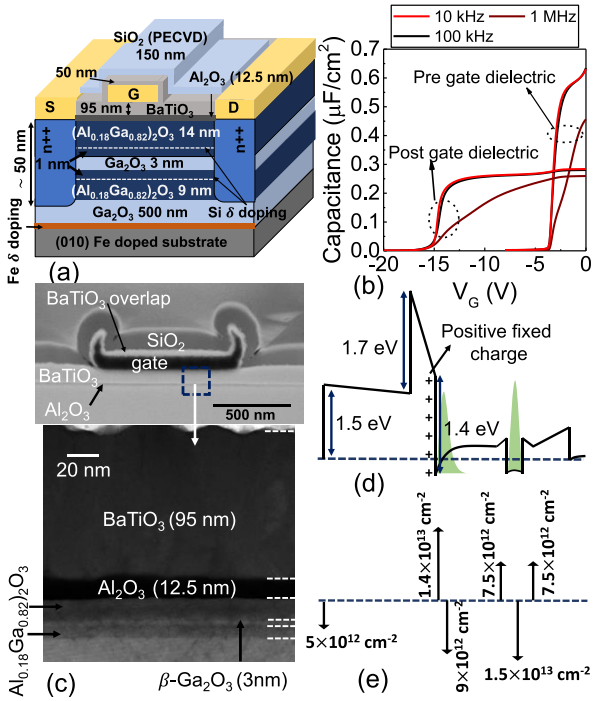

Fig. 2. (a) Epitaxial and final device structure. (b) Comparison of the capacitance-voltage measurements performed pre and post deposition of gate dielectric layers. (c) Cross sectional STEM image of $BaTiO_3/\beta$-Ga_2O_3 DHFET ($L_g = 0.9\mu m$) showing the $BaTiO_3/SiO_2$ field management structure and the epilayer and dielectric stack. The vertical protrusions on both sides of the gate are unintentional lift off edges. (d) Schematic band diagram of $SiO_2/BaTiO_3/\beta$-Ga_2O_3 DHFET including the positive fixed charges at the Al_2O_3/β-$(Al_{0.18}Ga_{0.82})_2O_3$ interface (e) Charge diagram showing the distribution of charges in the device.

transistor A. This provides an extreme dielectric discontinuity in both x and y directions. Fig. 1 (d) shows the electric field distribution between the gate and drain terminals of transistor B at the same reverse bias of 800 V. Due to the presence of the extreme dielectric discontinuity in both directions, the polarization charges formed in the extreme-κ dielectric completely screens the negative charges on the gate (Fig.1 (b)), reducing the overall peak field at the gate corner. The plot in Fig.1 (d) quantifies this reduction in peak field to below 6 MV/cm. Usage of a low-κ overlap dielectric with a large breakdown field like SiO_2, would ensure that transistor B has a much higher breakdown voltage compared to transistor A. The low-κ overlap dielectric is required since in its absence, the peak field is at the air/extreme-κ interface which is detrimental.

We fabricated lateral field effect transistors similar to transistor B using β-$(Al_{0.18}Ga_{0.82})_2O_3$/ Ga_2O_3 modulation doped double heterojunction, epitaxially grown using molecular beam epitaxy (MBE) as shown in Fig. 2 (a) and (c). Fe delta doping was carried out at the substrate-epilayer growth interface to prevent formation of unintentional parasitic channel due to Si impurity. Further details on the MBE growth of the epilayer and doping may be found in references [16], [17], [20].

Ohmic contacts were laid down using MBE regrowth technique [21] followed by ohmic metallization using Ti/Au/Ni (40/50/50 nm) stack annealed at 470 °C in N_2 ambient. Device isolation was carried out by etching a 180 nm deep mesa structure using BCl_3/Ar based dry etch [22]. 12.5 nm of Al_2O_3 dielectric (10 nm intended) was then deposited using atomic layer deposition (ALD). The Al_2O_3serves as a protective layer preventing damage to semiconductor surface during the subsequent radio frequency sputtering (670 °C) of $BaTiO_3$ gate dielectric (95 nm). Further details on sputtering of $BaTiO_3$ may be found in [18]. The extreme-κ gate dielectric is intentionally made thick since this improves the uniformity of electric field profile between the gate and drain [18]. Cr/Pt (5/100 nm) metal stack was then deposited to form the Schottky gate. Cr layer was added to improve adhesion of Pt with $BaTiO_3$. Following the deposition of gate, 50 nm of $BaTiO_3$ (RF sputtering) and 150 nm of SiO_2 (plasma enhanced chemical vapor deposition at 250 °C) is deposited to form the overlap field management structure as shown in Fig.2 (a) and (c).

III. Results and Discussion

Hall effect measurements were carried out on the epilayer before and after the deposition of gate dielectric layers (Al_2O_3 + $BaTiO_3$) giving a mobility of 85 cm^2/V-s and a charge density of 9.4×10^{12} cm^{-2}. Transfer length measurements (TLM) showed a total contact resistance of 5.5 Ω·mm in these devices pre deposition of $BaTiO_3$. The specific contact resistance between the metal and regrown layer (R_{sh} ~250 Ω/sq) was found to be 10^{-6}Ω·cm^2. Fig.2 (b) compares the capacitance-voltage (C-V, 200 μm pads) measurements performed on the devices before and after the deposition of gate dielectric layers (Al_2O_3+$BaTiO_3$). Negligible frequency dispersion is observed below 100 kHz, whereas significant dispersion is observed at 1 MHz. Since the dispersion is present before and after the deposition of gate dielectrics, the traps responsible must be inherent to the epitaxial structure and not from the dielectrics. As shown in Fig.2 (a), intentional Fe doping was carried out at the epilayer/substrate interface to compensate parasitic channel formation due to remnant

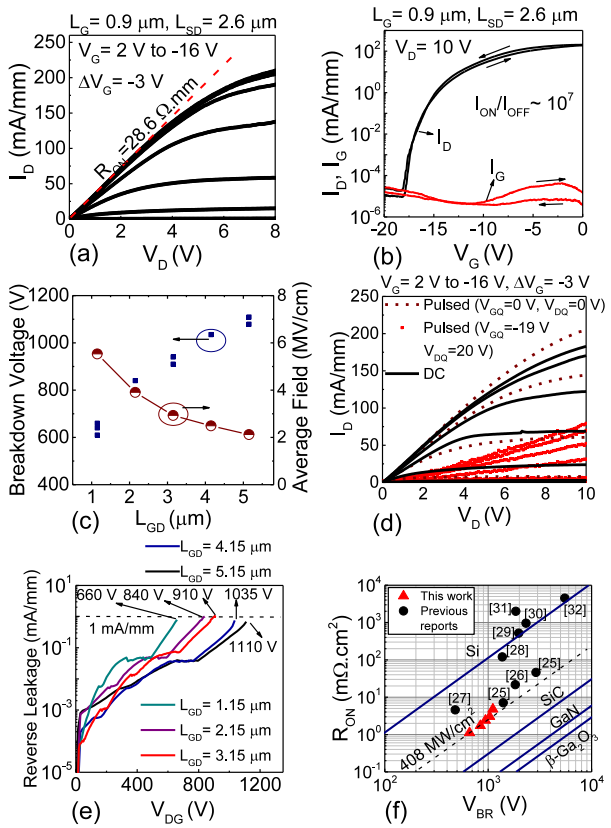

Fig. 3. (a) Output characteristics of $BaTiO_3$/β-Ga_2O_3 DHFET (L_g = 0.9 um, L_{sd} = 2.6 μm). (b) Transfer characteristics of $BaTiO_3$/β-Ga_2O_3 DHFET (L_g = 0.9 um, L_{sd} = 2.6 μm). (c) Pulsed I-V characteristics of $BaTiO_3$/β-Ga_2O_3 DHFET (L_g = 1.2 μm, L_{sd} = 4 μm). (d) Measured breakdown voltage and average breakdown field vs L_{gd}. (e) Reverse leakage current as a function of gate-drain bias for different values of L_{gd}. (f) $V_{br} - R_{ON}$ benchmark plot for β-Ga_2O_3 lateral transistors [25]–[32].

Si impurities. This results in a significantly longer Fe tail (~500 nm) deep into the buffer [16] which was previously shown to cause trapping and dispersion issues [23]. Increasing the buffer thickness such that the Fe tail is kept at least 400 nm away from the channel was previously found to reduce Fe related dispersion issues [23]. By comparing the 2DEG capacitance value measured before ($V_g = -1$ V) and after deposition ($V_g = -7.2$ V) of gate dielectrics, a dielectric constant of 203 for the $BaTiO_3$ layer is estimated ($\epsilon_{Al_2O_3}$ of 8.9 is assumed [24]). Channel charge density (n_s) of 1.1×10^{13} cm^{-2} is obtained in devices before the deposition of gate dielectrics, whereas $n_s$of 2.4×10^{13} cm^{-2} is observed in devices after the deposition of gate dielectric layers (100 kHz). This increase in $n_s$is likely due to the presence of positive fixed charges at the Al_2O_3/β-$(Al_{0.18}Ga_{0.82})_2O_3$ interface resulting in the formation of a parasitic channel. Fig.2 (d), (f) shows the band diagram and charge diagram of the device considering this positive fixed charge density (1.4×10^{13} cm^{-2})at the Al_2O_3/β-$(Al_{0.18}Ga_{0.82})_2O_3$ interface assuming a schottky barrier height of 1.5 eV to $BaTiO_3$ and band offsets given in [6].

Fig.3 (a) shows the measured output characteristics of the $BaTiO_3$/β-Ga_2O_3 DHFET with a source-drain (L_{sd}) spacing (gate length and gate-drain spacing) of 2.6 μm (0.9 μm and 1.15 μm). The device shows an on-resistance (R_{ON}) of 28.6 Ω·mm and a max drain current of 220 mA/mm at a gate bias of 2 V. As is clear from Fig.3 (a), the parasitic 2DEG at the Al_2O_3/β-$(Al_{0.18}Ga_{0.82})_2O_3$ interface being a low mobility channel leads to only a minimal increase in drain current (or reduction in R_{ON}) above a gate voltage of -4 V. The measured R_{ON} increases from 28.6 Ω·mm at L_{sd} of 2.6 μm to 59 Ω·mm at L_{sd} of 6.8 μm. Fig.3 (b) shows the transfer characteristics of the same device showing an on-off ratio of roughly 10^7.

Fig.3 (c) shows the pulsed I-V characteristics of a representative device with $L_g = 1.2$ μm an $L_{sd} = 4$ μm. Pulse width was set to a value of 5 μs with a duty cycle of 0.1%. A significant increase in R_{ON} from 41 Ω·mm to 125 Ω·mm is observed when comparing the DC and pulsed ($V_{GQ} = -19$ V, $V_{DQ} = 20$ V) measurements. Similar to the dispersion observed in the C-V measurements (Fig.2 (b)), the intentional Fe doping at the epilayer/substrate interface and the resulting long Fe tail deep into the buffer was found to cause trapping, resulting in current collapse [23]. Increasing the buffer layer thickness ensuring sufficient (>400 nm) separation between the channel and the Fe tail would ensure significantly improved pulsed I-V characteristics in future devices.

Two terminal breakdown (gate-drain) measurements were carried out on the devices to assess the effectiveness of the field management structure. Fig.3 (d) and (e) shows the breakdown characteristics of the devices as the gate-drain spacing is increased from 1.15 μm to 5.15 μm. The device dimensions reported were confirmed using cross sectional STEM imaging. The measured breakdown voltage (averaged value at a given L_{gd}) increases from 636 V (5.5 MV/cm) to 1095 V (2.1 MV/cm) as the gate-drain spacing (L_{gd}) is increased from 1.15 μm to 5.15 μm, with the best device at $L_{gd} = 1.15$ μm (L_{sd} =2.6 μm) showing a breakdown voltage of 660 V (5.7 MV/cm). The average field (F_{av}) of 5.7 MV/cm is the highest reported in any β-Ga_2O_3 transistor device showing the effectiveness of the field management strategy used in this study. At larger gate-drain spacing the field-management is less effective due to the large $n_s(2.4\times10^{13}$ cm$^{-2})$ being modulated [18].

The power figure of merit for these devices (V_{br}^2/R_{ON}) can be estimated by normalizing R_{ON} to the active area of the transistor, $L_{sd} + 2L_T$, where L_T corresponds to the transfer length between the metal and the regrown layer ($2L_T$ = 1.3 μm). Record high PFOM of 408 MW/cm^2 (558 MW/cm^2 without L_T) at an L_{sd} of 3.5 μm (R_{ON} = 1.72 mΩ·cm^2, V_{br} = 840 V) and 390 MW/cm^2 (586 MW/cm^2 without L_T) at an L_{sd} of 2.6 μm (R_{ON} = 1.11 mΩ·cm^2, V_{br} = 660 V) are obtained as shown in Fig. 3 (f). We note that the high PFOM was achieved despite the parasitic channel which did not contribute to conduction.

IV. Conclusion

In conclusion, we demonstrate a field management strategy to reduce the peak electric field at the drain side corner of the gate by using an extreme-κ /low-κ composite dielectric overlapped over the gate electrode. Utilizing this method in $BaTiO_3$/β-Ga_2O_3 double heterojunction transistor enabled a record average electric field of 5.5 MV/cm and a PFOM of 408 MW/cm^2 at a source-drain spacing of 3.5 μm.

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