A Cascaded Hybrid Switched-Capacitor DC-DC Converter Capable of Fast Self Startup for USB Power Delivery

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***Abstract*—Hybrid switched-capacitor DC-DC converters show promise in applications that require high conversion ratios and small physical size. However, the problem of flying capacitor voltage imbalance, especially during transients, remains a major challenge that limits the adoption of such converters. This paper presents a highly integrated hybrid switched-capacitor converter for USB powered applications, featuring fast balancing dynamics. The topology consists of two cascaded stages to increase the conversion ratio. The output voltage regulation and flying capacitor active balance are both achieved by modified ripple injection control, with an additional phase skipping technique further improving the transient response during startup. Fabricated in 0.18μm CMOS technology, the converter prototype has a peak efficiency of 96.9% for 5V:1.2V conversion. Safe startup can be achieved with the input voltage rising from 0 to 5V within 8μs (0.62V/μs slew rate).**

***Index Terms*—DC-DC converter, hybrid switched capacitor, capacitor balance, converter startup, USB power delivery.**

I. Introduction

As advances in CMOS technology push low-voltage digital power supplies down to the sub-volt range, there is growing pressure on DC-DC conversion systems to operate efficiently at ever smaller size and with more extreme conversion ratios, while also providing fast transient response [1]. Design of such power converters can be challenging, as traditional step-down topologies are limited by the size and performance of passive components, particularly inductors [2].

Known as one of the most prolific step-down topologies in power electronics, the Buck converter uses an inductor as the primary energy-storage element. Due to relatively low energy density [3], inductors often dominate the converter size, thus deteriorating the overall power density. Moreover, active power devices are required to block the full input voltage, which impacts size and efficiency. At large step-down ratios ($V_{in} \gg V_{out}$), narrow pulse-widths complicate duty-cycle control and gate driving, limiting the switching frequency and presenting further trade-offs among size, ripple, and efficiency.

Switched-capacitor (SC) converters leverage the relatively higher energy-density of capacitors to improve efficiency and power-density in size-constrained applications [4]–[6]. Large step-down ratios can be achieved through hierarchical and cascaded switched capacitor networks controlled by an array of low-voltage-rated switches. However, challenges associated with the SC approach include the intrinsic charge sharing and efficiency degradation when implementing wide-range output voltage regulation [7], [8].

Hybrid switched-capacitor converters combine elements of Buck and SC converters, using both capacitors and inductors as energy storage components. The benefits can be appreciated from two different perspectives. On one hand, by adding one or more inductors to a switched capacitor network, soft charging and efficient regulation characteristics can be achieved [9]. On the other hand, by adding high-energy-density capacitors to an inductor-based converter, energy storage requirements of inductors and therefore the overall volume can be reduced [10]. Additionally, because the inductor only sees a fraction of the input voltage, duty-cycle pulse widths are increased, relaxing timing requirements and root-mean squared (RMS) to DC current ratios in the circuit.

Although showing promising performance, challenges exist in the practical application of hybrid SC converters, highlighted by the issue of flying capacitor imbalance [12]–[15]. Flying capacitor networks in pure SC converters are rigidly constrained by Kirchhoff's voltage law: charge is transferred through capacitive loops (including flying capacitors and input/output bypass capacitors), which show simple dynamics and lead to a unique (balanced) voltage for each flying capacitor. However, in hybrid topologies, the charge transfer path typically links an inductor, which breaks the pure capacitive loops and increases the order of dynamics. Flying capacitors become independent energy storage elements and their unique (balanced) voltages are no longer guaranteed. This imbalance can increase switch voltage stress and ripple quantities, potentially compromising the reliability and efficiency.

Imbalance may occur due to non-idealities in practical implementation (mismatched switch timing, source impedance, initial conditions) [16]–[18] or even in certain ideal scenarios [19], and the worst case often happens in transients. For example, during converter startup, the input voltage may increase rapidly. Flying capacitor voltages, which assume a nominal fraction of the input voltage, must track this and other supply transients to avoid exposing power switches to excessive voltage stress. Therefore, fast balancing dynamics are crucial for safe operation during supply transients (including startup). Explored approaches to achieve flying capacitor balance in hybrid SC converters include relying on natural balancing [20]–[22], flying capacitor precharge [1], [23], and active balancing control [24], [25].

This paper expands the previous work in [26] and reports a hybrid SC converter for USB powered computing applications (5V:0.4-1.2V) in 0.18μm CMOS process. A new topology is presented that leverages a two-stage step-down architecture,

optimized for efficiency, transient performance, and balancing dynamics. Modified ripple injection control [25] regulates the output voltage and maintains balance of the converter; a phase-skipping technique is introduced that further accelerates the balancing dynamics during startup. All gate drivers including the bootstrap capacitors are fully integrated, supplied by internal voltages on either flying capacitors or the input node. Measured results show a peak efficiency of 96.9% for 5V:1.2V conversion, less than 36mV undershoot and overshoot for 1A/μs loading and unloading transients, and self startup time on the order of 10μs, which is over 100 times faster than the closest prior art.

The remaining sections are organized as follows. Section II introduces the converter topology and its principle of operation. Section III reiterates the general characteristics of modified ripple injection control and explains the phase skipping technique. Section IV describes the circuit implementation of gate drivers as well as core control blocks. Section V reports the measured results and section VI concludes this work with a performance summary and comparison.

II. Cascaded Hybrid Topology

As discussed in [27], there are a wide range of possible hybrid SC topologies, each derived loosely from a basis set of known switched capacitor network spanning Dickson, ladder, series-parallel, Fibonacci, and doubler. Each of these topologies also has a variety of advantages and disadvantages related to active and passive component utilization, ease of implementation, and achievable conversion ratio per unique active or passive component [4], [27]. However, as mentioned earlier and treated analytically in [28], the presence of an inductive impedance decouples various flying capacitor networks. While necessary to achieve 'soft-charging' per the discussion in [29], this decoupling results in higher-order dynamics which go in proportion to the number of independent capacitor networks in the converter. Therefore, higher-conversion-ratio topologies (with more flying capacitors thus more poles or eigenmodes [28]) are generally more difficult to regulate and balance.

Fig. 1 shows a two-stage step-down converter, where the SC network can be regarded as the reverse (exchange input and output) of the so-called doubler architecture. The multi-phase hybrid doubler has the distinction of achieving largest step-up (step-down when reversed) ratio per flying capacitor of all basic hybrid SC topologies [27]. With two flying capacitors (two balance objectives), along with the inductor and output capacitor, the two-stage step-down converter presents as a 4th-order system but achieves a nominal step-down ratio of 4.

In 4:1 operation, if balance is achieved, V_x is nominally $V_{in}/4$ in each phase. Referring to the equivalent circuit diagram in Fig. 1, it can be calculated that C_1 has a balanced voltage of $V_{in}/2$, and $V_{in}/4$ for C_2. With the frequency seen by the inductor denoted as f_{sw}, transistors in the first stage ($M_1 - M_4$) have a voltage stress of $V_{in}/2$ and switch at $f_{sw}/4$; transistors in the second stage ($M_5 - M_8$) have a voltage stress of $V_{in}/4$ and switch at $f_{sw}/2$. The advantage is that the higher voltage rated devices switch at a lower frequency to reduce their switching loss. Besides the nominal 4:1 operation, additional phases where the V_x node is connected to ground can be introduced to achieve V_{out} regulation, but the above principles still apply.

Closer investigation shows that switch M_5 can be removed from the topology. For example, the effect of turning off M_5 can be replicated by turning off both M_2 and M_3, decoupling the two power stages. This is similar to the high-Z or tri-state operation of the converter discussed in [1]. Removing M_5 simplifies gate driving and bootstrap circuits, saving die area and power loss. However, this results in V_{mid} switching between $V_{in}/2$ and $V_{in}/4$ at $f_{sw}/2$, causing CV^2 loss due to the associated parasitic capacitance. This problem will be further explained later in the section. Nevertheless, in this low frequency application, the power loss caused by such mechanism is insignificant compared to the power saved by removing switch M_5.

Another potential improvement on the two-stage step-down topology involves interleaving the first stage, shown in Fig. 2. Two interleaved copies, Φ_α and Φ_β, operate 180° out of

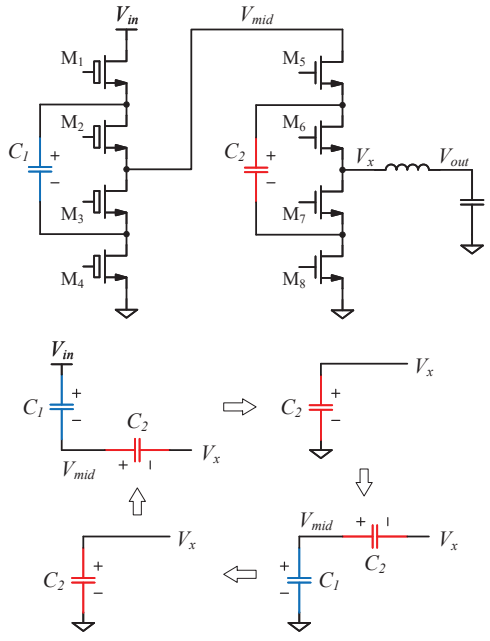

Fig. 1. The general schematic and equivalent circuit diagram in 4:1 operation of a two-stage step-down converter.

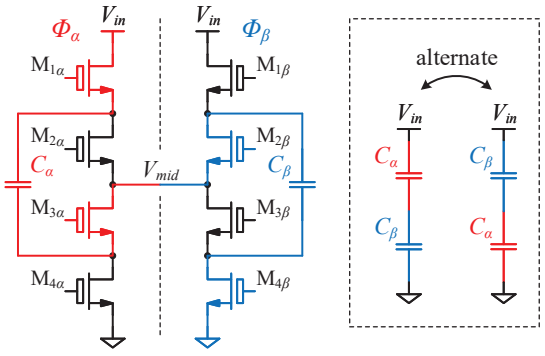

Fig. 2. Schematic and equivalent circuit diagram of first SC stage.

phase. In one switching state, the red switches in Φ_α and the blue switches in Φ_β are turned on, connecting the two flying capacitors, C_α and C_β, in series between V_{in} and ground. In another switching state, the black switches are turned on, forming the same equivalent circuit except that the two flying capacitors exchange position.

Interleaving the first stage indeed adds another flying capacitor, but it should be noticed that the order of the system is not increased, as the voltage on these two flying capacitors are not independent. The relationship

$$V_{C_\alpha} + V_{C_\beta} = V_{in} \tag{1}$$

holds true whenever C_α and C_β are connected. This ensures that there are no hard-charging losses in C_α and C_β in normal switching operation, and helps to accelerate balancing under line transients. As long as Φ_α and Φ_β are symmetric, any change of V_{in} will equally distribute between V_{C_α} and V_{C_β} with a time constant much smaller than the duration of the switching state; C_α and C_β operate as a capacitive divider such that the balanced V_{mid} voltage automatically tracks the supply voltage.

Another benefit of interleaving is that the required input bypass capacitance can be reduced. As one of C_α and C_β is always connected to ground, these serve as bypass capacitors for the second stage, providing a low-impedance path for high-frequency components regardless of the supply impedance. The interleaving also makes design of gate driving circuits more flexible, as will be discussed in section IV.

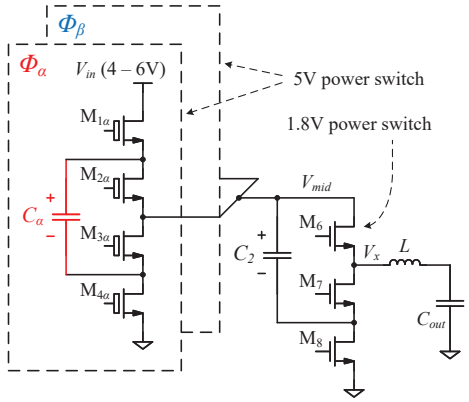

Fig. 3. The converter architecture used in this work.

Fig. 3 shows the proposed converter architecture after incorporating the aforementioned improvements. For an input voltage of 4-6V (nominally 5V), the voltage rating of the first stage power switches should be at least 3V. However, 5V switches were used due to their availability in the process technology and because the higher voltage rating did not result in a significant power loss penalty as the first stage switches at $f_{sw}/4$. In the second stage, the switch stress can be as high as 1.5V, and 1.8V devices were used.

In steady state operation, there are a total of 8 switching states ($\varphi_1 - \varphi_8$) in a period. The equivalent circuit in each state and exemplary waveforms are shown in Fig. 4. In state φ_1, switch $M_{1\alpha}$, $M_{3\alpha}$, $M_{2\beta}$, $M_{4\beta}$ and M_7 are turned on.

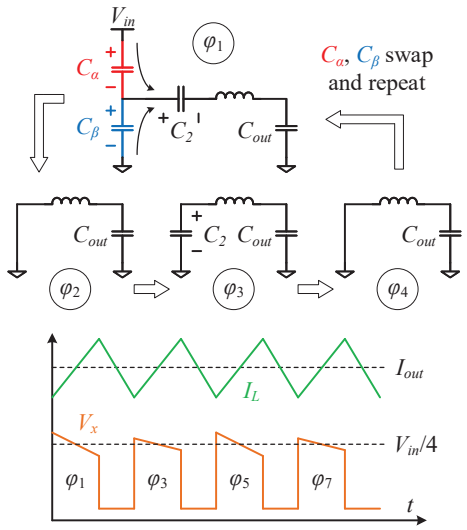

Fig. 4. The equivalent circuit in each switching state and exemplary waveform of the switching node voltage, V_x, and the inductor current, I_L.

Flying capacitor C_α is connected between V_{in} and V_{mid} while C_β between V_{mid} and ground. Flying capacitor C_2 is charged and the switching node voltage, V_x, is roughly at $V_{in}/4$. In state φ_2, switch M_7 and M_8 are turned on, connecting the switching node to ground. In state φ_3, switch M_6 and M_8 are turned on, discharging C_2. The switching node voltage, V_x, equals the voltage on C_2, which is again around $V_{in}/4$. State φ_4 is the same as state φ_2. It is worth noticing that switch $M_{4\alpha}$ and $M_{1\beta}$ are also turned on during $\varphi_2 - \varphi_4$ to avoid completely floating capacitors. The equivalent circuits in state $\varphi_5 - \varphi_8$ repeat $\varphi_1 - \varphi_4$ except that the first stage flying capacitors, C_α and C_β, swap position. It can be observed that the median node voltage, V_{mid}, is at $V_{in}/2$ during state φ_1 and φ_5, and at $V_{in}/4$ during $\varphi_2 - \varphi_4$ and $\varphi_6 - \varphi_8$. This is the effect of removing switch M_5 in the hybrid Doubler topology, discussed earlier in the section.

In this design, power switch sizes are optimized according to the trade-off between switching loss and conduction loss. Simulation of a typical operation (5V:0.9V, 0.25A load) shows a gate driving loss of 4.7mW and a conduction loss (including the switches and the inductor) of 5.2mW. Other mechanisms (switch overlap loss, C_{oss} loss, body diode loss, etc.) contributes an additional 5.0mW loss, and the simulated efficiency under this typical operation is 93.8%.

III. Regulation and Active Balance

Hysteretic control (a form of sliding mode control) is widely used in Buck converters for its fast transient response, robustness, and simple implementation [30]–[32]. It can be appreciated that if balance is maintained, the operation of hybrid SC converters is similar to Buck converters, as seen in the exemplary waveform in Fig. 4. These factors motivate using hysteretic control to achieve fast transient response in hybrid SC converters. First proposed in [25], modified ripple injection control (MRIC) is a hysteretic-based algorithm that achieves both output voltage regulation and active balance for

hybrid SC converters. This section first reviews the general principle of MRIC and then introduces the newly added phase skipping technique to further accelerate the startup.

A. Modified Ripple Injection Control

For Buck converters, a typical current-mode hysteretic controller generates a feedback signal, V_{fb}, that consists of the output voltage and the inductor current ripple [33]:

$$V_{fb} = V_{out} + k_i \cdot I_{L,AC}, \tag{2}$$

where k_i is the current to voltage gain. The feedback signal, V_{fb}, is compared to a reference voltage, V_{ref}, such that it is kept inside a hysteresis band around V_{ref}, thus achieving output voltage regulation. An alternative approach is adding hysteresis to V_{fb}:

$$V_{fb,hst} = \begin{cases} V_{fb} - \Delta V & \text{if } V_{fb} \text{ is rising,} \\ V_{fb} + \Delta V & \text{if } V_{fb} \text{ is falling,} \end{cases} \tag{3}$$

where $V_{fb,hst}$ is the feedback signal with added hysteresis; ΔV is half of the hysteresis window. When comparing $V_{fb,hst}$ and V_{ref}, a fast comparator without hysteresis can be used. These two methods are illustrated in Fig. 5. In an ideal case, the controller reacts instantaneously to any state deviation, ensuring fast transient response. However, in practice, sensing the inductor current ripple, $I_{L,AC}$, requires either a high-ESR output capacitor or a passive network that involves trade-offs among power consumption, die area, and bandwidth. To overcome this challenge, it was explored in [33] that an emulated $I_{L,AC}$ (a signal that is generated to resemble $I_{L,AC}$ but not necessarily from direct sensing) also works. In this design, the Volt-Amp characteristic of the inductor is used to emulate $I_{L,AC}$, depicted in Fig. 6.

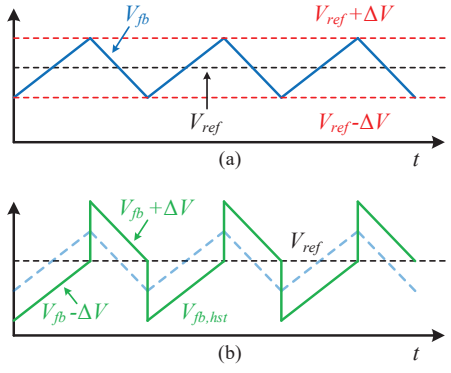

Fig. 5. Two equivalent ways to compare V_{fb} and V_{ref}: (a) use hysteretic comparator; (b) add hysteresis to V_{fb}.

Here we introduce the notation of odd and even states, φ_{odd} and φ_{even}, to represent switching states with odd and even sequence numbers, respectively. In balanced steady state, the switching node voltage, V_x, is roughly at $V_{in}/4$ in φ_{odd}, and is at zero in φ_{even} (refer to Fig. 4). Therefore, the slope of the actual inductor current ripple can be written as:

$$\frac{dI_{L,AC}}{dt} = \begin{cases} \frac{1}{L}(\frac{V_{in}}{4} - V_{out}) & \text{in } \varphi_{odd}, \\ -\frac{V_{out}}{L} & \text{in } \varphi_{even}. \end{cases} \tag{4}$$

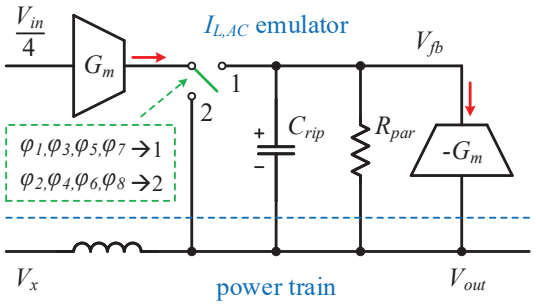

Fig. 6. Emulating the inductor current ripple, $I_{L,AC}$, using the Volt-Amp characteristic of the inductor.

The emulator in Fig. 6 generates the same slope by injecting modulated current into the ripple capacitor, C_{rip}. The value of parallel resistor, R_{par}, is chosen such that the current going through is much smaller than the two active branches (marked by red arrows). In φ_{odd}, the current $G_m V_{in}/4$ is directed to charge C_{rip}, therefore, the net current flowing into C_{rip} is the difference of the two active branch current. In φ_{even}, the current $G_m V_{in}/4$ has no effect on $V_{C_{rip}}$, thus C_{rip} is only discharged by $G_m V_{out}$. The capacitor current can be written in terms of the derivative of its voltage:

$$\frac{dV_{C_{rip}}}{dt} = \begin{cases} \frac{G_m}{C_{rip}}(\frac{V_{in}}{4} - V_{out}) & \text{in } \varphi_{odd}, \\ -\frac{G_m V_{out}}{C_{rip}} & \text{in } \varphi_{even}. \end{cases} \tag{5}$$

The parallel resistor, R_{par}, removes any DC component caused by transients so that $V_{C_{rip}}$ and $I_{L,AC}$ have the same DC level, which is zero. Comparing (4) and (5) yields

$$V_{C_{rip}} = \frac{G_m L}{C_{rip}} \cdot I_{L,AC}, \tag{6}$$

showing that $V_{C_{rip}}$ can approximate the term $k_i \cdot I_{L,AC}$ in (2).

However, all previous analysis in this section is built on the assumption that the flying capacitors are balanced. To actually achieve balance, an additional sliding mode is required [25]. In MRIC, another reference voltage, $V_{ref,bal}$, is generated to compare against the feedback signal with hysteresis, $V_{fb,hst}$, shown in Fig. 7 with exemplary waveform.

In φ_{even}, the reset switch is turned on, forcing $V_{ref,bal}$ to be equal to V_{ref}. In φ_{odd}, the reset switch is turned off, and the capacitor C_{bal} is charged by $g_m(V_x - V_{in}/4)$. Using its Volt-Amp relationship, it can be derived that:

$$V_{ref,bal}(t) = \begin{cases} k_b \cdot \int_0^t (V_x - \frac{V_{in}}{4})\, dt + V_{ref} & \text{in } \varphi_{odd}, \\ V_{ref} & \text{in } \varphi_{even}, \end{cases} \tag{7}$$

where t is the time index with respect to the beginning of the corresponding state; $k_b = g_m/C_{bal}$ is the balancing injection gain. Though this mathematical expression may seem abstract, it represents the average V_x level in φ_{odd}, and thus contains information of flying capacitor voltage balance.

As shown in the exemplary waveform in Fig. 7, the average V_x is higher than the balanced case ($V_{in}/4$) in φ_1; the integral

pushes up $V_{ref,bal}$, ending up with a voltage increment before reset. In φ_3, the average V_x is equal to $V_{in}/4$; the integral first rises and then falls back to zero at the end of the state. In φ_5, the average V_x is lower than $V_{in}/4$; the integral now pulls down $V_{ref,bal}$ to intersect earlier with $V_{fb,hst}$. In this scenario, the controller terminates the current switching state at the crossing point of $V_{fb,hst}$ and $V_{ref,bal}$, and initiate the next switching state.

The overall effect of such control action is that the duration of an odd state is reduced if the average V_x is lower than $V_{in}/4$. A lower V_x can result from a flying capacitor at low voltage being discharged, or a flying capacitor at high voltage being charged. In either case, this charge transfer is undesired and reducing the state duration applies a negative feedback on the flying capacitor voltage deviation, leading it back to balance. The stability is proved in the Appendix.

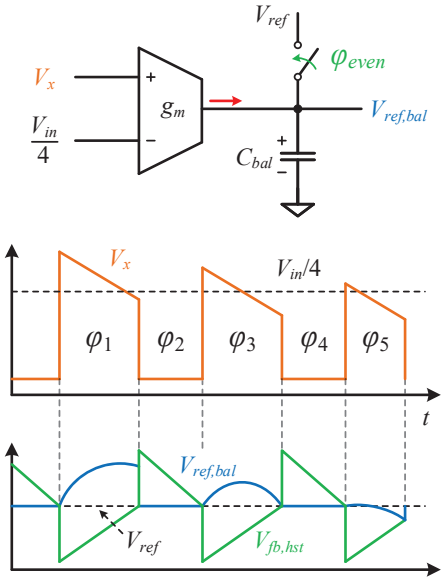

Fig. 7. Reference signal generation: $V_{ref,bal}$ is compared against $V_{fb,hst}$.

This balancing sliding mode combined with the previous ripple injection sliding mode, shown in Fig. 5 (b), forms the MRIC algorithm which achievs both output voltage regulation and flying capacitor voltage balance for hybrid SC converters.

B. Startup Detection and Phase Skipping

For USB power delivery, it is important for the converter to withstand fast line transients, which can result from hard-switching the power supply (i.e. hard-connecting a USB power cable). This is especially challenging for hybrid SC converters, as the flying capacitor voltages should be kept proportional to the input voltage to avoid switch overstress. Although a soft startup method can be used to slowly ramp up V_{in} [34], [35], it increases the physical size and significantly delays the startup response. It is desired to achieve fast regulation of flying capacitor voltages, so that the converter can safely startup in the worst case scenario.

In the cascaded hybrid topology of this work (shown in Fig. 3), balancing dynamics of the first stage flying capacitors, C_α and C_β, are fast due to interleaving (discussed in section II). However, balancing of the second stage flying capacitor, C_2, is relatively slow, because its charging and discharging current links the inductor even in transients. During converter startup, the MRIC algorithm would shorten the discharging state of C_2 to raise its voltage, but its voltage can rise faster if the discharging states are completely eliminated, motivating the phase skipping technique. Among the 8 switching states, C_2 is discharged in φ_3 and φ_7 (refer to Fig. 4), thus they are skipped during startup, accelerating the balancing dynamics. It should be noticed that when φ_3 and φ_7 are skipped, φ_2 and φ_4, φ_6 and φ_8 are also merged, respectively, leaving only 4 switching states during startup: φ_1, φ_2, φ_5, and φ_6.

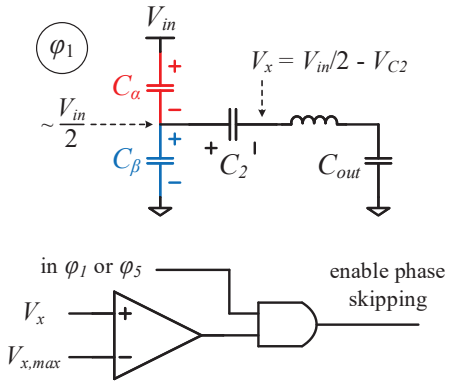

Fig. 8. Detecting startup during φ_1 and φ_5: if V_x is significantly higher than $V_{in}/4$, phase skipping is enabled.

Startup is detected by comparing the switching node voltage, V_x, with a high threshold, $V_{x,max}$, in state φ_1 and φ_5, as shown in Fig. 8. Due to symmetry of the first stage and the relationship in (1), voltage on C_α and C_β are roughly $V_{in}/2$ even during transients. Therefore, in state φ_1 and φ_5, the switching node voltage, V_x, is given by

$$V_x = \frac{V_{in}}{2} - V_{C_2}. \tag{8}$$

The high threshold, $V_{x,max}$, is proportional to V_{in} but with a coefficient slightly larger than $1/4$ so that V_x never exceeds

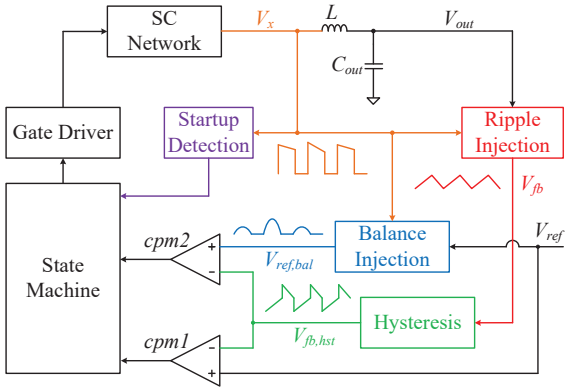

Fig. 9. Simplified control diagram of the MRIC algorithm, with additional startup detection and phase skipping technique.

$V_{x,max}$ in balanced state. If V_{C_2} is significantly lower than its nominal value ($V_{in}/4$), V_x would be higher than $V_{x,max}$ in φ_1 and φ_5, triggering phase skipping and the converter enters startup mode. If startup is no longer detected, the converter automatically enters regular mode in the next period.

After including the startup detection and phase skipping technique, the top-level control diagram is illustrated in Fig. 9. The switching node voltage indicates whether the converter is in φ_{odd} or φ_{even}, which is used to emulate and inject $I_{L,AC}$ to V_{out}. The feedback signal generated from ripple injection, V_{fb}, is added hysteresis to form $V_{fb,hst}$, which is then compared to the reference voltage, V_{ref}, by *cpm1* to maintain output voltage regulation. In another sliding mode, V_{ref} is injected with balancing information contained in V_x to generate $V_{ref,bal}$. A second comparator, *cmp2*, compares $V_{fb,hst}$ with $V_{ref,bal}$, and its output triggers the termination of odd switching states that has a low V_x, forcing the flying capacitors to balance. The switching node voltage, V_x, is also used to detect startup or extreme line transients. Under these scenarios, the state machine is modified to skip φ_3 and φ_7 to accelerate balancing dynamics of C_2.

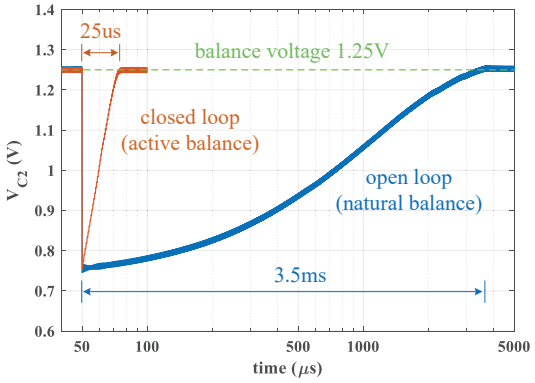

Fig. 10. Simulation results of open-loop and closed-loop balancing dynamics.

To illustrate the effectiveness of the control scheme, simulation is conducted to compare closed-loop operation against open-loop operation, where the voltage on flying capacitor C_2 is weakly regulated by natural balance, as shown in Fig. 10. For the simulation setup, the converter is initially in balanced steady state. At a certain moment ($50\mu s$), a forced deviation ($-0.5V$) is applied to mimic disturbances (such as line/load transient, false switching, etc.). In open-loop operation, it takes $3.5ms$ for V_{C2} to return to balance; in closed-loop operation, V_{C2} recovers within $25\mu s$, which is over 100 times faster.

IV. Gate Driving and Circuit Implementation

In this work, all gate drivers including the bootstrap capacitors are fully integrated, eliminating the need for external gate driving supplies. Additionally, several design techniques are used to reduce the bootstrap capacitor area. This section first introduces the fully integrated gate driving strategy and then describes the circuit implementation of key blocks.

A. Fully Integrated Gate Driving

The first stage of the converter uses $5V$ power switches with a nominal V_{th} of $0.78V$. Considering the trade-off between conduction loss and switching loss, $2.4V$ driving voltage has best overall efficiency in simulation. In the prototype, they are driven at $V_{in}/2$ ($2.5V$) since the rail is easy to generate and close to optimum. The gate driving schematic of $M_{1\alpha}$, $M_{1\beta}$, $M_{4\alpha}$, and $M_{4\beta}$ is shown in Fig. 11. Switch $M_{1\alpha}$ and $M_{1\beta}$ are bootstrapped from V_{in} during their off state. When signal A goes high, $C_{BS,1\alpha}$ supplies charge to turn on $M_{1\alpha}$ while $C_{BS,1\beta}$ is charged to $V_{in}/2$ through $M_{BS,1\beta}$. When signal B goes high, $C_{BS,1\beta}$ supplies charge to turn on $M_{1\beta}$ while $C_{BS,1\alpha}$ is charged back to $V_{in}/2$ through $M_{BS,1\alpha}$.

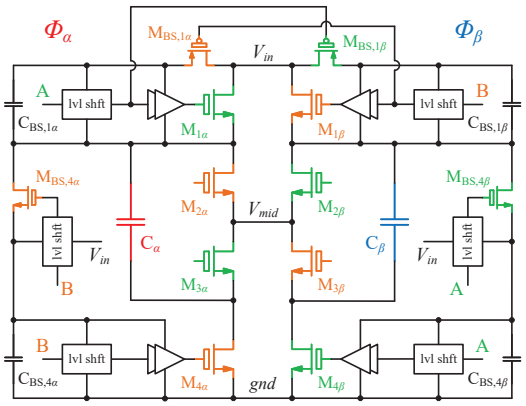

Fig. 11. The gate driving schematic of $M_{1\alpha}$, $M_{1\beta}$, $M_{4\alpha}$, and $M_{4\beta}$.

Different from the above case, the bootstrap capacitor of $M_{4\alpha}$ and $M_{4\beta}$ are charged when the corresponding power switch turns on, hereby referred to as synchronous bootstrap. For example, when signal A goes high, $C_{BS,4\beta}$ supplies charge to turn on $M_{4\beta}$, connecting the bottom plate of C_β to ground. Almost immediately after, C_β charges $C_{BS,4\beta}$ back to $V_{in}/2$ through $M_{BS,4\beta}$. Note that a N-channel device is used for the bootstrap switch, reducing the on resistance and accelerating the charge recovery of $C_{BS,4\beta}$. The symmetric circuitry in Φ_α operates similarly but 180° out of phase.

In the case of synchronous bootstrap, the bootstrap capacitor only needs to supply a small amount of initial charge before being charged back to its nominal voltage, as opposed to traditional bootstrapping where the bootstrap capacitor drives the power switch through charge sharing. Therefore, as long as the charge recovery process is fast, synchronous bootstrapping reduces the required bootstrap capacitance without the penalty of lower driving voltage. In this design, traditional bootstrap capacitors ($C_{BS,1\alpha}$, $C_{BS,1\beta}$) are $650pF$ each, implemented with MIM capacitors; the synchronous bootstrap capacitors ($C_{BS,4\alpha}$, $C_{BS,4\beta}$) are $310pF$ (52% smaller) each. Because the bottom plates are always grounded, they are implemented with stacked MIM and MOS capacitors for higher density.

Fig. 12 shows the gate driving schematic of $M_{2\alpha}$, $M_{2\beta}$, $M_{3\alpha}$, and $M_{3\beta}$ with exemplary waveform of gate signals and bootstrap capacitor voltage. For switch $M_{3\alpha}$ and $M_{3\beta}$, their source terminal is connected to the bottom plate of flying capacitor C_α and C_β, respectively. Therefore, the gate drivers are directly supplied by the corresponding flying capacitor. Switch $M_{2\alpha}$ and $M_{2\beta}$ are synchronously bootstrapped. They have a common source node (V_{mid}) and are never turned on

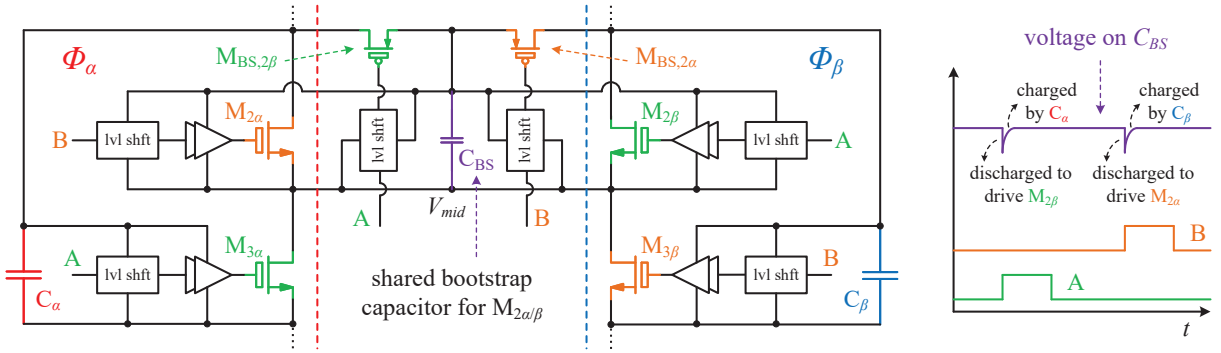

Fig. 12. The gate driving schematic of $M_{2\alpha}$, $M_{2\beta}$, $M_{3\alpha}$, and $M_{3\beta}$ with exemplary waveform of logic levels and bootstrap capacitor voltage.

at the same time, which allows the use of a shared bootstrap capacitor. When signal A goes high, C_{BS} supplies the initial charge to turn on $M_{2\beta}$ before being charged back to $V_{in}/2$ by C_α through $M_{BS,2\beta}$, as shown in the exemplary waveform. When signal B goes high, C_{BS} supplies charge to turn on $M_{2\alpha}$ and is charged back to $V_{in}/2$ by C_β. In this design, C_{BS} is implemented with MIM capacitor and has a value of $260pF$, which is about the same capacitance as $C_{BS,4\alpha}$ and $C_{BS,4\beta}$, but it supplies the drivers for both $M_{2\alpha}$ and $M_{2\beta}$.

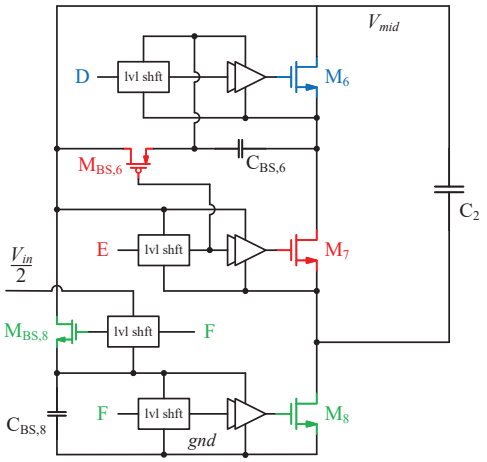

Fig. 13. The gate driving schematic of M_6, M_7, and M_8.

The second stage of the converter uses 1.8V power switches with a nominal V_{th} of 0.33V. They are all driven at $V_{in}/4$ (1.25V). Fig. 13 shows the gate driving schematic of M_6, M_7, and M_8. The gate driver of switch M_6 is supplied by the bootstrap capacitor $C_{BS,6}$. Switch M_7 have its source terminal connected to the bottom plate of flying capacitor C_2, thus can be directly driven by C_2. When M_7 turns on, C_2 also charges the bootstrap capacitor $C_{BS,6}$ through $M_{BS,6}$. Switch M_8 is synchronously bootstrapped from C_2, and the $V_{in}/2$ voltage rail required to turn on the bootstrap switch ($M_{BS,8}$) is provided by $C_{BS,4\beta}$ in the first stage (refer to Fig. 11).

B. Circuit Implementation of Key Blocks

In Fig. 9, the hysteresis block adds hysteresis to V_{fb} to generate $V_{fb,hst}$. Its circuit implementation is shown in Fig. 14. The bias current, I_{bias}, is mirrored to a resistor branch to create the desired hysteresis window:

$$\Delta V = I_{bias} \cdot R_{hst}. \tag{9}$$

When the converter is in φ_{odd}, V_{fb} is rising and the lower transmission gate turns on, pulling down V_{fb} by ΔV. When the converter is in φ_{even}, V_{fb} is falling and the upper transmission gate turns on, pushing up V_{fb} by ΔV.

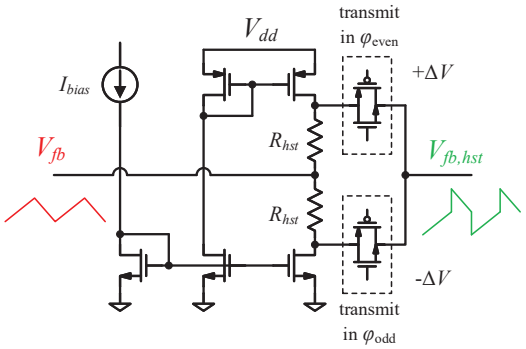

Fig. 14. The circuit implementation of the hysteresis block.

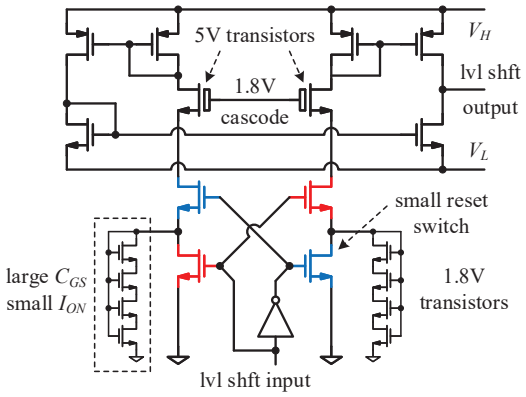

Fig. 15. The level shifter circuit in the second stage of the converter.

Fig. 15 shows the level shifter circuit in the second stage of the converter. This design uses transistors with isolated wells to avoid impacts of body effect. When the level shifter input

goes high (red switches turn on), a current pulse is generated on the right branch to charge the large C_{GS} of a long-channel diode-connected stack, which afterwards provides a small hold-state current. The current pulse is amplified and rectified in the linear OTA, which pulls the level shifter output to V_H. Meanwhile, the C_{GS} of the diode-connected stack on the left branch is discharged by the reset switch. When the level shifter input goes low (blue switches turn on), the current pulse on the left branch is amplified by the OTA and the level shifter output is pulled down to V_L, while the reset switch on the right branch discharges the diode-connected stack. The level shifter in the first stage of the converter uses a similar cascode-OTA structure; the only difference is that all transistors between the V_L and V_H rails are 5V devices.

V. Test Results and Performance Summary

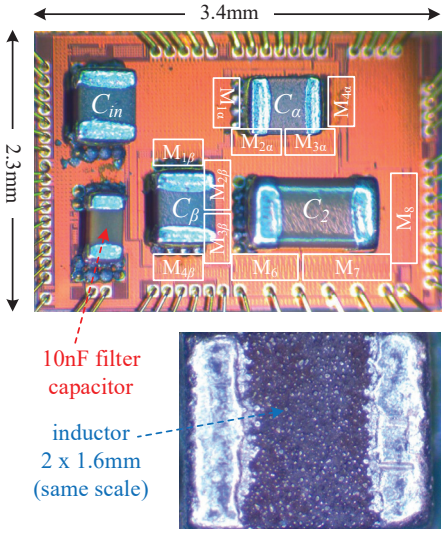

Fig. 16. The annotated micrograph of the chip and die-attached capacitors, along with the off-package inductor.

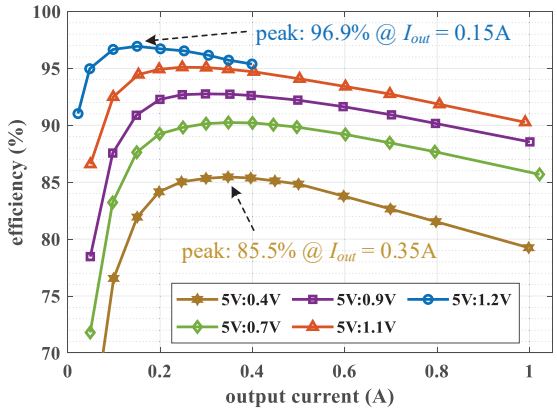

Fig. 17. The measured efficiency versus output current with $V_{in} = 5V$.

The converter prototype was fabricated in a $0.18\mu m$ bulk CMOS process, with a total die area of $7.82mm^2$. Fig. 16 shows the annotated micrograph of the chip and die-attached

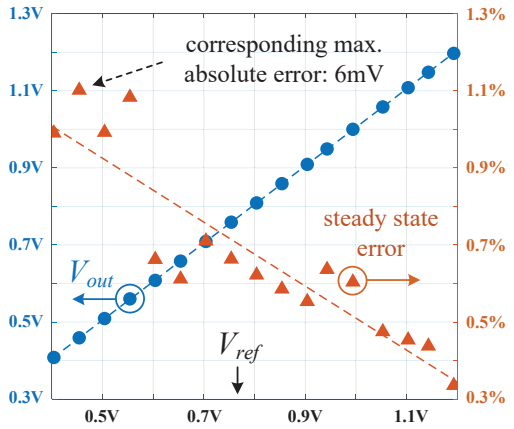

Fig. 18. The measured V_{out} and its steady state error versus output voltage.

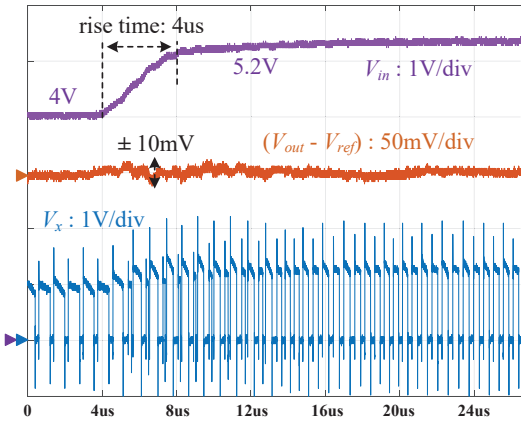

Fig. 19. The line transient response with V_{in} changes from $4V$ to $5.2V$.

capacitors, along with the off-package inductor. Capacitor C_{in}, C_α, and C_β have a nominal value of $4.7\mu F$; capacitance of C_2 is $10\mu F$. The inductor has a nominal value of $240nH$ with a DC resistance of $13m\Omega$.

Fig. 17 shows the measured efficiency versus output current for multiple conversion ratios. The overall peak efficiency of 96.9% is achieved at $0.15A$ output with a 5V:1.2V step down. At $5V$ input, the highest achievable V_{out} is $1.25V$ ($V_{in}/4$) at empty load. For 5V:1.2V conversion, regulation is lost when the load current exceeds 0.4A, thus higher load current is not recorded in this configuration. The converter maintains up to 85.5% efficiency for 5V:0.4V conversion.

Fig. 18 and 19 show the measured steady state error (SSE) and line transient response, respectively. At $5V$ input, V_{out} tracks V_{ref} with less than 1.1% SSE for the entire output range of 0.4-$1.2V$. For the line transient test, V_{in} rises from $4V$ to $5.2V$ with less than $10mV$ output variation. Settling time of the flying capacitor voltage is in the order of $10\mu s$.

Full-range (maximum I_{out} step size) load transient is often challenging for voltage regulators, due to the excessive V_{out} deviation it induces. Fig. 20 shows the replotted oscilloscope measurement of the full-range load transient response. The rise and fall time are less than $1\mu s$, and the measured undershoot and overshoot are $32mV$ and $36mV$, respectively. It can be

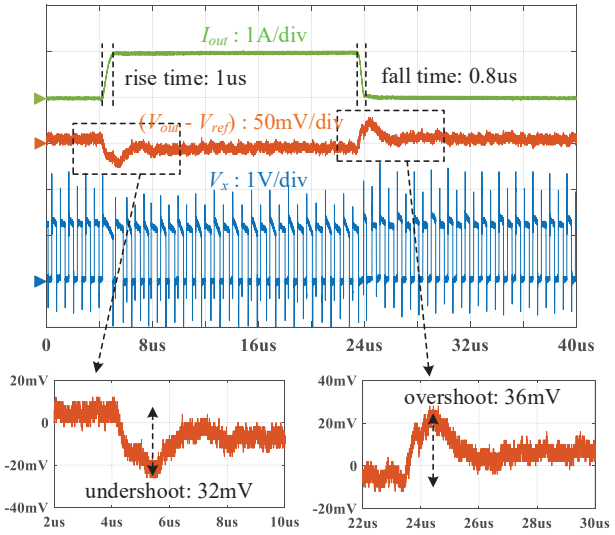

Fig. 20. Replotted oscilloscope measurement of the full-range load transient.

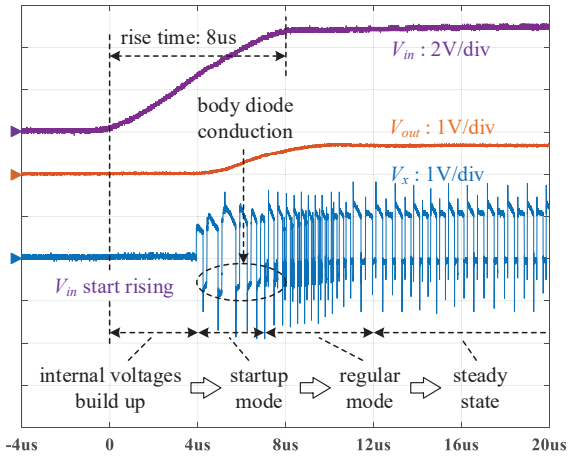

Fig. 21. The converter startup characteristics with V_{in} rising from 0 to $5V$ in $8\mu s$ ($0.6V/\mu s$ slew rate).

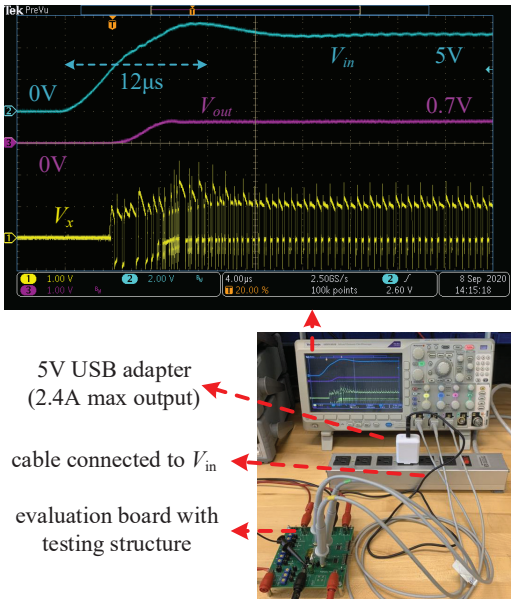

Fig. 22. Testing the startup with V_{in} directly connected to a USB adapter.

observed from the V_x waveform that flying capacitor balance is maintained, even when $I_{out} = 0$.

Fig. 21 shows converter startup characteristics with V_{in} rising from 0 to $5V$ in $8\mu s$ ($0.62V/\mu s$ slew rate). Different stages in the startup process are seen in the V_x waveform. During 0-4μs, V_{in} is rising but no switching event happens as the internal nodes and capacitors are charging up. In 4-7μs, the converter is in the startup mode since no lower pulse of V_x (i.e., φ_3 and φ_7 where C_2 is connected between V_x and ground) is observed, meaning these two states are skipped. As gate drivers in the second stage wait for C_2 to charge, switch M_7 and M_8 are subject to body-diode conduction, leading to temporarily negative V_x. In 7-12μs, C_2 is charged sufficiently close to its nominal voltage and the converter is in the regular mode, where the control loop is regulating both the output voltage and the flying capacitor voltage. The converter enters its steady state at 12μs.

Fig. 22 shows the worst case startup of the converter in practice. The USB cable, which connects to V_{in}, is directly plugged into the USB adapter. The V_{in} waveform has an overshoot due to cable inductance, but the converter still safely starts up then maintains balance and regulation in steady state.

Table I summarizes the converter performance and compares selected key features with similar prior works. This design achieves higher efficiency at comparable conversion ratios, although showing lower power density against designs in deep-submicron processes (we have summed up die and passive component areas to have a more fair comparison as opposed to not counting the area of the die-attached passives). The output voltage undershoot is also smaller under similar load current step. The major advantage here is the startup time that is over 100 times faster than the closest prior art.

VI. Conclusion

This work presented a cascaded hybrid switched capacitor converter with fast startup speed in 0.18μm CMOS process. The topology has the advantage of accelerating the balancing dynamics of flying capacitors and reducing the input bypass requirement. With fully integrated gate drivers, the converter does not need any external gate driving supply. The prototype achieves 96.9% peak efficiency for 5V:1.2V conversion, less than 36mV overshoot and undershoot for 1A/μs load transient, and a startup time that is in the order of 10μs. Tested in a practical scenario, this hybrid SC converter can withstand the worst case startup in the targeted application.

Appendix
Stability of the Balancing Sliding Mode

At the beginning of an odd state, assuming that the switching node voltage, V_x, is slightly lower than the balanced value, different control actions may be performed to determine the state duration, as shown in Fig. 23.

In case (a), the switching state is terminated when $V_{fb,hst}$ reaches V_{ref}, meaning that the state duration is not changed

TABLE I
THE PERFORMANCE SUMMARY AND COMPARISON WITH SIMILAR PRIOR ART.

	[20]	[36]◇	[21]	[37]	[25]	**This Work**
Topology	Hybrid Dickson	3-level Buck	4-level FCML	3-level Buck-Boost	5-level FCML	Hybrid Cascaded SC
Process	65nm	28nm	22nm	90nm	180nm	180nm
V_{in}	3-4.5V	3-4.5V	3.7-5V	2.5-5V	4-5.5V	4-6V
V_{out}	0.3-1V	0.8-1.45V	0.8-1.8V	0.4-9V	0.4-1.2V	0.4-1.2V
power switch count	8×2.5V	4	12×1.2V	5	8×1.8V	8×5V+3×1.8V
number of sw. states	6	4	6	4 or 6	8	8
inductor f_{sw}	1MHz	3MHz	5MHz	up to 3MHz	not reported	1.4-1.6MHz
$I_{out,max}$ (@ V_{out})	1.05A (0.95V)	1A (1.15V)	10A (1.8V)	1A (4.5V)	1.4A (1V)	1A (1.1V)
Control	integrated	integrated	off-chip	integrated	integrated	integrated
Flying capacitor	3x22μF	on-chip	2x13.2μF	10μF	3x4.7μF	2x4.7μF+10μF
Output capacitor	22μF	2μF	18μF	10μF	10μF	14.4μF
Inductor	470nH	2.2μH	10nH	2.2μH	240nH	240nH
Max. power density†	0.1W/mm^2	N/A	0.95W/mm^2	N/A	0.11W/mm^2	0.1W/mm^2
Max. Eff. (@ VCR*)	94.2% (4.4)	89.6% (3.8)	93.8% (2.8)	96.8% (1.2)	92.4% (4.6)	96.9% (4.2)
Max. VCR* (@ Eff.)	8.2 (86.5%)	3.8 (89.6%)	6.3 (85.8%)	12.5 (N/A)	13.8 (80.2%)	12.5 (85.5%)
I_{out} trans. step	N/A	0.35A→0.1A	0→6A	N/A	0→1A	0→1A
V_{out} over/undershoot	N/A	17mV	150mV	N/A	58mV	32mV
V_{in} startup step	N/A	N/A	0→5V	N/A	0→5.5V	0→5V
Duration (slew rate)	N/A	N/A	7ms (0.72V/ms)	N/A	2ms (2.8V/ms)	8μs (625V/ms)

*VCR refers to the step-down voltage conversion ratio, V_{in}/V_{out}.
†The total area includes active die, flying capacitors and inductor. In this work, the area of die-attached passives are also included.
◇V_{out} assumed as the average of multiple output.

by the balancing sliding mode. In case (b), the switching state is terminated when $V_{fb,hst}$ reaches $V_{ref,bal}$, which is the same algorithm as MRIC. In case (c), the switching state is terminated when $V_{ref,bal}$ reaches V_{ref}, meaning that the state duration is further reduced compared to MRIC. In all three cases, the imbalance error is given by the difference between V_x and its balanced value, with the initial and final error in that state denoted as e_i and e_f.

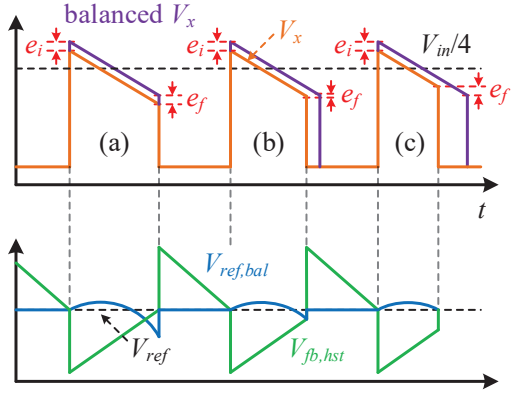

Fig. 23. Generating another reference voltage, $V_{ref,bal}$, to compare against the feedback signal with hysteresis, $V_{fb,hst}$.

In case (a), the state duration is not changed by the balancing sliding mode, thus the imbalance error is also unchanged from the beginning to the end of the state, and the error gain, $k_{e,a}$, is given by

$$k_{e,a} = \frac{e_{f,a}}{e_{i,a}} = 1. \tag{10}$$

in case (c), both V_x and its balanced value are symmetric with respect to $V_{in}/4$, as shown in Fig. 23. Therefore, $V_{f,c} = -V_{i,c}$, and the error gain is given by

$$k_{e,c} = \frac{e_{f,c}}{e_{i,c}} = -1. \tag{11}$$

in case (b), the state duration is between the state duration in case (a) and (c), and so is the error gain:

$$-1 < k_{e,b} < 1. \tag{12}$$

Therefore, in MRIC, which is the same as case (b), $|e_{f,b}| < |e_{i,b}|$, meaning the absolute imbalance error at the end of the state is always smaller than at the beginning of the state. Because the imbalance error is always decreasing, in the limit as time or the number of switching cycles goes to infinity, the error must converge to zero (similar to having discrete-time eigenvalues within the unit circle), thus stability is guaranteed.

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