Bottom-up Nanoscale Patterning and Selective Deposition on Silicon Nanowires

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ABSTRACT

We demonstrate a bottom-up process for programming the deposition of coaxial thin films aligned to the underlying dopant profile of semiconductor nanowires. Our process synergistically combines three distinct methods – vapor-liquid-solid (VLS) nanowire growth, selective coaxial lithography via etching of surfaces (SCALES), and area-selective atomic layer deposition (AS-ALD) – into a cohesive whole. Here, we study ZrO_2 on Si nanowires as a model system. Si nanowires are first grown with an axially modulated n-Si/i-Si dopant profile. SCALES then yields coaxial poly(methyl methacrylate) (PMMA) masks on the n-Si regions. Subsequent AS-ALD of ZrO_2 occurs on the exposed i-Si regions and not on those masked by PMMA. We show the spatial relationship between nanowire dopant profile, PMMA masks, and ZrO_2 films, confirming the programmability of the process. The nanoscale resolution of our process coupled with the plethora of available AS-ALD chemistries promises a range of future opportunities to generate structurally complex nanoscale materials and electronic devices using entirely bottom-up methods.

INTRODUCTION

The bottom-up synthesis of complex nanoscale materials and functional devices requires new patterning techniques that are not only compatible with the structure and dimensionality of the object to be patterned, but also offer a suitable marriage of resolution and programmability. Nanoscale patterning methods commonly deployed for 2-dimensional (2-D) surfaces, such as photo or e-beam lithography, are user-definable and offer excellent resolution.[1-4] However, the patterning of 3-dimensional (3-D) nanoscale objects introduces additional challenges. Techniques must be compatible with objects oriented in most any direction and exhibiting local curvature, in addition to offering programmability and nanoscale resolution.

Several examples highlight recent progress toward a robust ability to pattern 3-D nanoscale objects, and to leverage that pattern to direct subsequent deposition. Ozel *et al* demonstrated the fabrication of complex nanostructures in anodized alumina oxide (AAO) membranes using a combination of electrochemical deposition and selective etching.[5] The technique is amenable to any material that can be electrodeposited, including semiconductors (e.g., CdSe), metals (e.g., Au), or oxides (e.g., MnO_2). The resulting nanostructures are programmable in the axial direction by controlling the sequencing and deposition time of each segment. Phase separation of polymer-coated nanostructures can also be used to impart nanoscale patterns.[6, 7] Wang *et al* show that thermal treatment of polystyrene-block-poly(acrylic acid)-coated Au nanorod dispersions can result in a variety of surface structures that serve as masks for subsequent metal (e.g., Ag, Pd) deposition.[8] The mask structure is tunable through the polymer's structure and interactions with the underlying nanorod. To date, no similarly powerful techniques exist for nanopatterning the single crystalline, high mobility semiconductors that are the basis of high performance nanoelectronic devices.

Here, we demonstrate a bottom-up process for programming the deposition of nanoscale thin films on semiconductor nanowires. As illustrated in Figure 1, our approach combines bottom-up vapor-liquid-solid (VLS) nanowire growth,[9-14] selective coaxial lithography via etching of surfaces (SCALES),[15] and area-selective atomic layer deposition (AS-ALD). The resulting structure is that of a Si "proto-transistor," containing a source, channel, and drain as well as a model ZrO_2 gate dielectric aligned to the channel. Detailed experimental methods are available in the Supporting Information. We begin with the VLS synthesis of Si nanowires that alternate between nominally intrinsic (i-Si) and phosphorous-doped (n-Si) segments. Segment, and ultimately coaxial mask and thin film, dimensions are programmable via Si nanowire growth time and conditions. We next use SCALES[15] to create coaxial poly(methyl methacrylate) (PMMA) masks on the n-Si regions. A blanket poly(methyl methacrylate) (PMMA) brush is initially grown from the entire Si nanowire surface using atom transfer radical polymerization (ATRP)[16-18] (Supporting Information, Figure S1). We then selectively remove the polymer from i-Si regions but not n-Si regions using aqueous potassium hydroxide (KOH).[10, 19-22] In this step, KOH diffuses through the PMMA mask and selectively etches the underlying i-Si segments, which releases the tethered PMMA chains into solution. Notably, relative to our initial work on Si/Ge nanowires,[15] the n-Si/i-Si nanowires require distinct strategies for attaching the polymerization initiator and selectively etching the nanowire. We then use the SCALES mask to direct the AS-ALD of ZrO_2 onto i-Si segments.

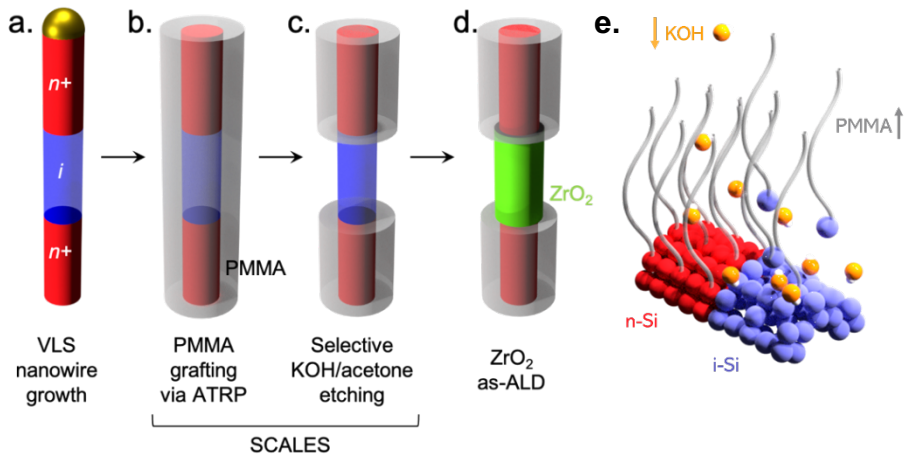

Figure 1. Overall process flow. *(a) VLS growth of Si nanowires with axially programmed phosphorus dopant profiles, (b) surface-initiated polymerization of PMMA from both i-Si and n-Si segments, (c) selective etching to remove PMMA from the i-Si segments, (d) AS-ALD of ZrO_2 on exposed i-Si segments. (e) Selective etching mechanism (transition from step b to c)*

Our approach enables the axial programming of patterns with nanoscale resolution on semiconductor nanowires. The single-crystallinity of VLS-grown semiconductor nanowires,[23, 24] in addition to the alignment of the coaxial masks and thin films to the nanowire dopant profile, promises to be useful for the fully bottom-up construction of nanoelectronic devices, such as field effect transistors. The availability of myriad VLS-grown nanowires[25-27] and AS-ALD chemistries[28-30] also offers versatility and extensibility. Moreover, the bottom-up nature of all process steps – VLS nanowire growth, SCALES, and selective deposition – also ensures compatibility with the 3-D nature of the nanowires themselves as well as any scalable nanowire manufacturing technique with which they may be produced (e.g., Geode Process,[31] Aerotaxy[32]).

RESULTS AND DISCUSSION

The entire sequence of VLS growth, SCALES patterning, and AS-ALD is shown in Figure 2. Si nanowires are grown with n-Si segments of a fixed length (~200 nm) and i-Si segments of different lengths (~200 and ~500 nm). Figure 2(a) shows a representative as-grown Si nanowire following a short KOH etch, confirming these segment lengths. Figure 2(b) shows a blanket PMMA film (false-colored in yellow) on an as-grown Si nanowire after ATRP. The PMMA thickness depends on the type of segment to which it is attached: i-Si and n-Si regions exhibit a thickness of ~20 and ~30 nm, respectively. Since the subsequent selective etching process relies on the diffusion of the etchant through the PMMA, the polymer film thickness was intentionally kept low. X-ray photoelectron spectroscopy (XPS) spectra of such a film on a Si wafer are consistent with PMMA (Supporting Information, Figure S2).

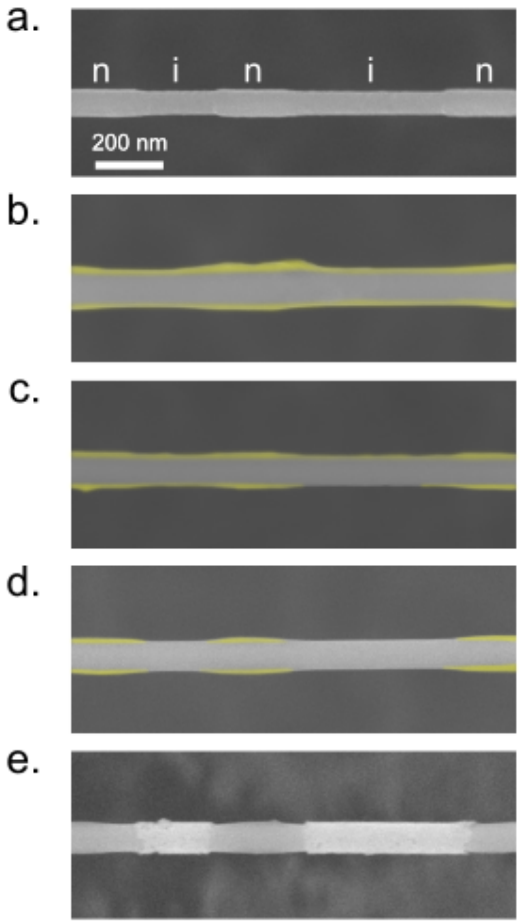

Figure 2. Demonstration of complete VLS growth, SCALES, and AS-ALD sequence. *(a) VLS-grown Si nanowire following a brief KOH etch to reveal the phosphorus dopant profile. (b) As-grown Si nanowire with a blanket coating of PMMA following ATRP. PMMA is false colored in yellow for clarity. (c) SCALES-patterned Si nanowire following cyclic etching with KOH/acetone to remove PMMA from the i-Si segments. (d) SCALES-patterned Si nanowire after a final KOH rinse to remove residual PMMA on the i-Si segments. (e) Si nanowire after AS-ALD of ZrO_2 onto the exposed i-Si segments. The magnification of all images is the same.*

Next, we apply a cyclic etch procedure, switching between aqueous KOH solution and acetone, to selectively remove PMMA from the i-Si segments. Figure 2(c) shows the resulting PMMA mask after 3 KOH/acetone cycles. We find that continuous KOH etching does not selectively remove the PMMA, even with a final acetone rinse. We suspect this behavior results because water is a poor solvent for PMMA[33] and the addition of acetone helps solvate both tethered and released PMMA chains, thereby facilitating etching. Notably, the n-Si segments also show some PMMA loss, albeit less than that on the i-Si segments. A final KOH rinse (without acetone) removes remaining PMMA on the i-Si segments, as displayed in Figure 2(d), without additional removal of PMMA on the n-Si segments.

The SCALES-patterned nanowires are then used as substrates for AS-ALD. AS-ALD is extensively used to direct thin film deposition on 2-D substrates, where selectively attached or top-down patterned self-assembled monolayers or polymers are the deposition-directing agents.[34-37] Figure 2(e) shows ZrO_2 thin films solely on the i-Si segments (also see Supporting Information, Figure S3). The ZrO_2 appears bright due to its large atomic number (40) relative to Si (14) or C (6). Despite modest removal of PMMA from the n-Si segments, the remaining film is still able to

resist ZrO_2 ALD. This result is consistent with previous studies, which show that the steric hinderance of the tetrakis groups of the Zr precursor minimizes interactions with PMMA.[38]

We now investigate the resulting coaxial thin films in more detail, confirming the programmability of our process and presence of ZrO_2. Figure 3(a) shows SEM images of Si nanowires with constant and different length i-Si segments following KOH etching without PMMA to reveal the i-Si and n-Si segments. The presence of a bright film following AS-ALD ZrO_2 only on the i-Si segments in Figure 3(b), as expected from the underlying dopant encoding shows the intended programmability. Zr(Lα) and O(Kα) energy dispersive X-ray (EDX) spectroscopy maps in Figure 3(c) and 3(d), respectively, confirm the presence of both Zr and O, which is consistent with the presence of ZrO_2. While Zr is only observable above the noise on the i-Si segments, O is observed on both the i-Si and n-Si segments. We attribute this observation to the presence of some native oxide on the n-Si surface. Despite demonstrating the programmability of our process, there is clearly room to improve the morphology, continuity, and edge abruptness of the coaxial thin films. We expect that this will be possible with a combination of increasingly abrupt dopant profiles in the Si nanowires, more complete PMMA removal upon KOH etching, and pre-ALD surface cleaning. These improvements will also facilitate the clean semiconductor-thin film interfaces needed for high performance nanoelectronic devices[39, 40].

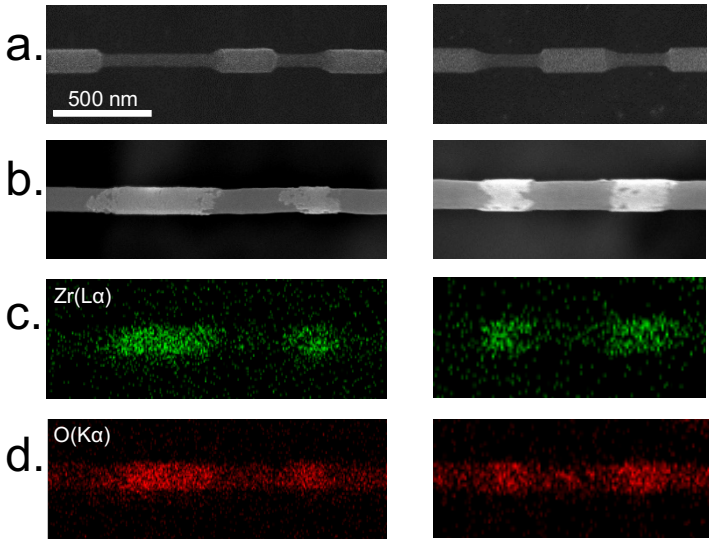

Figure 3. Demonstration of pattern programming and EDX analysis of AS-ALD thin film. *(a) SEM images of as-grown Si nanowires following KOH etch to confirm dopant profile. (b) SEM images of Si nanowires following SCALES patterning and 180 cycles of ZrO_2 ALD. (c) EDX map of Zr(Lα) showing the presence of Zr, as expected for ZrO_2, on the i-Si segments. Zr cannot be observed above the noise on the n-Si segments. (d) EDX map of O(Kα) showing a higher concentration of O on the i-Si, as expected for ZrO_2. The presence of some O on n-Si segments is attributed to native oxide. The magnification of all images is the same.*

The ultimate resolution of our patterning and deposition approach will depend on multiple factors, including abruptness of nanowire dopant profile, etch selectivity, and PMMA thickness. We begin to understand these factors, as shown in Figure 4, by comparing the length of as-grown i-Si segments after KOH etching, $L_{encoded}$, relative to the length of the regions exposed following PMMA removal, $L_{pattern}$. An ideal process would result in an $L_{encoded} = L_{pattern}$ line, as indicated by the dotted line. However, we find that PMMA removal is always less than the as-grown i-Si

segment length determined via selective KOH etching. We hypothesize that the finite thickness of the polymer means that chains near the i-Si/n-Si interface can collapse onto the i-Si regions and block AS-ALD.[41, 42]

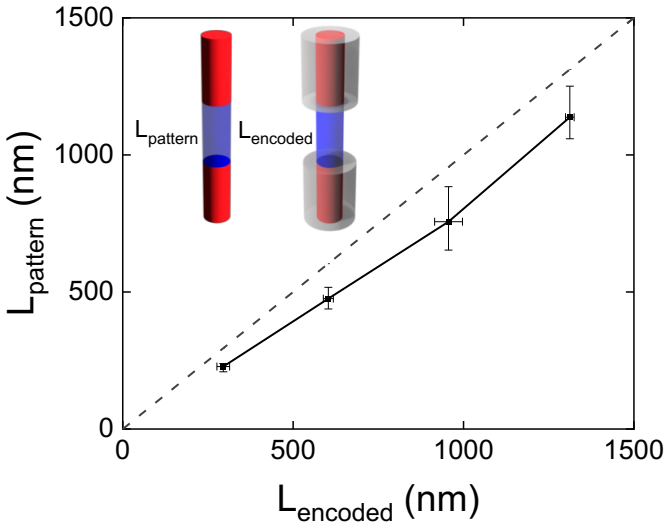

Figure 4. *Comparison of as-grown i-Si segment length ($L_{encoded}$) and length of segment exposed following PMMA removal ($L_{pattern}$).*

CONCLUSION

In summary, we demonstrate a process to apply coaxial thin films to Si nanowires using a combination of VLS growth, SCALES patterning, and AS-ALD. Our approach offers nanoscale resolution and is programmable via doping during VLS growth. It is versatile and extensible due to the variety of available VLS growth, selective etch, and AS-ALD chemistries. While feature sizes of ~200 nm are demonstrated, we expect that feature sizes of tens of nanometers are likely with careful control of nanowire growth, polymer chemistry, and polymer thickness. We use KOH to selectively remove PMMA from i-Si segments but note that an inverse process using HF to selectively remove PMMA from n-Si segments may also be possible. On-going work in our

laboratory is focused on understanding the intimate interplay between nanowire growth, nanowire surface structure and chemistry, polymer chemistry and thickness, selective etching, and AS-ALD. Finally, this work is an important step toward the entirely bottom-up fabrication of nanoelectronic devices.

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CONFLICT OF INTEREST

The authors declare no conflict of interest.

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SUPPORTING INFORMATION DESCRIPTION

Supporting information is available online at the Nanotechnology publications website. The following additional figures and details are available as referenced in the main text: experimental methods, figures S1-S3.

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SYNOPSIS TOC