Bottom-Up Fabrication and Characterization of a Self-Aligned Gate Stack for Electronics Applications

Amy C. Brummer[1], Amar T. Mohabir[2], Daniel Aziz[2], Michael A. Filler[2], Eric M. Vogel[1]

Georgia Institute of Technology: School of Materials Science and Engineering[1], School of Chemical & Biomolecular Engineering[2]

Abstract: A metal-oxide-semiconductor (MOS) gate stack that is self-aligned with the underlying silicon doping profile using a bottom-up process is demonstrated. We combine a new bottom-up patterning technique with atomic layer deposition (ALD) to selectively deposit a platinum-hafnium dioxide-silicon MOS gate stack. A poly(methyl methacrylate) (PMMA) brush is blanket grown from a Si(100) surface and selectively removed from the lightly-doped (~10^{18} cm^{-3}) regions using a doping-selective KOH etch. The PMMA brush that remains on the heavily-doped (~10^{20} cm^{-3}) regions effectively blocks the ALD of both HfO_2 and platinum. MOS capacitors exhibit promising capacitance-voltage characteristics, with a HfO_2 dielectric constant of ~25 and an average interface state density of 2.1 x 10^{11} cm^{-2} following forming gas anneal.

Main Text:

The availability of fully bottom-up fabricated device structures, such as metal-oxide-semiconductor (MOS) capacitors, would be valuable for a variety of emerging device applications. For example, vertical nanowire transistors monolithically integrated into the back end of line (BEOL) are being considered to further increase device density in integrated circuits.[1] Fabrication of the gate stack on the vertical nanowire sidewall is no simple task, currently requiring photolithography and complex, multistep process flows.[2] However, the process could be simplified if a self-aligned gate stack could be achieved with a bottom-up approach. Flexible electronics offer a variety of new use cases but necessitate low-temperature processes since most flexible substrates

cannot withstand high temperatures and alternative patterning techniques that are more scalable than conventional photolithography.[3]

Atomic layer deposition (ALD) allows for the area-selective and low temperature deposition of thin films intimately aligned with compositional patterns of the underlying substrate, largely irrespective of the geometry. The most common techniques for area-selective ALD (AS-ALD) involve the use of self-assembled monolayers (SAMs)[4-11] or other polymeric materials[12-17] to mask the surface by preventing ALD precursors from chemisorbing. These techniques often require photolithography to pattern the surface modification layer[9,12-14] or use surfaces patterned with different materials[4,8,17,18] to apply the masking material selectively based on the underlying substrate. For example, a SAM can be assembled only on silicon dioxide (SiO_2) regions of a patterned silicon wafer, leaving hydrogen-terminated silicon exposed.[4] This allows for deposition of self-aligned features based on the underlying substrate but requires the underlying materials (silicon and SiO_2) to have significantly different properties.

There are a number of challenges associated with the AS-ALD of a high-performance MOS gate stack. For BEOL and flexible electronics, one needs low temperatures and AS-ALD is well suited in this regard.[19] However, a high-performance gate stack needs high-quality materials and low defect density interfaces. While there has been some electrical characterization of AS-ALD films in the literaure,[7,8,15,20] there have been relatively few AS-ALD studies for such applications. In many cases, a self-aligned gate stack also requires selective deposition on chemically similar materials with only variation in dopant concentration designating the pattern (e.g., source/channel/drain), which is currently difficult to achieve with AS-ALD.

In this work, we combine a new bottom-up patterning technique with AS-ALD to deposit hafnium dioxide (HfO_2) and platinum (Pt) thin films based on the local carrier concentration of a

Si wafer. The patterning technique is a derivative of selective co-axial lithography via etching of surfaces (SCALES),[21] which was originally demonstrated on cylindrical nanowires (hence co-axial) but is equally amenable to planar substrates. The SCALES technique begins with the blanket growth of a polymer brush, followed by its selective removal based on differences in the etch rate of the underlying substrate. This work uses a poly(methyl methacrylate) (PMMA) brush chemically bonded to the silicon surface, as an alternative to the more commonly used spin-coated PMMA, which allows for selective removal based on the underlying Si carrier concentration by leveraging the selective etch properties of KOH.[22] KOH diffuses through the PMMA, removing a few layers of lightly-doped Si, which also removes the PMMA from these regions. The PMMA remains on the heavily-doped Si, serving as a mask. Using the SCALES patterning technique in combination with AS-ALD, we fabricate a self-aligned gate stack with promising capacitance-voltage characteristics.

Si(100) with doping levels of ~10^{18} cm^{-3} (lightly-doped) and ~10^{20} cm^{-3} (heavily-doped) is used as the substrate to mimic a typical MOSFET structure. A lightly boron-doped Si(100) wafer is patterned with a 500 nm-thick SiO_2 mask before being doped with boron via solid state diffusion (2 h at 1050 °C, B_2O_3 source). The masked regions (100 μm x 100 μm squares and a large 4 mm x 6 mm rectangle for XPS characterization) remain lightly-doped while the rest of the Si substrate is heavily boron-doped. A PMMA brush is synthesized to deactivate the Si surface using an adaptation of a previously described procedure.[21] Briefly, an anchoring molecule (11-undecen-1-ol) is attached to the hydrogen-terminated Si surface via hydrosilylation at 150 °C for 2 hours. Next, an initiating group (bromoisobutyryl bromide) is attached at room temperature for 2 hours. Finally, PMMA is polymerized at 90 °C for 4 hours via atom transfer radical polymerization of methyl methacrylate. The PMMA brush is selectively removed from the lightly-doped regions via

cycles of exposure to KOH solution (1 mL 45 wt% KOH : 3 mL IPA : 8.5 mL DI H_2O) to etch the Si and acetone to solvate the PMMA.

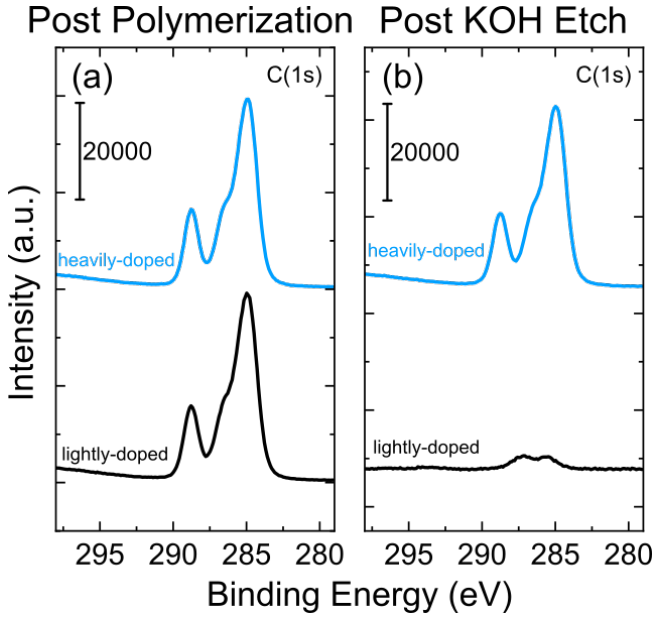

Figure 1. XPS characterization of surface-initiated polymerization before and after selective KOH etch. C(1s) spectra on the heavily-doped (blue) and lightly-doped (black) regions after PMMA polymerization (a) and after the KOH etch (b).

X-ray photoelectron spectroscopy (XPS) is used to characterize the selective removal of PMMA from the lightly-doped silicon. The XPS measurements are conducted using a monochromatic Al Kα source with a spot size of 400 μm and pass energy of 50 eV. Figure 1 shows typical C(1s) XPS spectra for the heavily- and lightly-doped silicon immediately after the polymerization process and after 25 etch cycles. After polymerization (Figure 1a), both the heavily- and lightly-doped silicon show strong C(1s) peaks characteristic of PMMA. It is known that the C(1s) photoelectron spectrum shows four strong peaks for PMMA corresponding to the C-C/C-H, C in α-position to the ester group, C-O, and O-C=O components at 285.0 eV, 285.7 eV, 286.8 eV, 289.1 eV, respectively.[23,24] Following 25 etch cycles (Figure 1b), the C(1s) spectrum is unchanged for the heavily-doped silicon, while the C(1s) peaks reduce by 90% for the lightly-

doped Si. The C(1s) signal observed for the heavily-doped silicon after PMMA removal is equivalent to that of adventitious carbon (not shown).

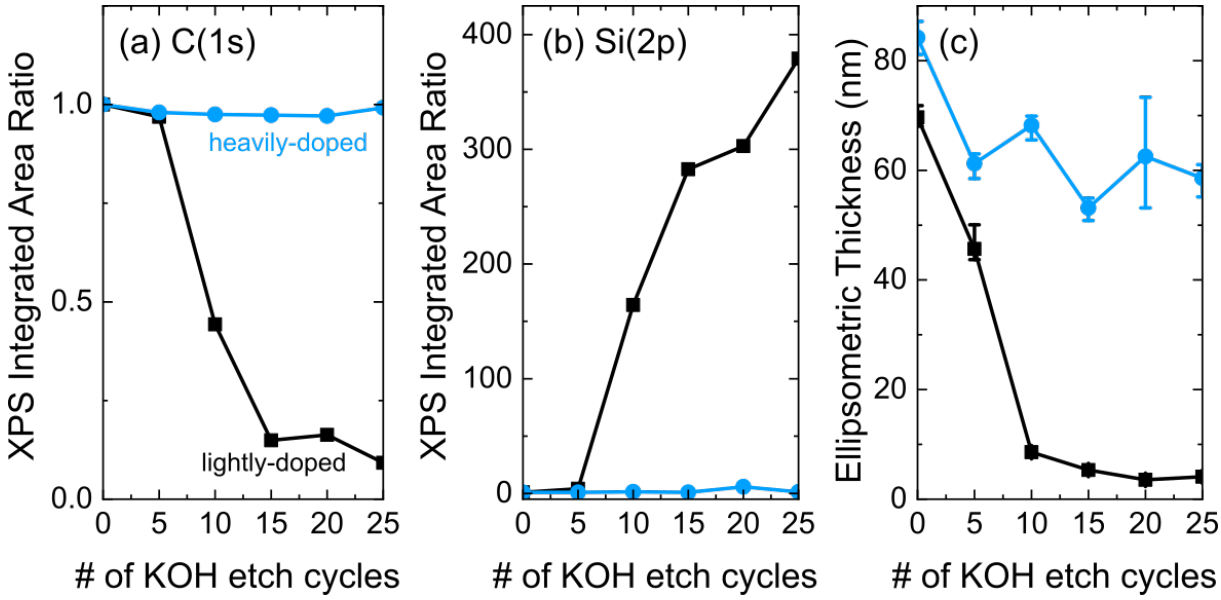

Figure 2. XPS and Ellipsometric characterization of PMMA brush during KOH etch process: (a) Integrated area of the C(1s) XPS spectrum (normalized to initial peak area) vs number of etch cycles; (b) Integrated area of the Si(2p) XPS spectrum (normalized to initial peak area) vs number of etch cycles; (c) PMMA film thickness measured with ellipsometry vs number of etch cycles.

PMMA removal as a function of number of etch cycles is investigated and characterized with XPS integrated area ratios as well as spectroscopic ellipsometry. As seen in Figures 2(a) and 2(b), the constant C(1s) and Si(2p) peak areas on the heavily-doped Si verify the durable attachment of the PMMA brush. On the lightly-doped Si, the C(1s) peak area decreases, and the Si(2p) peak area correspondingly increases as the PMMA is removed. Spectroscopic ellipsometry is performed using a Woollam M200 Ellipsometer, and the CompleteEASE software is used for fitting with the PMMA, SiO_2, and HfO_2 film models. Ellipsometry data in Figure 2(c) shows that the PMMA film thickness remains relatively constant on the heavily-doped Si while it decreases down to just a few nanometers on the lightly-doped Si. Overall, the results indicate that the process can achieve selective masking based on the underlying doping concentration.

To fabricate a gate stack leveraging the SCALES-patterned PMMA mask, HfO_2 and Pt are deposited via AS-ALD. A modified RCA clean consisting of 1 min in SC-1 (5 DI H_2O : 1 H_2O_2 : 1 NH_4OH) at 75 °C, 30 sec HF etch, and 10 min in SC-2 (5 DI H_2O : 1 H_2O_2 : 1 HCl) at 75 °C is used to clean the exposed Si before depositing the oxide and metal layers. The organic SC-1 clean is shortened to one minute to minimize damage to the patterned PMMA film, and the SC-2 clean forms a ~ 2 nm-thick passivating layer of chemical oxide on the Si surface. HfO_2 is then deposited selectively with 60 cycles of thermal ALD using tetrakis(dimethylamido)hafnium (TDMAHf) and H_2O precursors at 200 °C. The exposure times for TDMAHf and H_2O are 0.25 and 0.06 s, respectively, followed by purge times of 20 and 15 s. Immediately following HfO_2 deposition, platinum is selectively deposited with 300 cycles of thermal ALD using (trimethyl)methylcyclopentadienylplatinum(IV) ($MeCpPtMe_3$) and O_2 precursors at 300 °C. The exposure times for $MeCpPtMe_3$ and O_2 are 1 and 10 s, respectively, followed by purge times of 10 s. All materials are deposited with a Cambridge Fiji ALD system with argon as a carrier/purging gas and a total chamber pressure of 0.45 Torr.

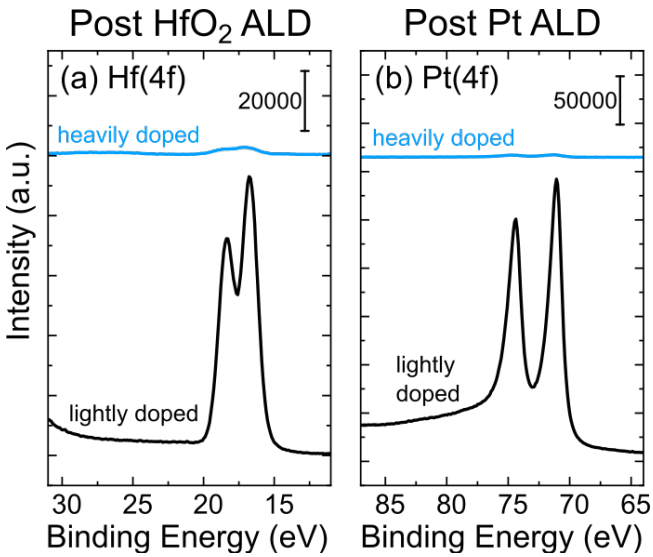

Figure 3. (a) Hf(4f) XPS spectra after HfO_2 ALD of PMMA-covered heavily-doped Si region and of lightly-doped Si region; (b) Pt(4f) XPS spectra after Pt ALD (immediately following HfO_2 ALD) of PMMA-covered heavily-doped Si region and of lightly-doped Si region.

The selectively deposited Pt-HfO_2-Si gate stack is characterized with XPS after each step. Though the deposition temperatures are above the glass transition temperature of PMMA (~115 °C),[25] the polymer brush offers robust passivation against ALD. The Hf(4f) XPS spectra taken after HfO_2 ALD in Figure 3(a) show a doublet with peaks at 16.7 eV and 18.3 eV in the lightly-doped region, confirming the selective deposition of HfO_2 on the exposed Si surface. As can also be seen, minimal HfO_2 deposits on the PMMA covering the heavily-doped regions. A comparison of integrated XPS peak areas for the lightly- and heavily-doped Si regions reveals a deposition selectivity of 30:1. Notably, an examination of TiO_2 and ZrO_2 AS-ALD shows these materials are also compatible with this process (see supplementary material). The Pt(4f) XPS spectra taken after Pt ALD in Figure 3(b) show a strong doublet with peaks at 71.2 eV and 74.5 eV verifying selective deposition of Pt on top of HfO_2 in the lightly-doped regions with very little deposition on the PMMA on the heavily-doped regions. Here, the deposition selectivity between the lightly- and heavily-doped Si regions is found to be 69:1, consistent with what is observed with SAMs[26] and spincoated PMMA.[12].

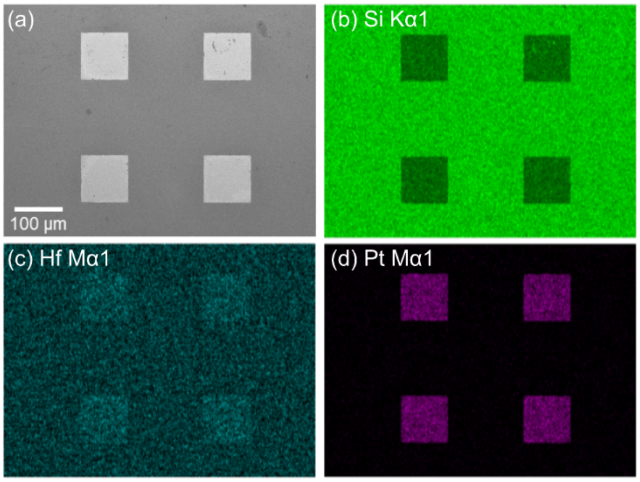

Figure 4. EDS characterization of self-aligned Pt-HfO_2-Si MOS capacitors: (a) SEM image of four, square capacitors; (b) Si elemental mapping by EDS; (c) Hf elemental mapping by EDS; (d) Pt elemental mapping by EDS.

Energy dispersive x-ray spectroscopy (EDS) is used to characterize the resulting self-aligned MOS structures to examine the spatial selectivity of deposition. Figure 4(a) shows an SEM image of four 100 µm x 100 µm MOS capacitors that are aligned with the lightly-doped Si (square) patterns. Figures 4(b), (c), and (d) show EDS maps for Si, Hf, and Pt, respectively, confirming the presence of HfO_2 and Pt mainly within the square patterns. The Hf Mα1 peak overlaps with the large Si Kα1 peak from the substrate, and the extra noise makes the pattern less clear, but a stronger intensity can be seen inside the square patterns where HfO_2 is present under the Pt layer.

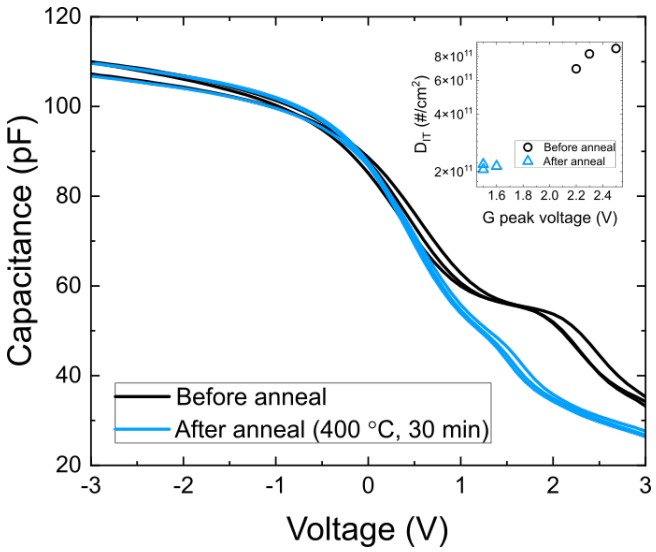

Figure 5. Capacitance vs voltage behavior of three selectively deposited Pt-HfO_2-Si MOS capacitors before and after forming gas anneal.

The MOS capacitors are characterized with capacitance-voltage (C-V) measurements to study the electrical properties of the selectively deposited gate stack and investigate the impact of a forming gas anneal. Capacitance and conductance are measured at 100 kHz with a voltage sweep range from 3 V to -3 V using a Keithley 4200-SCS semiconductor analyzer. Figure 5 shows the C-V behavior of three different MOS capacitors before and after a forming gas anneal at 400 °C for 30 min (96% N_2 / 4% H_2). With an oxide thickness of 6.1 nm of HfO_2 and a 2 nm-thick interlayer of SiO_2 (estimated from ellipsometry measurements), the maximum capacitance (from

Figure 5) is used to estimate a relative dielectric constant of ~ 25.3, as expected for HfO_2.[27] The C-V curves demonstrate typical MOS characteristics and show improved behavior after the forming gas anneal, indicated by the curve's reduced stretch out. The average interface state density of MOS capacitors following AS-ALD is 8.0 x 10^{11} cm^{-2}, as approximated using the conductance peak and $D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max}$. The inset plot in Figure 5 shows that D_{it} can be reduced by a factor of 4 using a forming gas anneal. The D_{it} is relatively high for silicon based MOS capacitors, however, and future work will be performed to improve the interface quality with alternate surface cleaning techniques and improved interfacial layers.

In summary, a self-aligned gate stack structure is demonstrated using a bottom-up process that combines SCALES and AS-ALD. The PMMA brush grafted from the Si(100) surface is selectively removed based on the underlying semiconductor carrier concentration and serves as a mask for ALD. HfO_2 and Pt are selectively deposited, forming MOS capacitors suitable for a gate stack. Current-voltage measurements show expected MOS capacitor behavior and improvement upon forming gas anneal. This process can be used to fabricate complex nano- and micro-structure devices without photolithography, which holds promise for BEOL processes and flexible electronics applications.

Supplementary Material: See supplementary material for XPS characterization of selectively deposited TiO_2 and ZrO_2 films.

Acknowledgements: This work was supported by the Department of Defense (DOD) through the National Defense Science & Engineering Graduate (NDSEG) Fellowship Program and the National Science Foundation (CMMI-1916953). This work was performed in part at the Georgia

Tech Institute for Electronics and Nanotechnology, a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (ECCS-2025462).

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

References:

[1] S. Datta, S. Dutta, B. Grisafe, J. Smith, S. Srinivasa, and H. Ye, IEEE Micro 39, 8 (2019).
[2] T. Bryllert, L.-E. Wernersson, T. Löwgren, and L. Samuelson, Nanotechnology 17, S227 (2006).
[3] D. Akinwande, N. Petrone, and J. Hone, Nat Commun 5, 5678 (2014).
[4] R. Chen, H. Kim, P. C. McIntyre, D. W. Porter, and S. F. Bent, Applied Physics Letters 86 (2005).
[5] R. Chen, H. Kim, P. C. McIntyre, and S. F. Bent, Applied Physics Letters 84, 4017 (2004).
[6] S. Seo, B. C. Yeo, S. S. Han, C. M. Yoon, J. Y. Yang, J. Yoon, C. Yoo, H. J. Kim, Y. B. Lee, S. J. Lee, J. M. Myoung, H. B. Lee, W. H. Kim, I. K. Oh, and H. Kim, ACS Appl Mater Interfaces 9, 41607 (2017).
[7] K. J. Park, J. M. Doub, T. Gougousi, and G. N. Parsons, Applied Physics Letters 86 (2005).
[8] F. S. Minaye Hashemi, C. Prasittichai, and S. F. Bent, ACS Nano 9, 8710 (2015).
[9] W. H. Kim, H. B. R. Lee, K. Heo, Y. K. Lee, T. M. Chung, C. G. Kim, S. Hong, J. Heo, and H. Kim, Journal of the Electrochemical Society 158, D1 (2011).
[10] H. Kim, ECS Transactions 16, 219 (2008).
[11] R. Wojtecki, J. Ma, I. Cordova, N. Arellano, K. Lionti, T. Magbitang, T. G. Pattison, X. Zhao, E. Delenia, and N. Lanzillo, ACS applied materials & interfaces 13, 9081 (2021).
[12] E. Färm, M. Kemell, M. Ritala, and M. Leskelä, The Journal of Physical Chemistry C 112, 15791 (2008).
[13] E. Färm, M. Kemell, E. Santala, M. Ritala, and M. Leskelä, Journal of The Electrochemical Society 157 (2010).
[14] A. Sinha, D. W. Hess, and C. L. Henderson, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 24 (2006).
[15] V. Suresh, M. S. Huang, M. P. Srinivasan, C. Guan, H. J. Fan, and S. Krishnamoorthy, The Journal of Physical Chemistry C 116, 23729 (2012).
[16] A. Sinha, D. W. Hess, and C. L. Henderson, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 25 (2007).
[17] T. G. Pattison, A. E. Hess, N. Arellano, N. Lanzillo, S. Nguyen, H. Bui, C. Rettner, H. Truong, A. Friz, and T. Topuria, ACS nano 14, 4276 (2020).
[18] M. Fang and J. C. Ho, ACS Nano 9, 8651 (2015).
[19] A. J. Mackus, A. A. Bol, and W. M. Kessels, Nanoscale 6, 10941 (2014).
[20] M. J. Biercuk, D. J. Monsma, C. M. Marcus, J. S. Becker, and R. G. Gordon, Applied Physics Letters 83, 2405 (2003).
[21] A. T. Mohabir, G. Tutuncuoglu, T. Weiss, E. M. Vogel, and M. A. Filler, ACS nano (2019).
[22] E. Bassous and A. Lamberti, Microelectronic Engineering 9, 167 (1989).
[23] C. Ton-That, A. Shard, D. Teare, and R. Bradley, Polymer 42, 1121 (2001).
[24] P. Louette, F. Bodino, and J.-J. Pireaux, Surface science spectra 12, 69 (2005).
[25] A. Richard, Faraday Discussions 98, 219 (1994).

[26] R. Chen and S. F. Bent, Advanced Materials 18, 1086 (2006).
[27] S.-W. Jeong, H. Lee, K. Kim, M. You, Y. Roh, T. Noguchi, W. Xianyu, and J. Jung, Thin solid films 515, 526 (2006).