Temperature Dependent Characteristics and Electrostatic Threshold Voltage Tuning of Accumulated Body MOSFETs

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***Abstract*—Narrow-channel accumulated body nMOSFET devices with p-type side-gates surrounding the active area have been electrically characterized between 100 and 400 K with varied side-gate biasing (V_{side}). The subthreshold slope (SS) and drain induced barrier lowering (DIBL) decrease and threshold voltage (V_t) increases linearly with reduced temperature and reduced side-gate bias. Detailed analysis on a 27 nm x 78 nm (width x length) device shows SS decreasing from 115 mV/dec at 400 K to 90 mV/dec at 300 K and down to 36 mV/dec at 100 K, DIBL decreasing by approximately 10 mV/V for each 100 K reduction in operating temperature, and V_t increasing from 0.42 V to 0.61 V as the temperature is reduced from 400 K to 100 K. V_t can be adjusted from ~0.3 V to ~1.1 V with ~0.3 V/V sensitivity by depletion or accumulation of the body of the device using V_{side}. This high level of tunability allows electronic control of V_t and drive current for variable temperature operation in a wide temperature range with extremely low leakage currents (< 10^{-13} A).**

***Index Terms*—Accumulated body MOSFET, cryogenic CMOS, drain induced barrier lowering, leakage current, side-gate, subthreshold slope, threshold voltage tuning.**

I. Introduction

Electrostatic control of the potential barrier between the source and the drain of metal oxide semiconductor field effect transistors (MOSFETs), and the emitter and collector of bipolar junction transistors (BJTs) determine the minimum feature sizes that can be successfully implemented for a given temperature of operation. Since the charges controlling the barrier height in MOSFETs are electrically isolated from the channel, there is no need for continuous charge injection from the control terminal, unlike BJTs. Ultra-thin-body silicon on insulator (SOI) [1]–[5], FinFET [6]–[9], tri-gate [10]–[15], gate-all-around [16]–[23] and multi-gate [24], [25] structures provide significant improvements in electrostatic control of the source-barrier in MOSFETs and suppress or eliminate the interface leakage currents [26]. Partially depleted SOI devices suffer from floating body effects [27], [28], where majority carriers trapped in the active region reduce the source-barrier (similar to charging of the base in BJTs) and cause soft errors. The active regions of bulk MOSFETs have good electrical and thermal contact with the substrate, allowing for efficient charge and heat removal. Electrostatic control of the source-barrier using substrate/body [23], [29]–[36] or back-gate biasing [37]–[39] allows for dynamic control of threshold voltage. In the case of narrow channel devices, an independently controlled side-gate structure that surrounds the body of a bulk MOSFET can be used to accumulate the body of the device and increase electrical coupling of the body to the channel, increase the source barrier and suppress short-channel effects (Fig. 1).

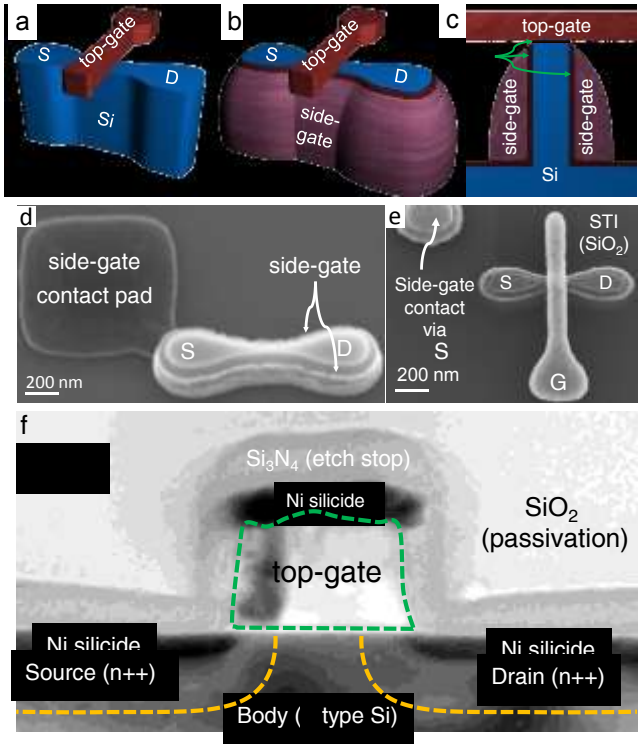

Fig. 1. Schematic drawings of a conventional narrow-channel bulk-Si MOSFET (a), accumulated body MOSFET with side-gate structure (b) and its cross-section view (c). The perspective view of the MOSFET showing the side-gate contact pad before shallow trench isolation (STI) (d), SEM image of the top view of the accumulated-body MOSFET showing the side-gate contact via after STI and gate formation (e), TEM image of a cross-sectional cut in the Source-Drain direction [44] (f).

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We had first reported a side-gated MOSFET structure with silicon nitride side-gate dielectric and field isolation (Si_3N_4 followed by low-stress $Si_{3+x}N_{4-x}$), compatible with removal of sacrificial SiO_2 using HF to open tunnels and release structures, as a very-low leakage device that can be monolithically integrated with micro-/nano-fluidics for high-sensitivity sensors for sequencing of biomolecules [40], [41]. Noticing the success of these devices in suppressing interface leakage currents (below 1 fA), improvements in drain induced barrier lowering (DIBL) and subthreshold slope (SS), and extreme control of threshold voltage (V_t), we fabricated higher-performance versions of these devices with p+ doped side-gates, SiO_2 side-gate dielectrics, and SiO_2 field isolations for accumulated body operation. These accumulated-body devices show dramatic V_t tuning and improved performance characteristics [42]–[45].

Transistors are thermal devices; the barrier height, the energy distribution of the carriers in the source and drain reservoirs and lifetime of trapped charges [46] depend on temperature. Carrier mobilities also increase with reduced temperature [23], [24], [47]–[49]. Hence, transistors can be operated with lower power and at a higher speed under lower temperatures. While high temperature operation is necessary for certain applications [50]–[53], cryogenic operation of high-performance VLSI circuits has been considered for a long time [23], [24], [47]–[49], [54]–[58]. Recent advances and growing interest in quantum computing have also led to renewed interest in cryogenic electronics for peripheral circuitry. However, significant changes in the operation temperature of the whole or part of the circuit introduces additional complexity in VLSI design and in computer architecture [59]–[61]. In this work, we characterized accumulated body devices [Fig.1, 44] in the 100 K to 400 K range, observed the performance characteristics, and explored the ability to dynamically tune V_t as the temperature is changed and the temperature range these devices can reliably operate at.

II. Device Structure and Fabrication

The narrow-channel accumulated body nMOSFETs were fabricated using a conventional bulk silicon process, with additional steps to form the p+ doped side-gate structure and its contact. The side-gate structure is formed around the body using a side-wall process [44], [62]. The side-gate contact is formed in the same etch step by using a lithographically defined region slightly offset from the active region. The side-gates are isolated from the body by 9 nm thermally grown SiO_2 and the top-gate is isolated from the active area by 3.9 nm thermally grown SiO_2. The body is doped with 1×10^{17} cm^{-3} boron, the side-gate with 1×10^{20} cm^{-3} boron, the source and drain with 1×10^{20} cm^{-3} phosphorous using ion-implantation. Details of the device fabrication, room temperature electrical characterization and simulation results, including high temperature behavior, can be found in [43], [44], and [62].

III. Electrical Characterization

All the experiments were carried out using an Agilent 4156C Parameter Analyzer between 100 K and 400 K in 25 K intervals in a Janis cryogenic probe station under vacuum, in dark. The characteristics presented here are from measurements

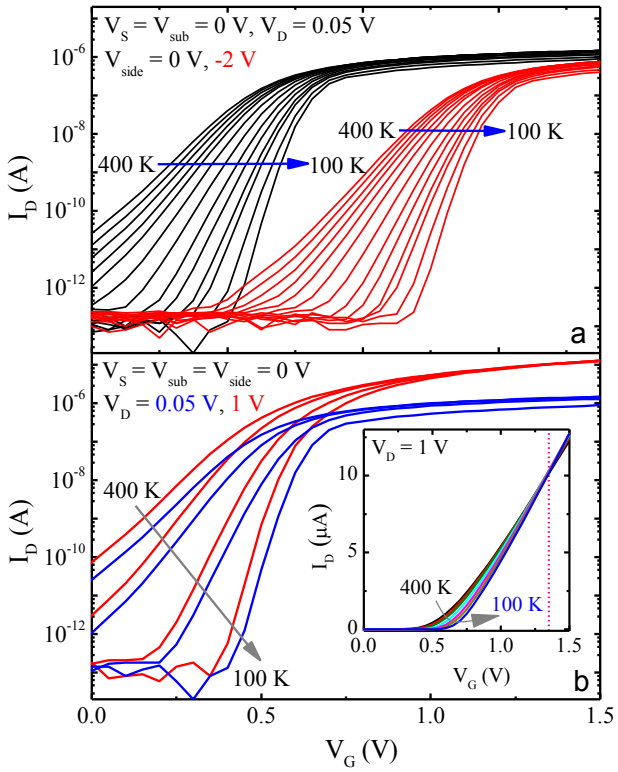

Fig. 2. Temperature and side-gate bias dependent transfer characteristics of a $W \times L = 27$ nm × 78 nm device. The change in V_t induced by the side-gate bias is much larger than the changes due to temperature (a). Temperature sensitivity of V_t decreases with reduced V_{side}. The transfer curves converge at $V_G \approx 1.35$ V for high drain bias (inset).

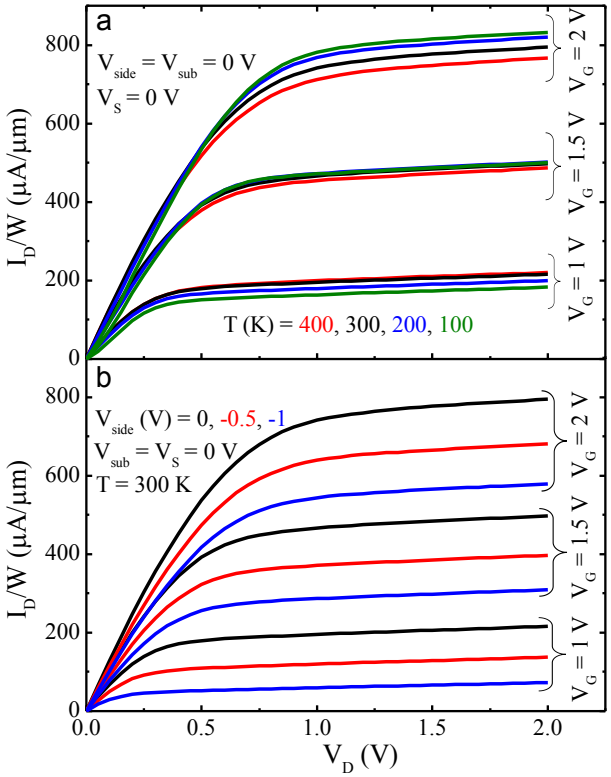

Fig. 3. Temperature (a) and side-gate bias (b) dependent output characteristics of a $W \times L = 27$ nm × 78 nm device. Saturation currents are insensitive to temperature for $V_G \approx 1.5$ V (a). Negative side-gate bias causes the saturation current to decrease (b).

performed on a device with width (W) × length (L) = 27 nm × 78 nm, with grounded source and substrate contacts ($V_S = V_{sub}$ = 0 V) unless stated otherwise (Fig. 2 and Fig. 3).

The body/side-oxide interfaces of these devices are in accumulation, even with V_{side} = 0 V since the side gates are p+ doped (unlike [40], [41]), thus suppressing recombination at the interface defects, blocking interface leakage currents, and reducing the depletion depth under the active region. Negative bias on the side-gate increases the hole concentration at the side-interfaces, shrinks the depletion depth further, increasing the electrostatic control of the body and suppressing control of the drain potential on the source barrier [41], [44], hence, improving DIBL and SS and increasing V_t.

The sensitivity of V_t to temperature ($\Delta V_t/\Delta T$) is significantly reduced for negative side-gate bias while sensitivity of V_t to V_{side} ($\Delta V_t/\Delta V_{side}$) decreases slightly with reduced temperature as shown in Fig. 4(a) and (b). V_t sensitivity to V_{sub} is significantly lower as shown by the open symbols (□) in Fig. 4(b). Subthreshold slope (SS), drain induced barrier lowering (DIBL= $\Delta V_t/\Delta V_D$), and maximum transconductance (g_m) show exponential responses to V_{side} and a linear response to temperature [Fig. 4(c)-(h)]. The observed reduction in drive current for negative side-gate bias [Fig. 4(i)-(l)] appears to be due to the increase in V_t at high drain biases [Fig. 4(i) and (j)] and also to the increase in channel resistance R_{ON} ($R_{ON} = V_{D,lin}/I_{D,lin}$@constant overdrive $V_G - V_t = 125\,mV$) at low drain biases [Fig. 4(k) and (l)]. The saturation current ($I_{D,sat}$) is directly proportional to temperature at lower gate voltages and inversely proportional to temperature at higher gate voltages, and insensitive to temperature for $V_G \approx 1.35$ V [Fig. 2 (inset) and Fig. 4(i)]. This is due to the interplay of increased carrier injection over the source-barrier and reduced mobility with increasing temperature [63]. The response of $I_{D,sat}$ to V_{side} is monotonous [Fig. 4(j)].

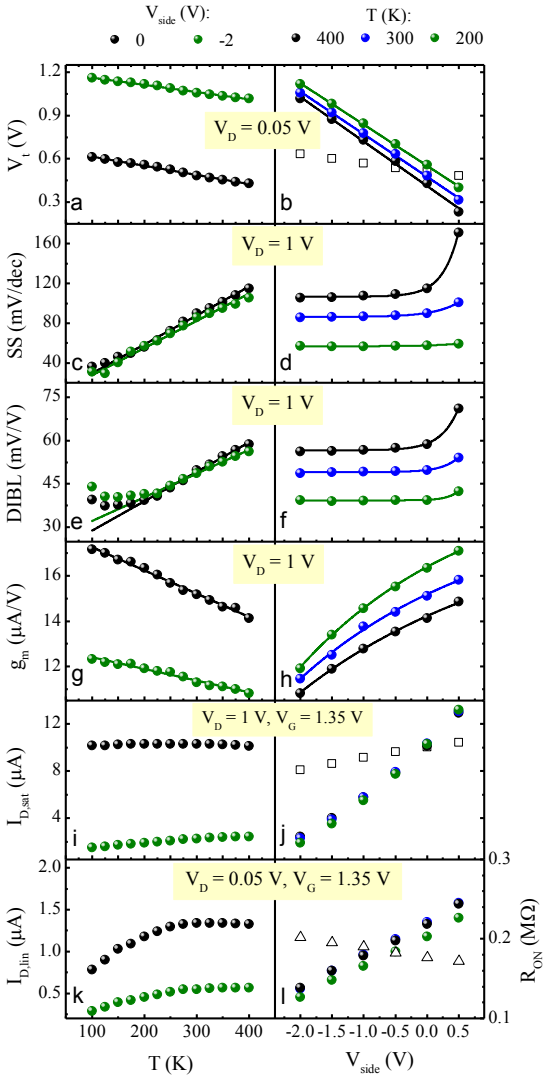

Fig. 4. Temperature and side-gate biasing response of threshold voltage (V_t), subthreshold slope (SS) and drain induced barrier lowering (DIBL), maximum transconductance (g_m), current drive in the saturation and linear regimes extracted from transfer characteristics presented in Fig. 2. The lines correspond to the fits only. V_t values, determined from the linear extrapolation of I_D at the maximum transconductance point, show better sensitivity to V_{side} than with V_{sub}. SS improves by ~ 29 mV/dec for each 100 K. The open squares in (b) and (j) correspond to V_t and $I_{D,sat}$ values vs V_{sub} instead of V_{side}, at V_{side} = 0 V. The open triangles in (l) correspond to R_{ON} (($V_{D,lin}$ = 50 mV)/$I_{D,lin}$ at a constant overdrive of V_G-V_t = 125 mV) vs V_{side}, at 300 K.

IV. Threshold Voltage Tuning

Accumulated body MOSFET offers an independent control through the side-gate which can be used to achieve a certain threshold voltage at different operation temperatures or to compensate for threshold drifts in unwanted local hotspots. The approximately linear response of V_t to V_{side} and T [Fig. 4(a) and

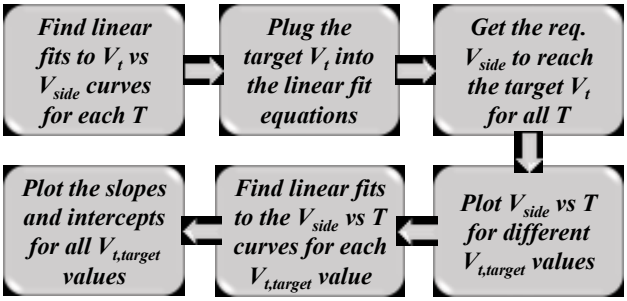

Fig. 5. A flow diagram of the procedure used for V_t tuning process.

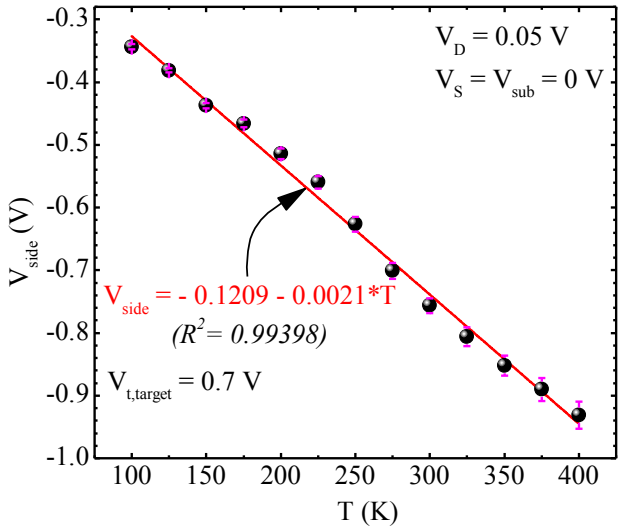

Fig. 6. The side-gate biases required to keep the threshold voltage fixed to 0.7 V across the entire temperature range (100-400 K). The linear fit shows a required rate of 2.1 mV/K V_{side} change to tune the threshold voltage to 0.7 V with a drain bias of 50 mV and the source and the substrate grounded for the device $W \times L$ = 27 nm × 78 nm.

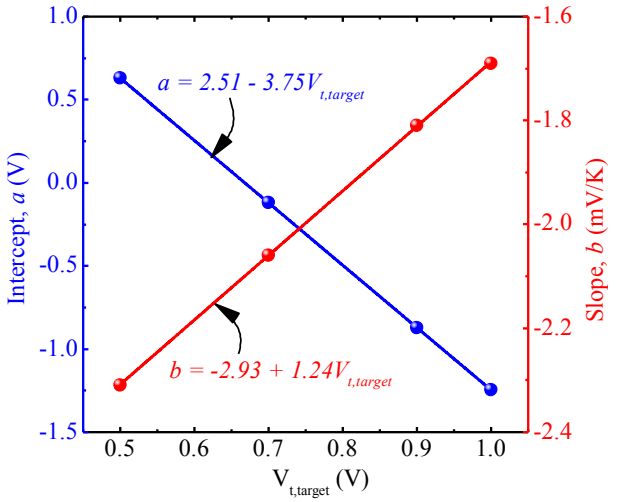

Fig. 7. Fitting parameters (intercept a and slope b) for the V_{side} vs T at different $V_{t,target}$. The parameters change linearly with the desired V_t value. From the fit equations, we can find the values of the slope and the intercept for V_{side} vs T graph for the device $W \times L$ = 27 nm × 78 nm.

(b)] can be used to predict V_{side} values required to maintain a constant V_t in a wide temperature range through a 2D linear fit of V_t (V_{side}, T) as shown in Fig. 5.

The V_t sensitivity to side-gate bias varies only slightly as a function of temperature, from ~ -308 mV/V at 400 K to ~ -278 mV/V at 100 K, between -2 and +0.5 V side-gate bias. This side biasing sensitivity of ~ 300 mV/V allows for threshold voltage tuning across a wide range of voltages. Linear fits to the set of V_t vs V_{side} curves in the 100 – 400 K range allow us to determine the required V_{side} value to tune V_t at a given temperature (Fig. 6). We then repeat this procedure to estimate V_{side} vs T relationships for any desired V_t values (Fig. 7). To validate our procedure, we repeated the I_D-V_G measurements between 100- and 400 K while applying the calculated V_{side} for each temperature to tune V_t to example target values of 0.5 V, 0.7 V, and 0.9 V. Fig. 8 shows the resulting V_t to be very close to the target values. Each I-V was performed once with the calculated V_{side}, after the previous one, with no need for any adjusting iterations, indicating minimal charge trapping on the side-gate dielectric, SiO_2 and Si/SiO_2 interfaces.

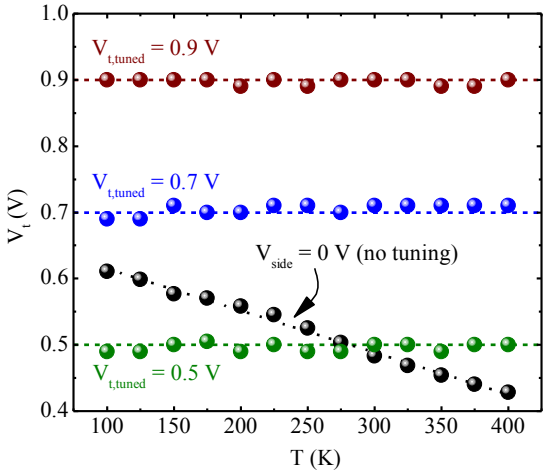

Fig. 8. The calculated threshold voltages after applying the side-gate biases required to keep V_t fixed to 0.5 V, 0.7 V, and 0.9 V, separately, at each temperature point for the device $W \times L$ = 27 nm × 78 nm. The tuned V_t values compared to those for the zero-side-gate bias case point to the proper side-gate biasing compensating for a ~6 mV change in V_t for a 10 K temperature reduction.

V. Summary

Temperature dependent electrical characteristics of narrow side-gated accumulated body MOSFETs in the 100 K and 400 K range are presented. The measurements show strong and very stable temperature and side-gate bias dependence of the transistor characteristics. Subthreshold slope, drain induced barrier lowering, threshold voltage, and leakage current, all exhibit significant improvements with decreasing temperature and side-gate bias, due to mitigation of short-channel effects. Threshold voltage can be tuned with ~ -300 mV/V sensitivity by side-gate biasing, with a fairly linear response. Hence, it is relatively easy to maintain a constant threshold voltage in a wide temperature range or dramatically change the threshold voltage in part or the whole circuit by adjusting the side-gate biases. Excessively negative side-gate biases are expected to result in degradation of the current drive, due to increased surface roughness scattering, which is more pronounced at lower temperatures [64].

Since the depletion depth and the threshold voltage are controlled by the side-gate bias, an undoped body can also be used, reducing any threshold voltage variations due to random dopant fluctuations [65]. Furthermore, the depletion region, and the threshold voltage can be adjusted significantly more than what could be achieved with body doping or biasing. The additional electrostatic control over performance parameters is expected to enable reliable circuit operation in a wide temperature range.

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