

A 4-Element 800MHz-BW 29mW True-Time-Delay Spatial Signal Processor Enabling Fast Beam-Training with Data Communications

Chung-Ching Lin, Chase Puglisi, Erfan Ghaderi,
Soumen Mohapatra, Deukhyoun Heo, Subhanshu Gupta
School of Electrical Engineering and Computer Science
Washington State University, Pullman, USA
chung-ching.lin@wsu.edu

Han Yan, Veljko Boljanovic, Danijela Cabric
Electrical and Computer Engineering Department
University of California Los Angeles
Los Angeles, USA
vboljanovic@ucla.edu

Abstract—Spatial signal processors (SSP) for emerging millimeter-wave wireless networks are critically dependent on link discovery. To avoid loss in communication, mobile devices need to locate narrow directional beams with millisecond latency. In this work, we demonstrate a true-time-delay (TTD) array with digitally reconfigurable delay elements enabling both fast beam-training at the receiver with wideband data communications. In beam-training mode, large delay-bandwidth products are implemented to accelerate beam training using frequency-dependent probing beams. In data communications mode, precise beam alignment is achieved to mitigate spatial effects during beam-forming for wideband signals. The 4-element switched-capacitor based time-interleaved array uses a compact closed-loop integrator for signal combining with the delay compensation implemented in the clock domain to achieve high precision and large delay range. Prototyped in TSMC 65nm CMOS, the TTD SSP successfully demonstrates unique frequency-to-angle mapping with 3.8ns maximum delay and 800MHz bandwidth in the beam-training mode. In the data communications mode, a ~ 12 dB uniform beamforming gain is achieved from 80MHz to 800MHz. The TTD SSP consumes 29mW at 1V supply achieving 122MB/s with 16-QAM at 9.8% EVM.

Index Terms—spatial signal processor, true-time-delay, frequency-to-angle mapping, ring amplifiers, fast beam training

I. INTRODUCTION

Wireless communication and sensing applications at millimeter-wave (mmWave) frequencies require rapid localization and direction finding of mobile nodes [1], [2]. However, current protocols for direction finding are based on repetitive time-division beam sweeping techniques that are often non-scalable and costly in latency (Fig. 1(a)). Novel array architectures and signal processing techniques are required to avoid prohibitive beam training overhead associated with large antenna arrays and narrow beams at mmWave.

True-time-delay (TTD) arrays are appealing yet insufficiently investigated alternative for both fast mmWave beam training and wideband directional data communications. Due to time delaying of the signal in each antenna branch, TTD arrays have frequency-dependent probing beams, which can

Supported partly by NSF awards (#: 1718742, 1955672, 955306, 2030159 and 1944688), CDADIC, DARPA JUMP ComSenTer and CONIX centers.

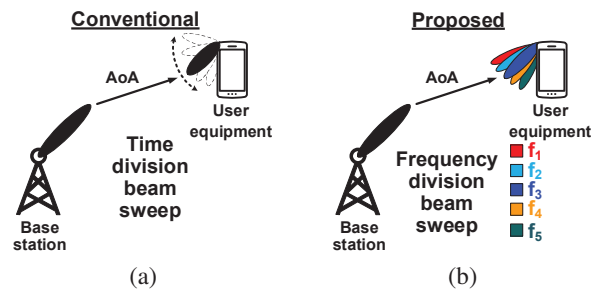


Fig. 1. (a) Latency-costly time-division beam sweep in analog arrays, and (b) proposed low-latency frequency-division beam sweep in analog arrays.

be exploited to enhance the channel probing capability or mitigate spatial effects by fully adjusting the delay introduced in the TTD circuits. Early implementations relied on delay lines in all antenna branches [3], but this approach suffers from limited delay ranges when implemented at RF which renders it insufficient to achieve frequency dispersive beam training as proposed in this work. Recent advancement in TTD arrays with baseband delay elements and large delay range-to-resolution ratios [4], [5] improved the scalability and thus enabled the realization of fast beam training schemes in large arrays without needing any bulky and costly external constructs (such as Rotman Lens [6] or Leaky Wave Antenna [7]). Lastly, it does not have wideband spatial effects (beam-squint) inherent to wideband phase-shift based arrays.

This work presents a reconfigurable TTD spatial signal processor (SSP) with large delay-bandwidth product for unique frequency-to-angle mapping for fast beam-training. Additionally, Wideband data communications is demonstrated using large unity-gain bandwidth and fast slewing ring amplifiers. The proposed architecture validates our fast beam-training algorithm for analog / hybrid arrays proposed in [2], [8] with hardware implementation for the first time. The salient features of this work in the two operation modes are as follows. In the beam-training mode, we demonstrate unique frequency-to-angle mapping with wide field-of-view for fast frequency division based beam-training. The proposed beam-training method do not need costly/bulky external constructs

such as Rotman Lens [6] or Leaky-Wave Antenna [7]. In the data communication mode, we achieve a 60% increase in modulation bandwidth compared to prior art consuming 33% lower power. The TTD SSP uses a 5mW 800MHz bandwidth ring amplifier based switched-capacitor integrator with delay compensation to achieve large delay-bandwidth product.

II. TTD-BASED LOW-LATENCY BEAM TRAINING WITH WIDEBAND COMMUNICATIONS

This section presents the system design for both wideband beam training and data communication, and the associated challenges in TTD IC design. We focus on uniform linear array with N elements. The channel dominant propagation direction is denoted as θ and the array response is $[a(\theta, f)]_n = \exp(-j2\pi(n-1)df \sin(\theta)/c)$, where d is the element spacing, f is the frequency, and c is the speed of light.

Low-latency beam training: The objective of beam training is to use signal received from search beams to identify θ . Fig. 1(a) illustrates the conventional beam training for phased array, where one direction is searched at a time. Hence, finding θ involves high search latency which becomes more troublesome with larger array size and narrower beam-width in the future. Fig. 1(b) shows our recently proposed fast beam training tailored for TTD array. Our approach leverages frequency-dependent search beam to sound all directions simultaneously which greatly reduces beam training latency [2]. More specifically, when TTD delay taps are set to be τ_n in the n -th element of a uniform linear array, the search beam synthesized at the frequency f is defined by the antenna weight vector $w(f)$, whose n -th element is $[w(f)]_n = \exp(-j2\pi f \tau_n)$. Different incident angle θ leads to different system frequency response $|w^H(f)a(\theta, f)|^2$. Hence, one can infer unknown θ by first measuring the system's frequency response, which can be achieved by a single multi-carrier pilot symbol. Furthermore, with the signal bandwidth BW, our theory shows that setting the TTD delay taps as $\tau_n = (n-1)/BW$, $n = 1, \dots, N$ enables searching the entire angular range $\theta \in [-\pi/2, \pi/2]$ at once [2]. The approach required the maximum TTD delay to be $\tau_N = (N-1)/BW$. For example, the delay range needs to be 3.75ns given 800MHz signal bandwidth and the array with $N = 4$ elements. Such bandwidth and delay range requirement represents a big design challenge of TTD IC.

Wideband communication: After the propagation direction θ is identified, TTD-based directional data communication aligns all the signal frequency components with θ and thus avoid the beam squint effect in wideband mmWave systems. Mathematically, the delay taps τ_n needs to be designed such that antenna weight $w(f)$ matches with array spatial response $a(\theta, f)$ for all frequencies, which requires the delay taps $\tau_n = (n-1)d \sin(\theta)/c$. In contrast to beam training, this task is mainly constrained by achievable delay resolution.

III. PROPOSED TTD SSP ARCHITECTURE AND CIRCUITS

This section describes the architecture and IC design of a TTD SSP that handles challenges described before.

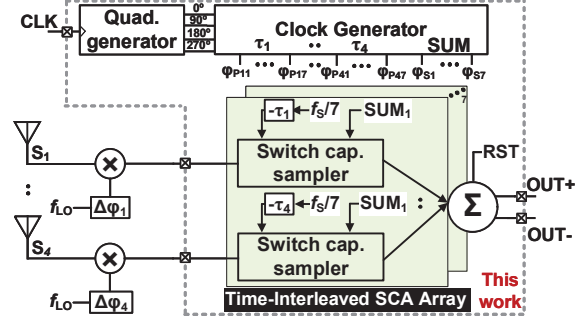


Fig. 2. System architecture of proposed SSP.

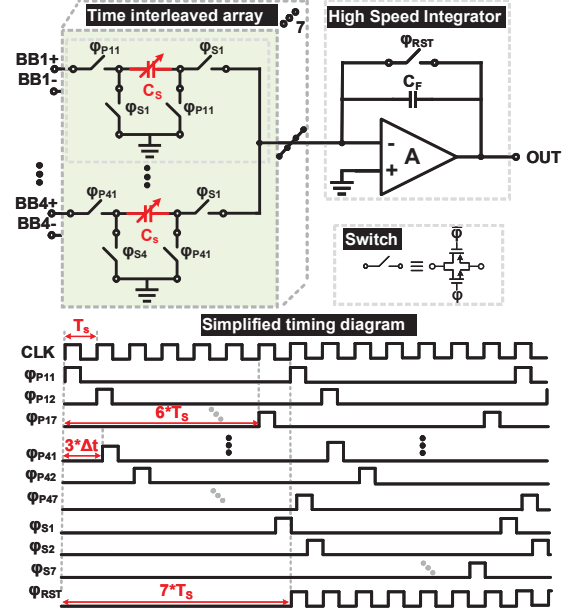


Fig. 3. SCA array realization.

The architecture for the proposed 4-element TTD SSP is shown in Fig. 3. A time-interleaved ring-amplifier based switched-capacitor array (SCA) is used for signal combining. An interleaving factor of 7 was chosen to cover a large delay range while meeting the Nyquist rate sampling requirements of a wideband signal. The delay compensation technique only requires digital logic, switches, and capacitors which can be well integrated in CMOS technology and benefit from process scaling. The SCA requires non-overlapping clocks for sampling, sum, and reset phases generated by a time-interleaver adapted from [4]. Each interleaved level has a conversion speed of roughly 228MHz (1.6GHz/7). The SCA uses 50fF sampling capacitor and optimally sized transmission gates for the switches in each path due to the common mode voltage being at roughly half the supply. Additionally, quadrature signals were assumed to allow for base band vector modulation, simplifying the design of the RF front end (vector modulator not included in this work for brevity).

Summation at the OpAmp virtual ground limits the feedback factor affecting the maximum closed-loop bandwidth possible.

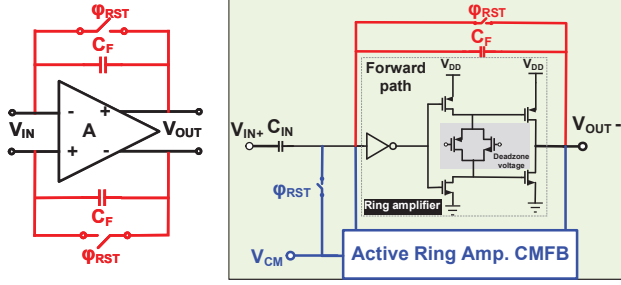


Fig. 4. Ring amplifier (inset) embedded in SCA summer.

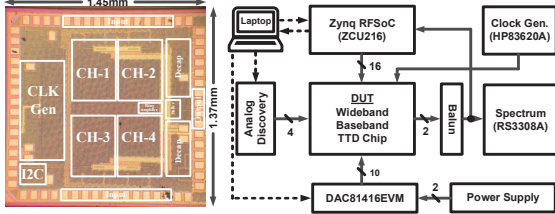


Fig. 5. Die photo and simplified test setup.

While advanced techniques such as [9] can mitigate the aforementioned drawback, higher power, design complexity, and additional area limits its use. Ring amplifier (RAMP) is an emerging topology [10] that aims to realize a low-voltage high-speed amplifier suited for advanced CMOS nodes. The RAMP provides high slew rate capabilities like that of underdamped systems initially, but settle to a desired value very quickly like that of critically damped systems. As shown in Fig. 4, the RAMP was placed in a pseudo-differential configuration with its common mode feedback (CMFB) realized using another ring amplifier placed in the common mode (CM) feedback path with high deadzone voltage. This placement achieves a better common-mode error rejection ensuring the output node is faithfully represented for the entire summing operation [11].

IV. MEASURED RESULTS

The proposed SSP was prototyped in 65nm CMOS occupying 1.98mm² area including pads as shown in Fig. 5. Fig. 5 also shows the test setup with the device-under-test (DUT). The Xilinx ZCU216 7.8GHz RF-DACs is used for both CW and modulated wideband waveform generation uploading MATLAB generated vectors.

Low-latency beam training To prove the concept in Section II, the input signals to the 4 channels of TTD IC are generated by RF-DAC which emulates the OFDM symbols received by a critically spaced linear array at 60GHz with incident angle θ , followed by down-conversion to intermediate frequency at 491.32MHz. The signal has bandwidth $BW = 491.32\text{MHz}$ and subcarrier spacing 960KHz. Each is loaded with a BPSK symbol. Although our beam training conceptually requires only one pilot OFDM symbol to measure the system frequency response and infer θ , our experiment lacks the necessary synchronization. Hence, we intentionally let the same OFDM pilot symbol repeats itself and uses power spectrum density (PSD) estimation of the combined

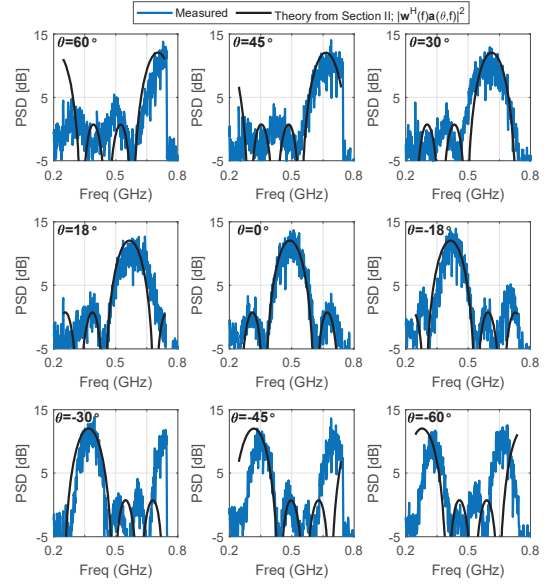


Fig. 6. Proof of fast beam training concept. With a fixed configuration of delay taps, the PSD of the received signal is uniquely determined by incidence angles θ . Hence, θ can be inferred without time-consuming sequential beam sweep.

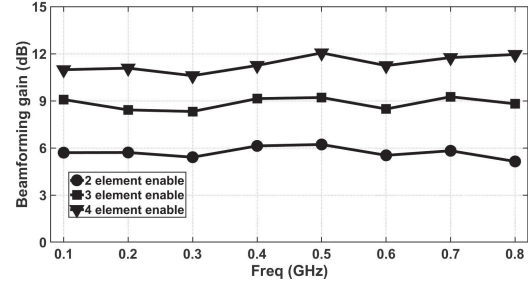


Fig. 7. Measured CW-tone beamforming gain.

signal after DUT as indirect measurements of DUT frequency response. The delay taps τ_n are set according to Section II. Fig. 6 presents the PSD to 9 different incidence angles θ , in contrast with the theoretic frequency response of DUT to θ from Section II. The results indicate the unknown incident angle θ can be identified by analyzing the frequency response of the array upon receiving a wideband pilot symbol, thanks to the TTD frequency-dependent antenna weight vector. The procedure accelerate beam training by avoiding the sequential switching-measuring as required by conventional method.

Wideband communications Measured beamforming gain is plotted in Fig. 7 for an incident angle of 0° with swept CW-tone from near DC to 800MHz, showing an uniform beamforming gain of $\sim 6\text{dB}$, $\sim 9\text{dB}$, and $\sim 12\text{dB}$ as the number of elements are increased from 2 to 4. For the angle of incidence testing, the beam patterns of the SSP are plotted in polar format (Fig. 8), showing the effectiveness of the TTD SSP for 0° , 30° , 60° , and -45° . Fig. 9 shows a $\sim 12\text{dB}$ frequency-independent beamforming gain for a 720MHz wide bandwidth with four channels enabled demonstrating delay compensation with RAMP based signal combiner. The off-chip

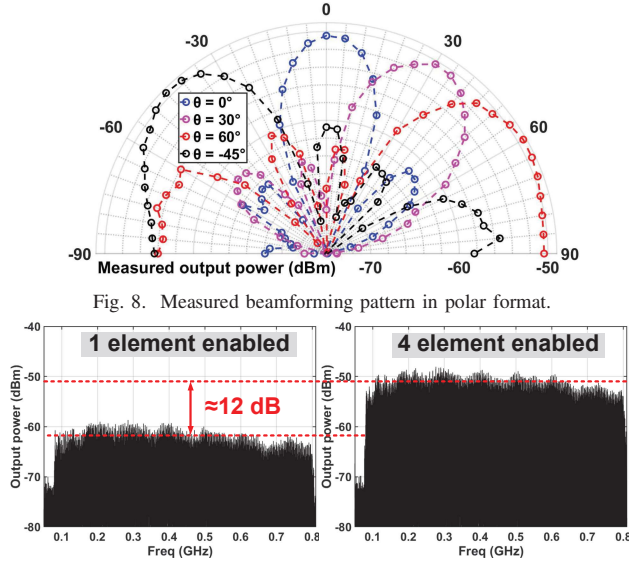


Fig. 8. Measured beamforming pattern in polar format.

bandpass filter with 70MHz 3-dB high-pass corner attenuates the gain at lower frequencies. At higher frequencies, the observed gain roll-off is due to amplifiers in the ZCU216 RF-ADC. Error vector magnitude (EVM) measurement with 30.8Mb/s QPSK signal and 122.8Mb/s 16-QAM signal are fed into the SSP for data communications performance evaluation. An EVM of 5.2% and 9.8% are obtained with four channels enabled as shown in Fig. 10. In these results, the 5dB loss in the on-chip output buffer is not decoupled and that may limit the EVM performance.

Table I summarizes the critical parameters for the proposed TTD SSP and compares with state-of-the-art. Though [13] demonstrated similar bandwidth as the proposed work, the use of a RF sampling mixer and digitally-controlled delay line will limit its application at mmWave frequencies. In contrast, the proposed work has the ability to connect with different RF and mmWave front end downconverters relaxing the overall system design complexity for TTD arrays.

V. CONCLUSIONS

This work demonstrates for the first time the fast beam-training algorithm for TTD arrays leveraging frequency-dependent search beams to sound all directions simultaneously which greatly reduces beam training latency. In addition, the proposed architecture supports wideband data communications with large delay-bandwidth product using fast slewing wideband ring amplifier for efficient signal combining in the baseband switched-capacitor array. A 3.8ns delay compensation across 800MHz bandwidth is demonstrated with EVM of < 10% supporting 16-QAM. Prototyped in 65nm CMOS with 1.98mm², the TTD SSP consumes 29mW only.

REFERENCES

- [1] Y. Ghasempour *et al.*, "Single-shot link discovery for terahertz wireless networks," *Nature Comm.*, vol. 11, no. 1, p. 2017, Apr. 2020.

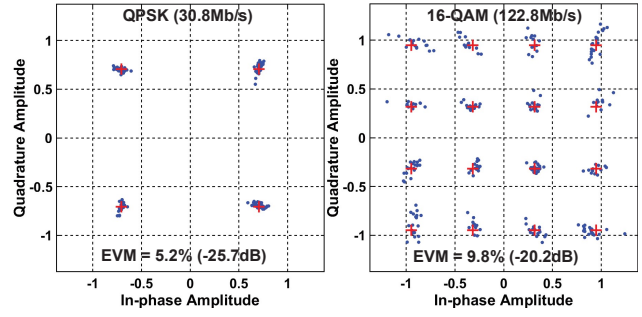


Fig. 10. Measured EVM for QPSK and 16-QAM modulation.

TABLE I
COMPARISON TO PRIOR-ART SSP.

Parameters	[12]	[4]	[5]	[13]	This work
Method	BB-TTD	BB-TTD	BB-TTD	RF-TTD	BB-TTD
Architecture	MIMO	MIMO	MISO	MISO	MISO
# of Elements	4	4	4	4	4
Domain	Charge	Charge	Time	Charge	Charge
BW (MHz)	100	100	500	800	800
Delay range (ns)	10	15	1	5	3.8
Digital intensive	Yes	No	Yes	Yes	Yes
Beamtraining	No	No	No	No	Yes
Power(mW)	70*	52	40†	70	29‡
Area (mm ²)	0.5*	0.82	0.9	1.2	1.98‡
Technology (nm)	65	65	65	28	65

*Baseband delay, mixers, and LO; †incl. ADC power; ‡excl. test buffers;

‡incl. vector modulator

- [2] V. Boljanovic *et al.*, "Fast beam training with true-time-delay arrays in wideband millimeter-wave systems," *IEEE TCAS-I*, vol. 68, no. 4, pp. 1727–1739, 2021.
- [3] T. Chu and H. Hashemi, "True-time-delay-based multi-beam arrays," *IEEE TMTT*, vol. 61, no. 8, pp. 3072–3082, 2013.
- [4] E. Ghaderi *et al.*, "Integrated discrete-time delay-compensating technique for large-array beamformers," *IEEE TCAS-I*, vol. 66, no. 9, pp. 3296–3306, 2019.
- [5] E. Ghaderi *et al.*, "10.8 A 4-element 500MHz-modulated-BW 40mW 6b 1GS/s analog-time-to-digital-converter-enabled spatial signal processor in 65nm CMOS," in *IEEE ISSCC*, 2020, pp. 186–188.
- [6] R. Rotman *et al.*, "True time delay in phased arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 504–518, 2016.
- [7] H. Saeidi *et al.*, "22.1 THz Prism: One-shot simultaneous multi-node angular localization using spectrum-to-space mapping with 360-to-400GHz broadband transceiver and dual-port integrated leaky-wave antennas," in *IEEE ISSCC*, 2021, pp. 314–316.
- [8] H. Yan *et al.*, "Wideband millimeter-wave beam training with true-time-delay array architecture," in *IEEE Asilomar Conf. on Sig., Syst., and Compt.*, 2019, pp. 1447–1452.
- [9] M. Naderi *et al.*, "Operational transconductance amplifier with class-B slew-rate boosting for fast high-performance switched-capacitor circuits," *IEEE TCAS-I*, vol. 65, no. 11, pp. 3769–79, 2018.
- [10] B. Hershberg *et al.*, "Ring amplifiers for switched capacitor circuits," *IEEE JSSC*, vol. 47, no. 12, pp. 2928–2942, 2012.
- [11] J. Lagos *et al.*, "A single-channel, 600-MS/s, 12-b, ringamp-based pipelined ADC in 28-nm CMOS," *IEEE JSSC*, vol. 54, no. 2, pp. 403–416, 2019.
- [12] A. Fikes *et al.*, "Programmable active mirror: A scalable decentralized router," *IEEE TMTT*, vol. 69, no. 3, pp. 1860–74, 2021.
- [13] K. Spoof *et al.*, "A 0.6–4.0 GHz RF-resampling beamforming receiver with frequency-scaling true-time-delays up to three carrier cycles," *IEEE SSCL*, vol. 3, pp. 234–237, 2020.