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Atomic Layer $MoTe_2$ Field-Effect Transistors and Monolithic Logic Circuits Configured by Scanning Laser Annealing

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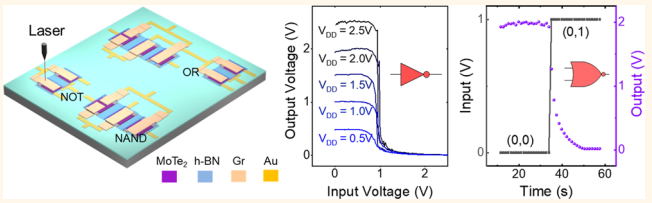
ABSTRACT: Atomically thin semiconductors such as transition metal dichalcogenides have recently enabled diverse devices in the emerging two-dimensional (2D) electronics. While scalable 2D electronics demand monolithic integrated circuits consisting of complementary p-type and n-type transistors, conventional p-type and n-type doping in desired regions, monolithically in the same semiconducting atomic layers, remains elusive or impractical. Here, we report on an agile, high-precision scanning laser annealing approach to realizing 2D monolithic complementary logic circuits on atomically thin $MoTe_2$, by reliably designating p-type and n-type transport polarity in the constituent transistors *via* localized laser annealing and modification of their Schottky contacts. Pristine p-type field-effect transistors (FETs) transform into n-type ones upon controlled laser annealing on their source/drain gold electrodes, exhibiting a mobility of 96.5 $cm^2\ V^{-1}\ s^{-1}$ (the highest known to date) and an On/Off ratio of 10^6. Elucidation and validation of such an on-demand configuration of polarity in $MoTe_2$ FETs further enable the construction and demonstration of essential logic circuits, including both inverter and NOR gates. This dopant-free, spatially precise scanning laser annealing approach to configuring monolithic complementary logic integrated circuits may enable programmable functions in 2D semiconductors, exhibiting potential for additively manufactured, scalable 2D electronics.



KEYWORDS: *2D electronics, molybdenum ditelluride, $MoTe_2$, laser annealing, polarity control, Schottky barrier, complementary logic circuit*

INTRODUCTION

Atomically thin transition metal dichalcogenides (TMDCs) have been investigated and employed for diverse 2D nanoelectronic devices.[1,2] Two-dimensional field-effect transistors (FETs) with TMDCs as channel materials, such as MoS_2 n-FETs and WSe_2 p-FETs, have shown very promising functions and performance.[3] p-Type and n-type FETs are essential building blocks for enabling 2D integrated circuits.[3,4] Rational control and manipulation of the transistor polarity is highly desirable for constructing complementary logic integrated circuits on a single TMDC material platform, similar to CMOS in silicon. However, as the channel thickness approaches a single- or few-layer thickness in these crystals, conventional techniques for realizing complementary pairs of p- and n-type FETs, such as ion implantation and dopant diffusion,[5,6] no matter how mild, become cumbersome or impractical.

Possible solutions include a number of unconventional atomic doping and surface modification techniques that are being explored, such as molecular doping,[7−9] surface charge transfer or electron doping,[10−12] electrical activation,[13,14] focused laser irradiation,[15−17] and deep ultraviolet (DUV) irradiation.[18,19] These methods mainly involve surface dopants or H_2O in the atmosphere,[8] MgO film evaporated by electron-beam evaporation,[11] O_2/H_2O *via* electrothermal annealing induced by an electric field,[14] or doping in the channel due to generation of vacancy defects and excess O atoms induced by laser irradiation.[15] Another route is electrostatic doping achieved through gating, where the presumably dominant transport carrier type in the 2D channel is often regulated and dominated by a Schottky barrier (SB).[20,21] However, the state-of-the-art method of tailoring the SB height has been limited to employing contact metals with different work functions. Lately, we have demonstrated dopant-free control of transport polarity

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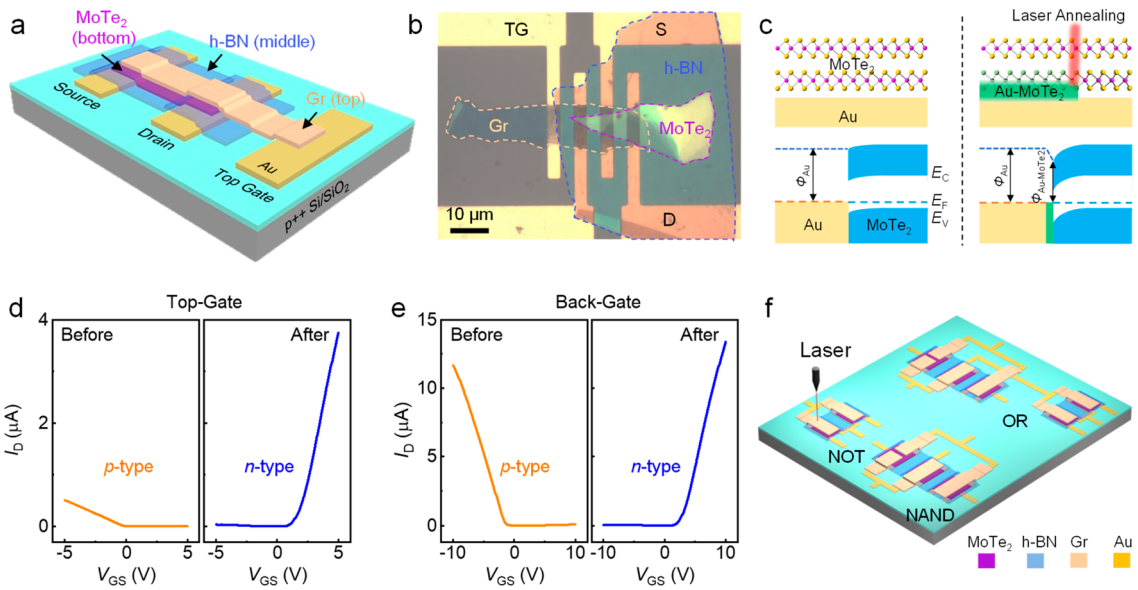

Figure 1. $MoTe_2$ Schottky barrier field-effect transistor (SB FET) with both back and top gates and its polarity change *via* focused laser annealing of the Schottky contacts. (a) Schematic illustration of a dual-gated $MoTe_2$ FET. (b) Optical microscopy image of the representative device composed of $MoTe_2$ at the bottom, h-BN in the middle, and a thin graphite (Gr) layer as the top gate. (c) Interface of $MoTe_2$–Au contact under laser annealing and its corresponding energy band diagram. (d, e) I_D–V_{GS} characteristics of the top-gate branch and back-gate branch before and after laser annealing, respectively, at V_{DS} = 0.1 V. (f) Schematic illustration depicting a single scanning laser probe can directly write and configure, on demand, various monolithic complementary logic circuits on the same $MoTe_2$ film.

in $MoTe_2$ FETs by chip-level bulk thermal annealing-induced modification of Schottky barriers at source/drain contacts of $MoTe_2$ FETs.[22] Toward realizing integrated circuits and scalable 2D electronics with high-performance complementary p-type and n-type FETs on the same $MoTe_2$ thin film monolithically, however, major technological gaps remain, and significant in-depth investigations are still needed.

In this work, we develop 2D monolithic complementary logic circuits by assigning and configuring p- and n-FETs on-demand, on the same $MoTe_2$ thin layer with metallic electrodes, *via* direct focused laser writing and localized annealing of the $MoTe_2$–metal contacts. The SB height at $MoTe_2$–metal contacts of the global-gated $MoTe_2$ FETs is modified by the focused laser annealing ($T \approx 141$ °C, by using a 785 nm laser, a laser power of 13.2 mW with a 1 μm spot size), changing the selected FETs' transport polarity from p-type to n-type. Determined by the spot size of the laser, the spatial resolution is ~1 μm. This method is efficiently exploited to configure families of $MoTe_2$ SB FETs, thus to create complementary inverters and NOR gates. Further, a thin hexagonal boron nitride (h-BN) flake as the dielectric for the top-gate device encapsulates the $MoTe_2$ layer, enhancing device performance and stability. The effectiveness and simplicity of the SB FETs' polarity control method manifest in several aspects. The scanning laser annealing is highly localized only on the $MoTe_2$–metal contact regions, with no perturbation in the channel. The stability of the FETs is improved by the h-BN encapsulation. This approach sheds light on the potential of agile and efficient laser-writing enabled, p-type and n-type configurable SB FETs, for large-area 2D integrated circuits.

RESULTS AND DISCUSSIONS

p-Type to n-Type Polarity Change in Dual-Gate $MoTe_2$ FETs by Laser Annealing. Surface transport dominates in 2D FETs since global electrostatic gating enables carrier accumulation near the semiconductor surface when the gate voltage is applied. The characteristics of metal–semiconductor (M-S) contacts determine the transport of the accumulated carriers. Due to the effect of interfacial states,[23] 2D semiconductors always form Schottky contact with the source/drain (S/D) electrodes. Therefore, engineering the SB height in 2D FETs can decide which type of carriers can go through the channel, thus altering the transistor polarity. Here, we propose a method of SB height modification by using spatially controllable focused laser annealing of $MoTe_2$–Au contacts to change the FET polarity from p-type to n-type. We design dual global gates in the thin $MoTe_2$ FET as illustrated in Figure 1a. The dual-gated $MoTe_2$ FET consists of an h-BN layer as the top-gate dielectric, SiO_2 as the back-gate dielectric, and thin graphite (Gr) as the top gate. The top-view optical micrograph of the as-fabricated h-BN/$MoTe_2$ FET (Figure 1b) displays the distinctive colors of different stacking layers. Raman spectroscopy probing (λ = 532 nm) on the Gr/h-BN/$MoTe_2$ stacking region provides the overall information about the identities of the constitutive flakes (Supplementary Figure S1(a,b)). The thicknesses of h-BN, Gr, and $MoTe_2$ layers are 9, 7, and 8 nm, respectively (Supplementary Figure S1(c,d)). Figure 1c shows laser annealing treatment is applied on the $MoTe_2$–Au structure in order to change the interface material property. Here, the left panels of Figure 1d and e display that the top-gate and back-gate branches of the FET both exhibit hole conduction (p-type) before laser annealing. In the right panel of Figure 1d, with varying gate voltage, the drain current output characteristics (I_D–V_{GS}) of the top-gate transistor show electron conduction (n-type) behavior after laser annealing. The back-gate FET displays the same phenomenon of the polarity change from p-type to n-type after laser annealing (Figure 1e). The value of the gate voltage at which the drain current I_D assumes its minimum (V_{Min}) is positive, shown in Supplementary Figure S2, indicating that the laser-heated $MoTe_2$ FET channel remains p-doped and thus the transport

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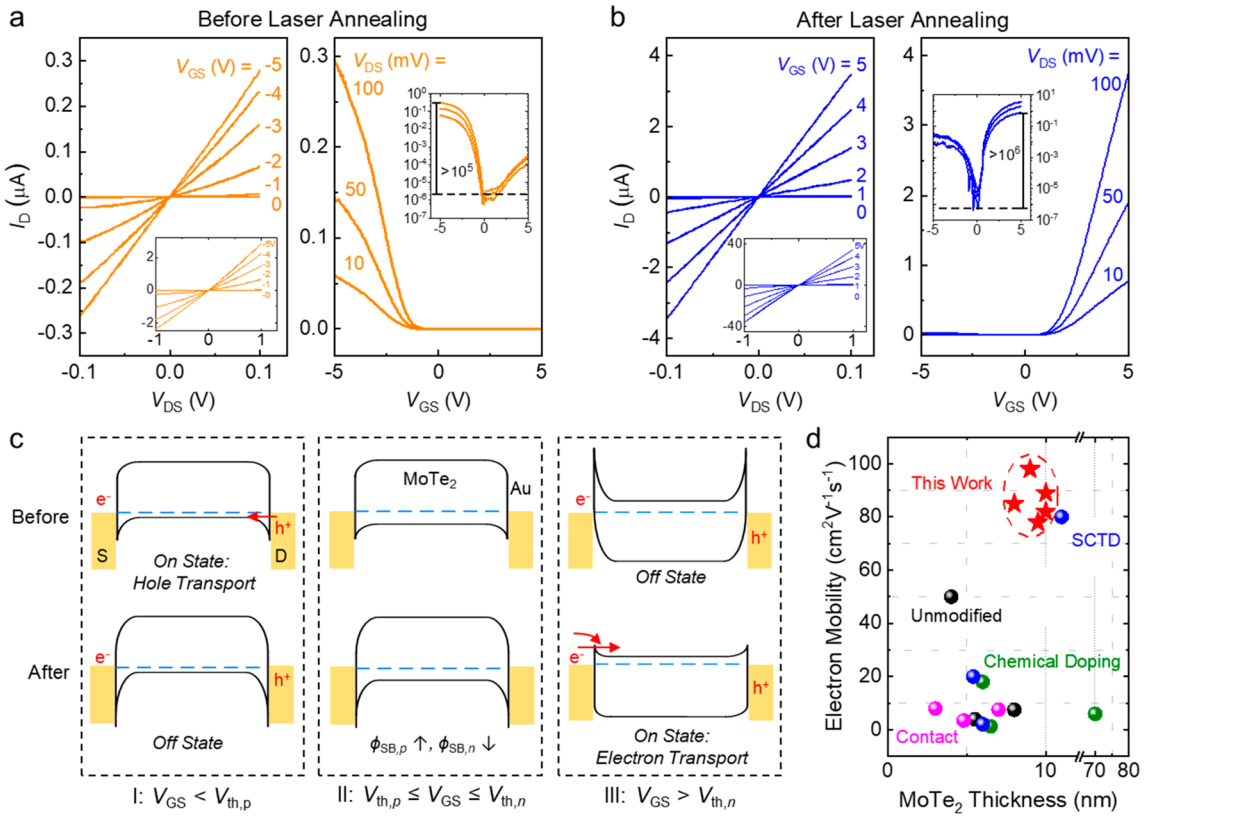

Figure 2. Electrical characteristics and performance of top-gate $MoTe_2$ p-FET and n-FET and their corresponding band diagram analysis. (a) (Left) Drain current I_D as a function of V_{DS} for the top-gate $MoTe_2$ FET before laser annealing, increasing with decreasing top-gate voltage, V_{GS}, from 0 to −5 V with a step of −1 V. Insets in (a) and (b) are I_D−V_{DS} curves with a wider range of V_{DS}. (Right) I_D as a function of V_{GS} with drain-to-source bias voltage, V_{DS}, of 10, 50, and 100 mV, in linear and logarithmic scales, respectively. (b) I_D−V_{DS} and I_D−V_{GS} characteristics of the same transistor after laser annealing. (c) Corresponding electrostatic gated band diagrams of the transistor with horizontal source−gate−drain structure during the laser annealing process. (d) Measured electron field-effect mobility of the n-type $MoTe_2$ FETs and comparison with data in the literature.

behavior of the laser-heated FET is not determined by the channel doping. Figure 1f illustrates the logic gates (OR, inverter, NAND) that we envision to employ this localized laser annealing to configure and validate.

The electrical performance of the top-gate $MoTe_2$ FET is systematically studied, as shown in Figure 2. Figure 2a presents the I_D−V_{DS} and I_D−V_{GS} characteristics of the device before laser annealing. The field-effect hole mobility is $\mu_{FE,p} = \frac{L^2}{CV_{DS}}\frac{dI_D}{dV_{GS}} \approx 7.57$ cm^2 V^{-1} s^{-1}, where L and C are the channel length and the gate capacitance, respectively. Interestingly, after laser annealing, the electronic characteristics exhibit the opposite behavior, n-type conduction with an On/Off current ratio of $I_{on}/I_{Off} > 10^6$, as shown in Figure 2b. The change of the polarity manifests the variation of SB height: $\phi_{SB,p} > \phi_{SB,n}$. The curves in Figure 2b appear just like mirror images of those in Figure 2a, demonstrating a clear and neat polarity change from p-FET to n-FET. The electron mobility of the n-type $MoTe_2$ FET is calculated to be $\mu_{FE,n}$ = 96.5 cm^2 V^{-1} s^{-1} at V_{GS} = 3.35 V, which is the highest electron mobility value reported to date. Before laser annealing, the contact resistance R_c is about 125 kΩ·μm, as shown in Supplementary Figure S3. After laser annealing it turns out that R_c reduces to 10 kΩ·μm. In addition, the hysteresis effect also decreases after the laser annealing (Supplementary Figure S4). The intrinsic origin of the hysteresis effect in $MoTe_2$ transistors could probably be attributed to charge trap states at the interface between $MoTe_2$ and the dielectric due to adsorption/desorption of air/water molecules or other contaminants. These results demonstrate that the $MoTe_2$ device functions as a p-type FET and n-type FET through global electrostatic gating, before and after focused laser annealing of the Schottky contacts, respectively. From the carrier transport perspective, electronic characteristics of the $MoTe_2$ transistor during the laser annealing process are explained using band diagrams at $V_{GS} < V_{th,p}$, $V_{th,p} \le V_{GS} \le V_{th,n}$, and $V_{GS} > V_{th,n}$, all illustrated in Figure 2c. We consider $MoTe_2$ as initially a p-type material due to the built-in Te excess, which dictates that the Fermi level (E_F) should be closer to the valence band. Before laser annealing, the Schottky barrier height for holes ($\phi_{SB,p}$) is lower than that for electrons ($\phi_{SB,n}$), resulting in the On state when $V_{GS} < V_{th,p}$, while $\phi_{SB,p}$ increases and $\phi_{SB,n}$ ($\phi_{SB,n} = E_g - \phi_{SB,p}$) decreases after laser annealing, which corresponds to the work function reduction of the Au−$MoTe_2$ composite. The transistor is switched On when $V_{GS} > V_{th,n}$, presenting n-type conduction. As shown in Figure 2d, the methods for realizing n-type $MoTe_2$ FETs reported to date include intrinsic n-type $MoTe_2$,[24] chemical doping,[24] surface charge transfer doping (SCTD),[25] and contact engineering.[26] Our n-type $MoTe_2$ FETs exhibit higher mobility than counterparts reported in previous studies.[4,8,11−13,19,22,25−38] In addition, $MoTe_2$ FETs with fewer numbers of layers (<12 layers) exhibit declined mobility due to enhanced Coulomb impurity scattering.[39]

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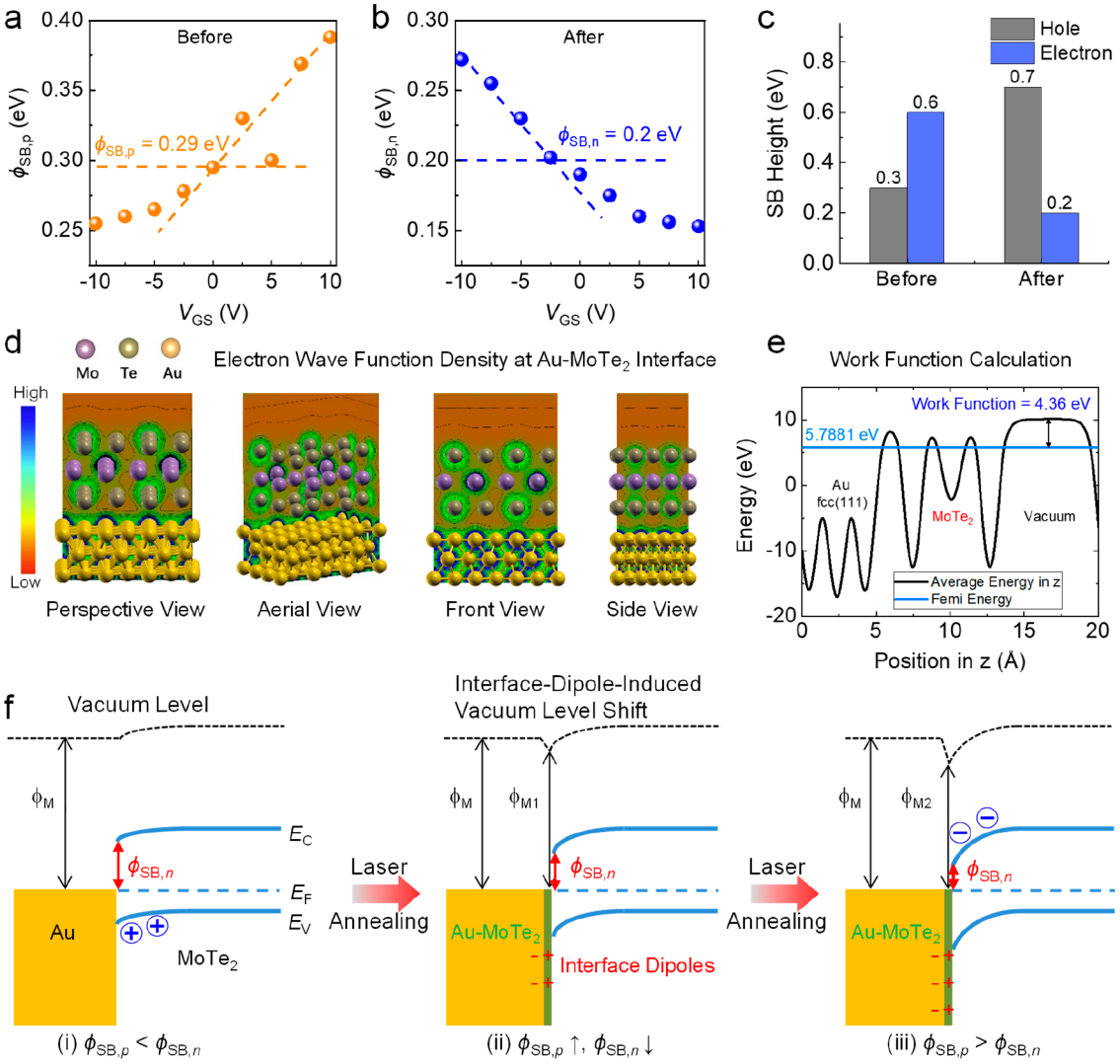

Figure 3. Extraction of the Schottky barrier (SB) height and band diagram analysis during the laser annealing process. (a, b) Gate voltage dependence of the SB height before and after laser annealing. (c) Comparison of the SB height values for electrons and holes before and after scanning laser writing on contacts. (d) Possible interface structure of Au−$MoTe_2$ including position of atoms and local electron wave probability density computed by DFT. (e) Work function of Au−$MoTe_2$ from *ab initio* calculations. (f) Energy band diagrams of the vertical $MoTe_2$−Au contact at the initial state and during the laser annealing process. The thicknesses of the Au/Au−$MoTe_2$ alloy/$MoTe_2$ structure are not to scale. The thickness of the band-bending region is <1 nm.

The pristine $MoTe_2$ is initially a p-type material due to tellurium (Te) excess during the crystal synthesis.[40] Energy dispersive X-ray spectroscopy (EDS) analysis (Supplementary Figure S5) shows that the atomic ratio of Te/Mo ranges from 2.33 to 2.14, indicating that the stoichiometric value of $MoTe_2$ is over 2, before and after laser annealing. It is reported that the $MoTe_2$ with the h-BN encapsulation can remain intact under thermal annealing treatment.[41,42] Thus, it is clearly verified that the fact of p-type doping in the channel does not change before and after the laser annealing, while the carrier transport in the transistor changes from p-type to n-type after the treatment.

Elucidating the Mechanism: $MoTe_2$−Au Schottky Barrier Change *via* Laser Annealing. To evaluate the SB height, the variations of the current through the device as a function of V_{GS} under different temperatures are used to generate the Arrhenius plots reported in Supplementary Figure S6. It is well known that in an FET the current depends mainly on the thermionic emission and the thermally assisted tunneling. The effective SB height ϕ_{SB} is extracted using the equation[20] $I_D = AT^2\exp(q\phi_{SB}/k_BT)[1 - \exp(qV_{DS}/k_BT)]$, where A is the Richardson's constant, k_B is the Boltzmann constant, q is the electronic charge, and T is the temperature. Since we consider $qV_{DS} \gg k_BT$ when V_{DS} is applied with 1 V, the equation can be simplified to obtain a linear relationship between $\ln(I_D/T^2)$ and $1000/T$ as shown in Supplementary Figure S6. Therefore, the SB height is determined from the slope of the Arrhenius plots and plotted as a function of V_{GS} in Figure 3a and b. From Figure 3a, a true Schottky barrier height of the p-type transistor before laser annealing is extracted to be around 0.3 eV. From Figure 3b, the Schottky barrier height for electrons of the transistor after laser annealing is extracted to be around 0.2 eV. Therefore, upon laser annealing, the SB height for holes increases from $\phi_{SB,p}$ = 0.3 eV to 0.7 eV, while the SB height for electrons decreases from $\phi_{SB,n}$ = 0.6 eV to 0.2 eV (Figure 3c). These results clearly provide direct and deterministic evidence of modifying relative SB heights for electrons/holes by laser writing on the contacts.

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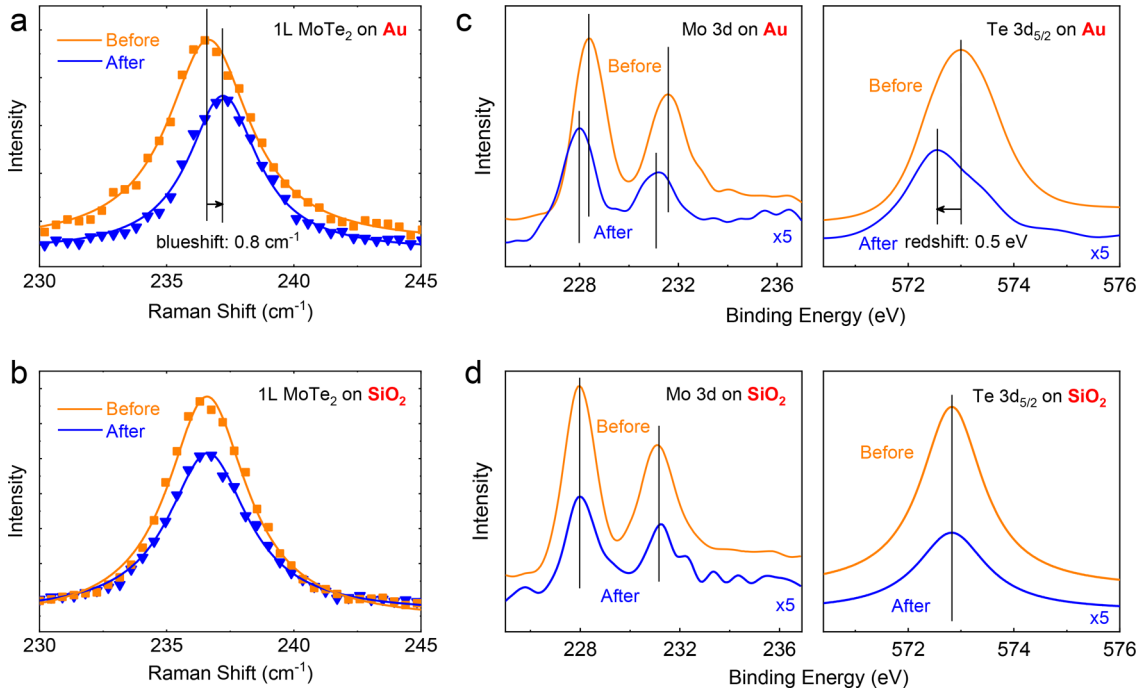

Figure 4. Spectroscopic characterization of the $MoTe_2$–Au Schottky contacts. (a) Raman analysis of single-layer (1L) $MoTe_2$ on the Au electrode before and after laser annealing. (b) Raman spectra of the 1L $MoTe_2$ on the SiO_2 substrate for comparison. (c) XPS spectra of a few-layer $MoTe_2$ flake on the Au electrode and (d) on the SiO_2 substrate (bottom panels). The vertical dashed lines indicate the positions of the XPS spectral peaks.

To further understand the observed SB height variation under laser annealing, we perform first-principle calculations (by using density functional theory (DFT)) for the electron wave function probability density and work function of the Au–$MoTe_2$ interface as shown in Figure 3d and e. We have computed the possible Au–$MoTe_2$ interface structures. It turns out that the effective work function of the Au–$MoTe_2$ interface is 4.36 eV. The value is between those of bare Au (5.1 eV) and $MoTe_2$ (4.1 eV), indicating SB height lowering on the Au–$MoTe_2$ interface after laser annealing.[43] DFT calculations are also conducted on the Au–$MoTe_2$ interface with different distances between Au and $MoTe_2$ as shown in Supplementary Figure S7. Considerable metal-induced gap states (MIGS) can be seen from the plots of local density of states, and the MIGS reduce as the distance between Au and $MoTe_2$ increases. In addition, by analyzing the band alignment of $MoTe_2$ on Au during the laser annealing process (Figure 3f), it suggests that the $MoTe_2$–Au interface exhibits a lower work function compared to that of the bare Au, resulting in the SB height for electrons ($\phi_{SB,n}$) decreasing and becoming lower than that for holes ($\phi_{SB,p}$).

In order to validate the effect of the M-S contact on the transistor polarity, we have conducted a control experiment in which the focused laser only illuminates the $MoTe_2$ channel region. The I_D–V_{GS} characteristics (Supplementary Figure S8) show that the $MoTe_2$ FET remains p-type after laser illumination when the laser is focused only on the channel region, which suggests that the earlier observed transistor polarity change is indeed due to scanning laser annealing of the Schottky contacts and is independent of the channel region, and the carrier polarity of $MoTe_2$ on SiO_2 has been negligibly affected by laser annealing of the channel region. As another control experiment, platinum (Pt), with a higher work function ($\phi_{M,Pt}$ = 5.9 eV), is used as the S/D electrodes for the $MoTe_2$ FETs (Supplementary Figure S9). We do not observe the transistor polarity change from p-type to n-type conduction after laser annealing of the $MoTe_2$–Pt contacts. In addition, it validates that Fermi level pinning does not dictate the SB height. In fact, if Fermi level pinning was playing a role universally in all these Schottky contacts, then the devices with Pt S/D contacts should have also exhibited a polarity change upon laser writing on the S/D contacts. Therefore, the Fermi level pinning effect of the metal contacts in our transistors is not dominant in our devices with the prepatterned S/D electrodes.[44,45]

Subsequently, the underlying mechanism of the transistor polarity change is elucidated through spectroscopic characterization of materials (Figure 4). The interface of single-layer (1L) $MoTe_2$ and the Au electrode is investigated through Raman spectroscopy and X-ray photoelectron spectroscopy (XPS). The 1L $MoTe_2$ flake on Au (Supplementary Figure S10) is treated by focused laser annealing as described in the Methods. As seen in Figure 4a, the laser-heated $MoTe_2$ region exhibits a clear Raman peak shift (to the right) as compared to that of the pristine area. The roughness of $MoTe_2$ on Au decreases slightly after laser annealing due to the improved contact quality; there is no other peak observed in the Raman spectra before and after laser annealing (Supplementary Figure S11). In comparison, Raman data of 1L $MoTe_2$ on the SiO_2 substrate show no peak shift before and after laser annealing (Figure 4b). Following previous studies about the effect of annealing on other 2D material such as MoS_2,[46−48] we estimate that the Raman shift of $MoTe_2$ on the Au contacts after laser annealing is caused by some interactions, such as alloying or hybridization, thus changing the effective work function and Schottky barrier at the contacts. The $MoTe_2$–Au interaction is further verified by XPS, with associated evidential XPS peak shifts displayed in Figure 4c, while in contrast, the

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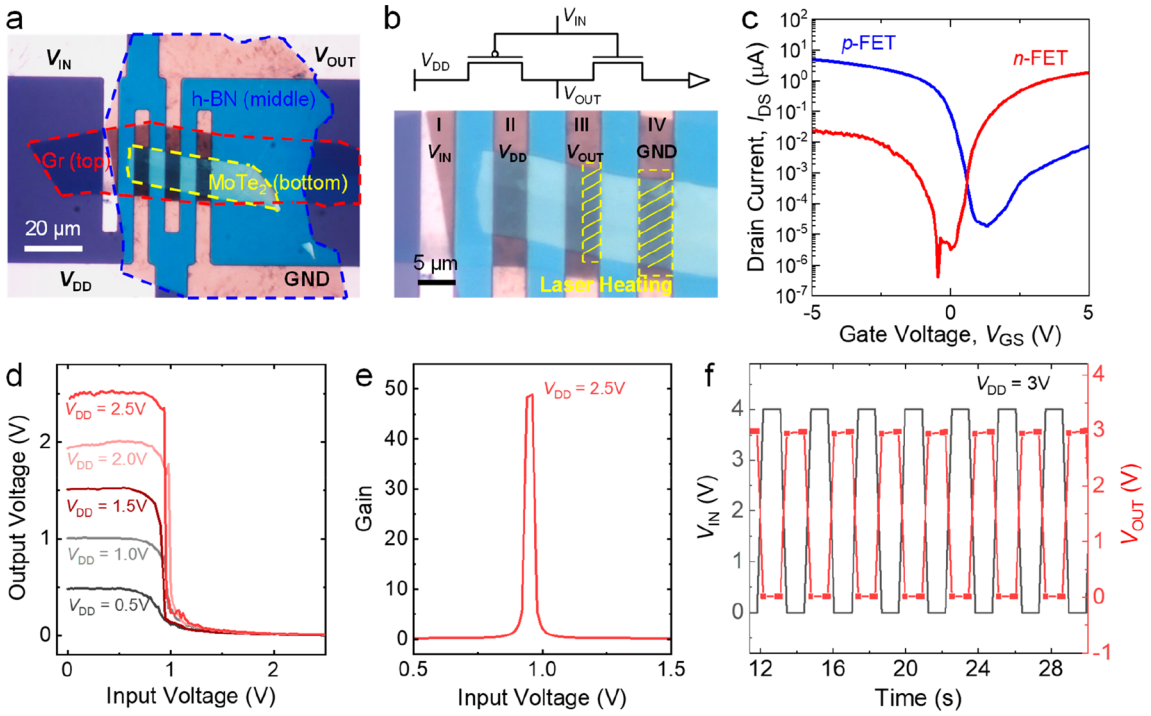

Figure 5. Monolithic $MoTe_2$ inverter and its measured performance, enabled by complementary FETs configured by scanning focused laser annealing. (a) Optical microscopy image of the $MoTe_2$ inverter consisting of a $MoTe_2$ channel, an h-BN dielectric, and a Gr top gate. (b) Inverter circuit scheme and detailed view of the electrodes with highlighted regions (hatched) scanned by a 785 nm laser, which has converted one initial p-FET into an n-FET. (c) I_D−V_{GS} characteristics measured from the p-FET (blue curve) and the n-FET (red curve). (d) Voltage transfer characteristics (VTC) of a $MoTe_2$ complementary inverter at different supply voltages of V_{DD} = 0.5, 1, 1.5, 2, and 2.5 V. (e) Small-signal voltage gain ($g = -dV_{OUT}/dV_{IN}$) measured from the inverters is as high as g = 48 obtained at V_{DD} = 2.5 V. (f) Dynamic switching capability of the inverter. V_{IN} is a square wave signal with minimum and maximum values of 0 and 4 V, and it causes the output voltage to oscillate synchronously with a phase difference of π at V_{DD} of 3 V.

$MoTe_2$ on SiO_2 has no XPS peak shift after laser annealing (Figure 4d). The decrease in the binding energy after the treatment implies a corresponding change in the $MoTe_2$−Au interface. It has been reported that laser annealing treatment can induce shifted Raman and XPS peaks of $MoTe_2$.[36] The spectroscopic changes have emerged at the $MoTe_2$−Au contacts upon focused laser annealing, validating the interaction or alloying of $MoTe_2$ and Au at their interface.

Furthermore, *in situ* Raman spectroscopy is performed to measure the temperature dependence of the $MoTe_2$−Au characteristics under different laser power. The $MoTe_2$ on Au undergoes heating by using a 785 nm laser in a power range of 0 to 13.2 mW. A green laser (532 nm, 0.15 mW) is also focused on the same spot for Raman measurement. Supplementary Figure S12(a) shows that the Raman peak shifts as a function of the laser power and with varying number of layers (thickness) of $MoTe_2$, as extracted from Supplementary Figure S12(b−g). The absolute value of the Raman shift of the bulk $MoTe_2$ increases with the heating laser power (at λ = 785 nm). When the laser power is 13.2 mW, the Raman shift of the bulk $MoTe_2$ reaches −1.6 cm^{-1}. The temperature of the bulk $MoTe_2$ is calculated to be ∼141 °C under the laser annealing with a power of 13.2 mW. However, we find that the 1L $MoTe_2$ flake has almost no Raman shift under different laser powers, which is not in agreement with the temperature-dependence characteristic of $MoTe_2$.[49] Thinner $MoTe_2$ shows less Raman shift over the laser power. Therefore, the *in situ* Raman measurement further suggests that there occurs an alloying interaction between the 1L $MoTe_2$ and the Au electrode during laser annealing that induces the right shift of the Raman peak, in competition with the heating-induced left shift of the Raman peak. Furthermore, in Supplementary Figure S13, the Raman shift of the multilayer $MoTe_2$ sample on Au is reversed when the heating laser spot is removed, while there is almost no Raman shift for 1L $MoTe_2$ on Au under the same conditions. This further indicates the alloying interaction between the 1L $MoTe_2$ and the Au electrode during the laser annealing.

Monolithic Logic Gate Demonstrations by Utilizing the Polarity Control. Next, the transistor polarity change by laser annealing is exploited to enable a $MoTe_2$ complementary inverter, monolithically on a single $MoTe_2$ flake. Figure 5a shows an optical microscopy image of the dual-gate $MoTe_2$ complementary inverter. The van der Waals heterostructure of the inverter consists of Gr (top) as the top gate, h-BN (middle) as the dielectric, and $MoTe_2$ (bottom) as the channel for both p-type and n-type FETs. As shown in Figure 5b, the electrode I connects with the Gr flake as V_{IN}, and V_{DD} is applied to electrode II. The right half part of the electrode III (as V_{OUT}) and the electrode IV (as ground, GND) are illuminated by the focused laser probe (785 nm, 13.2 mW). As depicted in Figure 5c, after laser annealing on the electrodes, the channel between electrodes II and III (II−III channel) maintains p-type conduction and the channel between electrodes III and IV (III−IV channel) switches to n-type conduction. Transfer characteristics of both FETs display a high On/Off current ratio of ∼10^6. The transfer characteristics of the p-FET exhibit excellent repeatability and thermal stability (Supplementary Figure S14).

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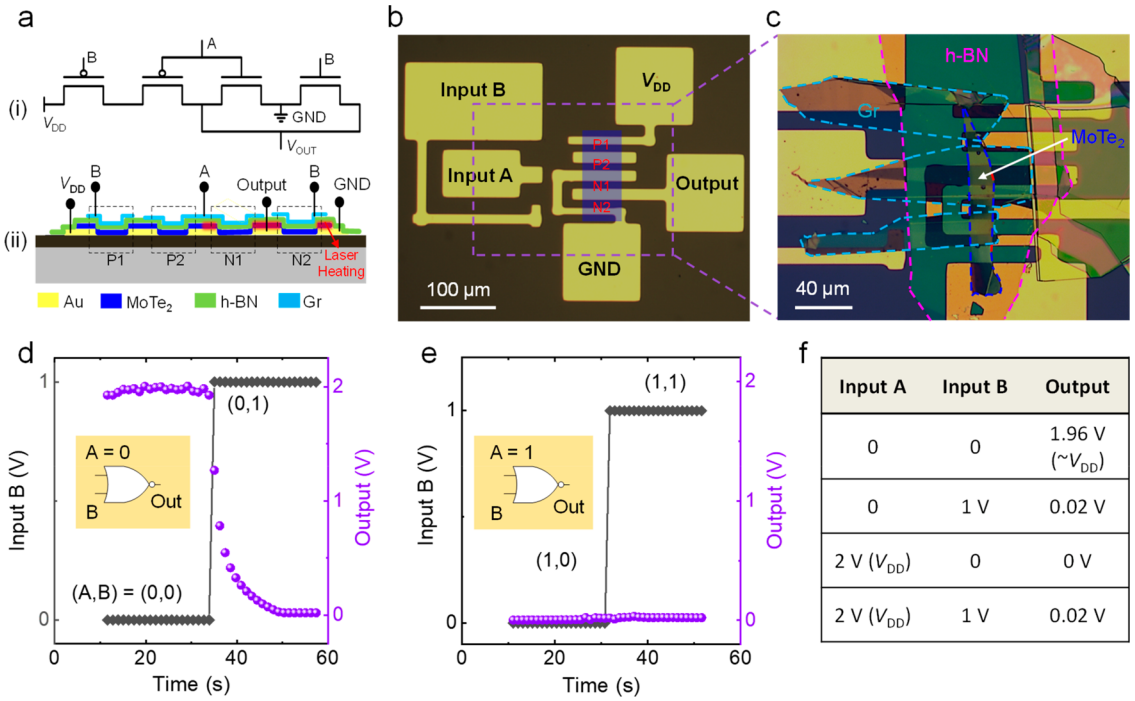

Input A	Input B	Output
0	0	1.96 V (~V_{DD})
0	1 V	0.02 V
2 V (V_{DD})	0	0 V
2 V (V_{DD})	1 V	0.02 V

Figure 6. Monolithic $MoTe_2$ complementary NOR logic circuit and measured performance. (a) (i) NOR logic circuit; (ii) cross-section schematic of a $MoTe_2$ complementary NOR logic composed of two p-FETs in series and two n-FETs in parallel. (b) Optical microscopy image of the predefined electrodes for the NOR circuit. (c) Optical microscopy image of the NOR circuit with three stacking layers: three Gr flakes (top), one large-area h-BN flake (middle), and one $MoTe_2$ flake (bottom). (d) Time domain outputs of the NOR logic, measured with the input of (0,0) and (0,1). (e) Time domain outputs of the NOR logic with the input of (1,0) and (1,1). (f) Measured truth table of the NOR logic circuit.

An inverter is a "NOT" logic gate whose output presents the opposite logic level to its input. Clear inverter operation is observed in Figure 5d for switching between logic "1" (~V_{DD}) and logic "0" (0 V). When V_{IN} is at V_{DD} (logic state "1"), the n-FET is turned on and thus V_{OUT} decreases to near 0 V (logic state "0"). When V_{IN} is pulled down to zero (logic state "0"), V_{OUT} is approaching the supply voltage V_{DD} (logic state "1"), indicative of the complete input/output signal inversion. The slope of the transition region in the middle (*e.g.*, at the intercept with $V_{OUT} = V_{IN}$ curve) provides the measurement of the small signal voltage gain (defined as $g = -dV_{OUT}/dV_{IN}$), which presents the responsivity of V_{OUT} to the variation in V_{IN}. The highest small-signal voltage gain of ~48 is achieved under a supply voltage (V_{DD}) of 2.5 V, as shown in Figure 5e. The inverter is switched by a square waveform of voltage applied to the gate, which causes the output voltage to oscillate synchronously with a phase difference of π, as shown in Figure 5f. V_{IN} is a square wave signal with minimum and maximum values of 0 and 4 V. Similar rectification dynamics have been observed at higher frequencies of 1 kHz and 10 kHz, as shown in Supplementary Figure S15.

Finally, we construct a logic NOR circuit monolithically on a $MoTe_2$ flake including two p-FETs in series and two n-FETs in parallel as shown in Figure 6a. Unlike previous studies, *i.e.*, ternary inverters based on a MoS_2 n-FET and $MoTe_2$ p-FET[28,50] or a WSe_2-based inverter with different contact metals for p- and n-FETs,[51] here all the FETs only involve $MoTe_2$ and the same contact metal (Au), and the n-type FETs are converted from initial p-FETs by direct laser annealing configuration, on demand. First, the $MoTe_2$ flake is transferred onto prefabricated electrodes as shown in Figure 6b; subsequently, an h-BN layer is transferred on top of the $MoTe_2$ flake and completely covers it; next, three Gr flakes are transferred on top of the h-BN layer to bridge to top-gate electrodes. Figure 6c highlights the van der Waals stacking structure of the NOR circuit. The top gates are designed, and meticulously ensured in delicate heterostructure fabrication, to partially overlap with the S/D electrodes. This overlapping structure aims at maintaining electrostatic gating over the S/D electrodes to manipulate the carrier accumulation throughout the channel and the $MoTe_2$–Au junctions. The two top gates are biased independently, and the back gate is grounded.

The transfer characteristics measured from individual $MoTe_2$ FETs in the NOR circuit are presented in Supplementary Figure S16, with the results of P1 FET as a p-FET, P2 as a p-FET, N1 and N2 as n-FETs. By combining the two p-FETs (P1 and P2) in series and the two n-FETs (N1 and N2) in parallel, a standard monolithic NOR circuit is successfully realized, as shown in the plots of output voltage (V_{out}) *versus* input voltage ($V_{in,A}$ and $V_{in,B}$) in Figure 6d and e. When V_{DD} = 2 V is applied to the source of the P1, input A is fixed at $V_{in,A}$ = 0 V and input B is switched between two voltages of $V_{in,B}$ = 0 and 1 V, and the output shows the opposite state of $V_{in,B}$ (Figure 6d). When input A is fixed at $V_{in,A}$ = 2 V and input B is switched between two voltages of $V_{in,B}$ = 0 and 1 V, the output maintains near 0 V (Figure 6e). This monolithic complementary $MoTe_2$ circuit precisely follows the NOR logic ($\overline{A + B}$) and the two logic states (1 and 0) are clearly observed. The data summarized in the experimental truth table (Figure 6f) demonstrates that the NOR logic computation is realized on a single $MoTe_2$ flake. The implementation of this NOR circuit again clearly demonstrates the localized laser annealing method is highly

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effective and nimble for configuring and realizing monolithic 2D integrated circuits.

CONCLUSIONS

In summary, we have developed a doping-free method to spatially configure transport polarity of SB FETs by localized scanning laser annealing and modification of the SB height, thus empowering both p-type and n-type FETs on the same $MoTe_2$ thin film monolithically and on demand. This approach is independent of the initial doping of the channel material. The n-FETs are converted from p-FETs, and high On/Off current ratios of 10^6 and high mobilities up to 96.5 $cm^2 V^{-1} s^{-1}$ have been achieved. Spectroscopic studies on monolayer $MoTe_2$ alloying interaction with Au electrodes at their contacts directly validate signatures of $MoTe_2$–Au, and its SB height modification is confirmed by temperature-dependent drain current measurements and first-principle calculations by using DFT computation. Further, the polarity change method is applied to multiple transistors with designed logic functions, to realize monolithic $MoTe_2$ complementary, high-gain inverters, and NOR circuits. This agile, localized, highly precise transistor polarity change method shall allow us to rationally configure 2D FETs and arrays into large-scale integrated circuits with increasing complexity and functionality.

METHODS

Device Fabrication. $MoTe_2$ flakes are exfoliated from 2H-$MoTe_2$ bulk crystal (HQ Graphene) onto PF films (Gel-Pak) glued on a glass slide and then transferred to the silicon oxide on a silicon (290 nm SiO_2 on Si) substrate with prefabricated gold (Au) electrodes upon inspection under the optical microscope. It is noted that the flakes are carefully aligned with Au electrodes. During the transfer, it is also necessary to keep a very small angle between the flake and the chip in order not to trap bubbles between the flake and the substrate. The flake thickness ranges from monolayer to 12 nm. The flake thickness is confirmed by Raman and/or atomic force microscopy (AFM). The electrodes are patterned on the SiO_2-on-Si substrate using photolithography and Au deposition. The Au thickness is 30 nm, and the adhesive Cr thickness is 5 nm. Chips with S/D electrodes are diced from such a wafer and are sonicated in acetone and isopropyl alcohol (IPA) and dried using a N_2 gun. The second transfer step is started by exfoliating h-BN flakes from h-BN bulk crystal (HQ Graphene). The shape and size of the h-BN flake are carefully chosen, to ensure complete encapsulation of the $MoTe_2$ flake. The wavelength of the laser for heating is 785 nm, and the laser power is set to 0.6, 1.5, 3, 6, 9, 12, or 13.2 mW. The spot size of the laser is calibrated to be 1 μm, and the laser is scanned on the $MoTe_2$–Au contacts. The scan rate is 1 μm/step, and the delay time of each step is 10 s. Each area is scanned three times with the same condition.

Material Characterization. AFM imaging is performed using an Agilent N9610A AFM in the tapping mode. Raman spectroscopy is performed using a customized micro-Raman system. Raman spectra of $MoTe_2$ flakes are measured in vacuum (~10 mTorr) at room temperature using a 532 nm green laser at different laser power levels. The $MoTe_2$–Au contact is heated by the 785 nm laser at a power range from 0.6 to 13.2 mW. A green laser (532 nm, 0.15 mW) is focused on the same spot to measure *in situ* Raman spectra. EDS is measured using an XEDS and EBSD Oxford system (X-Max 50 mm^2 EDS, Nordlys high-resolution EBSD) that is integrated into the SEM system (FEI Nova NanoLab 200).

Density Functional Theory (DFT) Calculations. The simulations of the Au–$MoTe_2$ interface are conducted by DFT with the Vienna *ab initio* simulation package (VASP) codes. The generalized gradient approximation (GGA) method is used with the Perdew–Burke–Ernzerhof (PBE) exchange–correlation functional. The Brillouin zone is sampled by the 10 × 10 × 1 Monkhorst–Pack scheme. The cutoff energy for the wave function expansion is set to 400 eV. The total local potential is set to contain the entire local potential including the ionic, Hartree, and exchange–correlation potential. The structure of the supercell for VASP simulation contains trilayer Au and monolayer $MoTe_2$ or $AuTe_2$ to form the interface of Au–$MoTe_2$. The total energy of supercells achieves the minimum value by adjusting the distance between Au and $MoTe_2$/$AuTe_2$. The vacuum energy level and Fermi energy level are both acquired from simulation results, and the difference of energy reveals the work function of the Au–$MoTe_2$ interface. Given the *ab initio* computation results, the electron wave function probability density is plotted and visualized by using XcrySDen.

Electrical Measurement. All the measurements of the electronic characteristics are performed in the dark at room temperature using a parameter analyzer (Keithley 4200A-SCS) and a customized probe station. For the high-frequency measurement, a high-precision mixed signal oscilloscope (model: MSO54, Tektronix) and an arbitrary function generator (model: AFG31102, Tektronix) are used.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.1c07169.

Wide-range Raman spectrum and thickness of the dual-gate $MoTe_2$ FET; analysis of V_{Min} of the dual-gate $MoTe_2$ FET before and after laser annealing; analysis of contact resistance; analysis of hysteresis effect; EDS analysis of $MoTe_2$ before and after laser annealing; extraction of Schottky barrier height; DFT calculations on the $MoTe_2$–Au interface with different atomic distances; control experiment with laser only illuminating on the channel; control experiment with different contact metals; 1L $MoTe_2$ flake and its Raman spectrum; surface topography images of $MoTe_2$ FET before and after laser annealing; estimation of laser annealing temperature; comparison of Raman of $MoTe_2$ on Au and $MoTe_2$ on SiO_2 before and after laser annealing; stability of p-type FET in the inverter; cycling performance of the $MoTe_2$ inverter; transistor performance of the NOR logic circuit (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Jariwala, D.; Sangwan, V. K.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano* **2014**, *8* (2), 1102−1120.
(2) Liu, Y.; Duan, X.; Shin, H.-J.; Park, S.; Huang, Y.; Duan, X. Promises and Prospects of Two-Dimensional Transistors. *Nature* **2021**, *591*, 43−53.
(3) Jeon, P. J.; Kim, J. S.; Lim, J. Y.; Cho, Y.; Pezeshki, A.; Lee, H. S.; Yu, S.; Min, S.-W.; Im, S. Low Power Consumption Complementary Inverters with *n*-MoS_2 and *p*-WSe_2 Dichalcogenide Nanosheets on Glass for Logic and Light-Emitting Diode Circuits. *ACS Appl. Mater. Interfaces* **2015**, *7* (40), 22333−22340.
(4) Larentis, S.; Fallahazad, B.; Movva, H. C. P.; Kim, K.; Rai, A.; Taniguchi, T.; Watanabe, K.; Banerjee, S. K.; Tutuc, E. Reconfigurable Complementary Monolayer $MoTe_2$ Field-Effect Transistors for Integrated Circuits. *ACS Nano* **2017**, *11* (5), 4832−4839.
(5) Eftekhari, A. Tungsten Dichalcogenides (WS_2, WSe_2, and WTe_2): Materials Chemistry and Applications. *J. Mater. Chem. A* **2017**, *5* (35), 18299−18325.
(6) Hu, Z.; Wu, Z.; Han, C.; He, J.; Ni, Z.; Chen, W. Two-Dimensional Transition Metal Dichalcogenides: Interface and Defect Engineering. *Chem. Soc. Rev.* **2018**, *47* (9), 3100−3128.
(7) Gong, Y.; Yuan, H.; Wu, C.-L.; Tang, P.; Yang, S.-Z.; Yang, A.; Li, G.; Liu, B.; van de Groep, J.; Brongersma, M. L.; Chisholm, M. F.; Zhang, S.-C.; Zhou, W.; Cui, Y. Spatially Controlled Doping of Two-Dimensional SnS_2 through Intercalation for Electronics. *Nat. Nanotechnol.* **2018**, *13* (4), 294−299.
(8) Lim, J. Y.; Pezeshki, A.; Oh, S.; Kim, J. S.; Lee, Y. T.; Yu, S.; Hwang, D. K.; Lee, G.-H.; Choi, H. J.; Im, S. Homogeneous 2D $MoTe_2$ *p-n* Junctions and CMOS Inverters Formed by Atomic-Layer-Deposition-Induced Doping. *Adv. Mater.* **2017**, *29* (30), 1701798.
(9) Yang, L.; Majumdar, K.; Liu, H.; Du, Y.; Wu, H.; Hatzistergos, M.; Hung, P. Y.; Tieckelmann, R.; Tsai, W.; Hobbs, C.; Ye, P. D. Chloride Molecular Doping Technique on 2D Materials: WS_2 and MoS_2. *Nano Lett.* **2014**, *14* (11), 6275−6280.
(10) Zhang, X.; Shao, Z.; Zhang, X.; He, Y.; Jie, J. Surface Charge Transfer Doping of Low-Dimensional Nanostructures toward High-Performance Nanodevices. *Adv. Mater.* **2016**, *28* (47), 10409−10442.
(11) Luo, W.; Zhu, M.; Peng, G.; Zheng, X.; Miao, F.; Bai, S.; Zhang, X.-A.; Qin, S. Carrier Modulation of Ambipolar Few-Layer $MoTe_2$ Transistors by MgO Surface Charge Transfer Doping. *Adv. Funct. Mater.* **2018**, *28* (15), 1704539.
(12) Liu, T.; Xiang, D.; Zheng, Y.; Wang, Y.; Wang, X.; Wang, L.; He, J.; Liu, L.; Chen, W. Nonvolatile and Programmable Photodoping in $MoTe_2$ for Photoresist-Free Complementary Electronic Devices. *Adv. Mater.* **2018**, *30* (52), 1804470.
(13) Wu, E.; Xie, Y.; Zhang, J.; Zhang, H.; Hu, X.; Liu, J.; Zhou, C.; Zhang, D. Dynamically Controllable Polarity Modulation of $MoTe_2$ Field-Effect Transistors through Ultraviolet Light and Electrostatic Activation. *Sci. Adv.* **2019**, *5* (5), eaav3430.
(14) Chang, Y.-M.; Yang, S.-H.; Lin, C.-Y.; Chen, C.-H.; Lien, C.-H.; Jian, W.-B.; Ueno, K.; Suen, Y.-W.; Tsukagoshi, K.; Lin, Y.-F. Reversible and Precisely Controllable *p*/*n*-Type Doping of $MoTe_2$ Transistors through Electrothermal Doping. *Adv. Mater.* **2018**, *30* (13), 1706995.
(15) Seo, S.-Y.; Park, J.; Park, J.; Song, K.; Cha, S.; Sim, S.; Choi, S.-Y.; Yeom, H. W.; Choi, H.; Jo, M.-H. Writing Monolithic Integrated Circuits on a Two-Dimensional Semiconductor with a Scanning Light Probe. *Nat. Electron.* **2018**, *1* (9), 512−517.
(16) Chen, J.; Zhu, J.; Wang, Q.; Wan, J.; Liu Chen, R. J.; Zhu, J.; Wang, Q.; Wan, J.; Liu, R. Homogeneous 2D $MoTe_2$ CMOS Inverters and *p-n* Junctions Formed by Laser-Irradiation-Induced *p*-Type Doping. *Small* **2020**, *16* (30), 2001428.
(17) Ke, Y.; Song, X.; Qi, D.; Liu, J.; Hao, Q.; Wang, Z.; Tang, S.; Zhang, W. Modulation of Electrical Properties with Controllable Local Doping in Multilayer $MoTe_2$ Transistors. *Adv. Electron. Mater.* **2020**, *6* (10), 2000532.
(18) Aftab, S.; Yousuf, S.; Usman Khan, M.; Khawar, R.; Younus, A.; Manzoor, M.; Waqas Iqbal, M.; Zahir Iqbal, M. Carrier Polarity Modulation of Molybdenum Ditelluride ($MoTe_2$) for Phototransistor and Switching Photodiode Applications. *Nanoscale* **2020**, *12*, 15687.
(19) Aftab, S.; Samiya, M.; Raza, A.; Waqas Iqbal, M.; Mansoor, H.; Haque, U.; Ramachandraiah, K.; Yousuf, S.; Jun, S. C.; Rehman, A. U.; Iqbal, M. Z. A Reversible and Stable Doping Technique to Invert the Carrier Polarity of $MoTe_2$. *Nanotechnology* **2021**, *32*, 285701.
(20) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13* (1), 100−105.
(21) Chen, J.-R.; Odenthal, P. M.; Swartz, A. G.; Floyd, G. C.; Wen, H.; Luo, K. Y.; Kawakami, R. K. Control of Schottky Barriers in Single Layer MoS_2 Transistors with Ferromagnetic Contacts. *Nano Lett.* **2013**, *13* (7), 3106−3110.
(22) Liu, X.; Islam, A.; Guo, J.; Feng, P. X.-L. Controlling Polarity of $MoTe_2$ Transistors for Monolithic Complementary Logic *via* Schottky Contact Engineering. *ACS Nano* **2020**, *14* (2), 1457−1467.
(23) Nakaharai, S.; Yamamoto, M.; Ueno, K.; Tsukagoshi, K. Carrier Polarity Control in α-$MoTe_2$ Schottky Junctions Based on Weak Fermi-Level Pinning. *ACS Appl. Mater. Interfaces* **2016**, *8* (23), 14732−14739.
(24) Qu, D.; Liu, X.; Huang, M.; Lee, C.; Ahmed, F.; Kim, H.; Ruoff, R. S.; Hone, J.; Yoo, W. J. Carrier-Type Modulation and Mobility Improvement of Thin $MoTe_2$. *Adv. Mater.* **2017**, *29* (39), 1606433.
(25) Ji, H.; Joo, M.-K.; Yi, H.; Choi, H.; Gul, H. Z.; Ghimire, M. K.; Lim, S. C. Tunable Mobility in Double-Gated $MoTe_2$ Field-Effect Transistor: Effect of Coulomb Screening and Trap Sites. *ACS Appl. Mater. Interfaces* **2017**, *9* (34), 29185−29192.
(26) Sung, J. H.; Heo, H.; Si, S.; Kim, Y. H.; Noh, H. R.; Song, K.; Kim, J.; Lee, C.-S.; Seo, S.-Y.; Kim, D.-H.; Kim, H. K.; Yeom, H. W.; Kim, T.-H.; Choi, S.-Y.; Kim, J. S.; Jo, M.-H. Coplanar Semiconductor-Metal Circuitry Defined on Few-Layer $MoTe_2$ *via* Polymorphic Heteroepitaxy. *Nat. Nanotechnol.* **2017**, *12* (11), 1064−1070.
(27) Afzal, A. M.; Iqbal, M. Z.; Dastgeer, G.; Ahmad, A. ul; Park, B. Highly Sensitive, Ultrafast, and Broadband Photo-Detecting Field-Effect Transistor with Transition-Metal Dichalcogenide van der Waals Heterostructures of $MoTe_2$ and $PdSe_2$. *Adv. Sci.* **2021**, *8* (11), 2003713.
(28) Pezeshki, A.; Shokouh, S. H. H.; Nazari, T.; Oh, K.; Im, S. Electric and Photovoltaic Behavior of a Few-Layer α-$MoTe_2$ /MoS_2 Dichalcogenide Heterojunction. *Adv. Mater.* **2016**, *28* (16), 3216−3222.

(29) Lee, H. S.; Choi, K.; Kim, J. S.; Yu, S.; Ko, K. R.; Im, S. Coupling Two-Dimensional $MoTe_2$ and InGaZnO Thin-Film Materials for Hybrid PN Junction and CMOS Inverters. *ACS Appl. Mater. Interfaces* **2017**, *9* (18), 15592−15598.
(30) Pezeshki, A.; Hosseini Shokouh, S. H.; Jeon, P. J.; Shackery, I.; Kim, J. S.; Oh, I. K.; Jun, S. C.; Kim, H.; Im, S. Static and Dynamic Performance of Complementary Inverters Based on Nanosheet α-$MoTe_2$ *p*-Channel and MoS_2 *n*-Channel Transistors. *ACS Nano* **2016**, *10* (1), 1118−1125.
(31) Choi, K.; Lee, Y. T.; Kim, J. S.; Min, S. W.; Cho, Y.; Pezeshki, A.; Hwang, D. K.; Im, S. Non-Lithographic Fabrication of All-2D α-$MoTe_2$ Dual Gate Transistors. *Adv. Funct. Mater.* **2016**, *26* (18), 3146−3153.
(32) Chen, J.; Feng, Z.; Fan, S.; Shi, S.; Yue, Y.; Shen, W.; Xie, Y.; Wu, E.; Sun, C.; Liu, J.; Zhang, H.; Pang, W.; Sun, D.; Feng, W.; Feng, Y.; Wu, S.; Zhang, D. Contact Engineering of Molybdenum Ditelluride Field Effect Transistors through Rapid Thermal Annealing. *ACS Appl. Mater. Interfaces* **2017**, *9* (35), 30107−30114.
(33) Cho, Y.; Park, J. H.; Kim, M.; Jeong, Y.; Yu, S.; Lim, J. Y.; Yi, Y.; Im, S. Impact of Organic Molecule-Induced Charge Transfer on Operating Voltage Control of Both *n*-MoS_2 and *p*-$MoTe_2$ Transistors. *Nano Lett.* **2019**, *19* (4), 2456−2463.
(34) Ke, Y.; Qi, D.; Han, C.; Liu, J.; Zhu, J.; Xiang, Y.; Zhang, W. Facile *p*-Doping of Few-Layer $MoTe_2$ by Controllable Surface Oxidation toward High-Performance Complementary Devices. *ACS Appl. Electron. Mater.* **2020**, *2* (4), 920−926.
(35) Pradhan, N. R.; Rhodes, D.; Feng, S.; Xin, Y.; Memaran, S.; Moon, B. H.; Terrones, H.; Terrones, M.; Balicas, L. Field-Effect Transistors Based on Few-Layered α-$MoTe_2$. *ACS Nano* **2014**, *8* (6), 5911−5920.
(36) Cho, S.; Kim, S.; Kim, J. H.; Zhao, J.; Seok, J.; Keum, D. H.; Baik, J.; Choe, D.-H.; Chang, K. J.; Suenaga, K.; Kim, S. W.; Lee, Y. H.; Yang, H. Phase Patterning for Ohmic Homojunction Contact in $MoTe_2$. *Science* **2015**, *349* (6248), 625−628.
(37) Iqbal, M. W.; Elahi, E.; Amin, A.; Aftab, S.; Aslam, I.; Hussain, G.; Shehzad, M. A. A Facile Route to Enhance the Mobility of $MoTe_2$ Field Effect Transistor *via* Chemical Doping. *Superlattices Microstruct.* **2020**, *147*, 106698.
(38) Amit, I.; Octon, T. J.; Townsend, N. J.; Reale, F.; Wright, C. D.; Mattevi, C.; Craciun, M. F.; Russo, S. Role of Charge Traps in the Performance of Atomically Thin Transistors. *Adv. Mater.* **2017**, *29* (19), 1605598.
(39) Li, S.-L.; Wakabayashi, K.; Xu, Y.; Nakaharai, S.; Komatsu, K.; Li, W.-W.; Lin, Y.-F.; Aparecido-Ferreira, A.; Tsukagoshi, K. Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors. *Nano Lett.* **2013**, *13* (8), 3546−3552.
(40) Roy, A.; Movva, H. C. P.; Satpati, B.; Kim, K.; Dey, R.; Rai, A.; Pramanik, T.; Guchhait, S.; Tutuc, E.; Banerjee, S. K. Structural and Electrical Properties of $MoTe_2$ and $MoSe_2$ Grown by Molecular Beam Epitaxy. *ACS Appl. Mater. Interfaces* **2016**, *8* (11), 7396−7402.
(41) Zhu, H.; Wang, Q.; Cheng, L.; Addou, R.; Kim, J.; Kim, M. J.; Wallace, R. M. Defects and Surface Structural Stability of $MoTe_2$ under Vacuum Annealing. *ACS Nano* **2017**, *11* (11), 11005−11014.
(42) Chen, B.; Sahin, H.; Suslu, A.; Ding, L.; Bertoni, M. I.; Peeters, F. M.; Tongay, S. Environmental Changes in $MoTe_2$ Excitonic Dynamics by Defects-Activated Molecular Interaction. *ACS Nano* **2015**, *9* (5), 5326−5332.
(43) Qi, D.; Wang, Q.; Han, C.; Jiang, J.; Zheng, Y.; Chen, W.; Zhang, W.; Wee, A. T. S. Reducing the Schottky Barrier between Few-Layer $MoTe_2$ and Gold. *2D Mater.* **2017**, *4* (4), 045016.
(44) Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Approaching the Schottky−Mott Limit in van der Waals Metal-Semiconductor Junctions. *Nature* **2018**, *557* (7707), 696−700.
(45) Islam, A.; Feng, P. X. L. Effects of Asymmetric Schottky Contacts on Photoresponse in Tungsten Diselenide (WSe_2) Phototransistor. *J. Appl. Phys.* **2017**, *122* (8), 085704.
(46) Kang, J.; Liu, W.; Banerjee, K. High-Performance MoS_2 Transistors with Low-Resistance Molybdenum Contacts. *Appl. Phys. Lett.* **2014**, *104* (9), 093106.
(47) Islam, A.; Lee, J.; Feng, P. X.-L. All-Dry Transferred Single- and Few-Layer MoS_2 Field Effect Transistor with Enhanced Performance by Thermal Annealing. *J. Appl. Phys.* **2018**, *123* (2), 025701.
(48) Kang, J.; Liu, W.; Sarkar, D.; Jena, D.; Banerjee, K. Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors. *Phys. Rev. X* **2014**, *4* (3), 031005.
(49) Park, J.; Kim, Y.; Jhon, Y. I.; Jhon, Y. M. Temperature Dependent Raman Spectroscopic Study of Mono-, Bi-, and Tri-Layer Molybdenum Ditelluride. *Appl. Phys. Lett.* **2015**, *107* (15), 153106.
(50) Cheng, R.; Wang, F.; Yin, L.; Wang, Z.; Wen, Y.; Shifa, T. A.; He, J. High-Performance, Multifunctional Devices Based on Asymmetric van der Waals Heterostructures. *Nat. Electron.* **2018**, *1* (6), 356−361.
(51) Das, S.; Dubey, M.; Roelofs, A. High Gain, Low Noise, Fully Complementary Logic Inverter Based on Bi-Layer WSe_2 Field Effect Transistors. *Appl. Phys. Lett.* **2014**, *105* (8), 083511.

https://doi.org/10.1021/acsnano.1c07169
ACS Nano 2021, 15, 19733−19742