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Hexagonal boron nitride (h-BN) memristor arrays for analog-based machine learning hardware

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Recent studies of resistive switching devices with hexagonal boron nitride (h-BN) as the switching layer have shown the potential of two-dimensional (2D) materials for memory and neuromorphic computing applications. The use of 2D materials allows scaling the resistive switching layer thickness to sub-nanometer dimensions enabling devices to operate with low switching voltages and high programming speeds, offering large improvements in efficiency and performance as well as ultra-dense integration. These characteristics are of interest for the implementation of neuromorphic computing and machine learning hardware based on memristor crossbars. However, existing demonstrations of h-BN memristors focus on single isolated device switching properties and lack attention to fundamental machine learning functions. This paper demonstrates the hardware implementation of dot product operations, a basic analog function ubiquitous in machine learning, using h-BN memristor arrays. Moreover, we demonstrate the hardware implementation of a linear regression algorithm on h-BN memristor arrays.

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INTRODUCTION

Two-dimensional (2D) materials have attracted significant interest for the downscaling of CMOS (complementary metal-oxide-semiconductor)^{1–3}, as well as for beyond-CMOS electronic applications^{4,5}. Their atomic scale thicknesses and pristine (i.e., dangling-bond free) surfaces could enable ultra-dense integration for next-generation integrated electronic systems⁵. Consequently, many studies have evolved from the demonstration of isolated devices (e.g., field effect transistors or FETs) based on exfoliated flakes towards large-area methods for fabrication of integrated circuits with 2D materials^{6–12}. While early device demonstrations focused predominantly on FET applications^{13–16}, recent studies have proposed memory and neuromorphic devices based on the non-volatile resistive-switching (NVRs) behavior observed in various 2D materials including transition metal dichalcogenides (TMDC)¹⁷, black-phosphorus^{18,19}, graphene^{20,21}, hexagonal boron nitride (h-BN)^{22–30}, etc. These devices are generally configured in vertical two-terminal structures, where the resistive switching layer is sandwiched between top and bottom metal electrodes. The use of 2D materials has enabled the demonstration of devices with atomically thin resistive switching layers having low voltage operation²⁷ and fast switching speeds^{23,24}. Chemical vapor deposition (CVD)-grown h-BN has attracted much attention for use as the resistive switching layer due to its compatibility with large-area wafer-scale fabrication, and arrays of h-BN memristors have been reported¹¹. In CVD-grown h-BN devices the resistive switching process is attributed to the formation and rupture of conductive paths via penetration of metal ions into defects at h-BN grain boundaries.

Initial studies of h-BN memristors reported on their non-volatile resistive switching behavior observed as transitions or hysteresis in measurements of DC current–voltage characteristics^{23,24,27,29}. Previous work¹¹ has also shown the programming of multiple resistive states in h-BN memristors by the application of consecutive voltage pulses, although using significantly larger pulse widths (milliseconds) compared to what is reported here (nanoseconds). Pulsed programming is required for practical

memory and neuromorphic computing applications. Moreover, the pulsed programming of multiple conductive states is critical for the implementation of synaptic plasticity (i.e., long-term potentiation and depression) in neuromorphic hardware, as well as for the analog-based implementation of machine learning functions in memristor arrays^{31,32}. For example, most analog-based implementations of neural networks and/or machine learning hardware based on memristor crossbars rely on dot-product (i.e., multiply-accumulate) operations^{33–35}. Here, the accumulated currents at the outputs of the array result from the product of input voltage signals (input vector) and the conductance of the memristors in the array (column vectors). Nevertheless, this basic function has not been reported in arrays of h-BN memristors.

This paper presents the wafer-scale fabrication of memristor arrays using on CVD-grown h-BN resistive switching layers, and their multi-state analog programmability. We focus on the experimental demonstration of dot-product operation on h-BN memristor arrays and on the hardware implementation of multi-variable stochastic linear regression. This work extends beyond existing demonstrations of NVRs behavior in isolated h-BN memristors and paves the way for more sophisticated demonstrations of machine learning applications based on 2D materials.

RESULTS

Fabrication of h-BN memristor arrays

Multilayer CVD-grown h-BN was transferred from copper onto a 90 nm SiO₂/Si substrate patterned with Au bottom electrodes. The h-BN film was then shaped using standard photolithographic and etching techniques to expose the bottom electrodes. Subsequently, we prepared top electrodes through patterning and Ti deposition using e-beam evaporation and lift-off (see “Methods” and Supplementary Fig. 2 for fabrication details). Figure 1a shows a schematic of the fabricated Au/h-BN/Ti memristors arrays where the Au bottom electrode (BE) is shared across various devices each having an independent Ti top electrode (TE) (1 × 3 and 1 × 10

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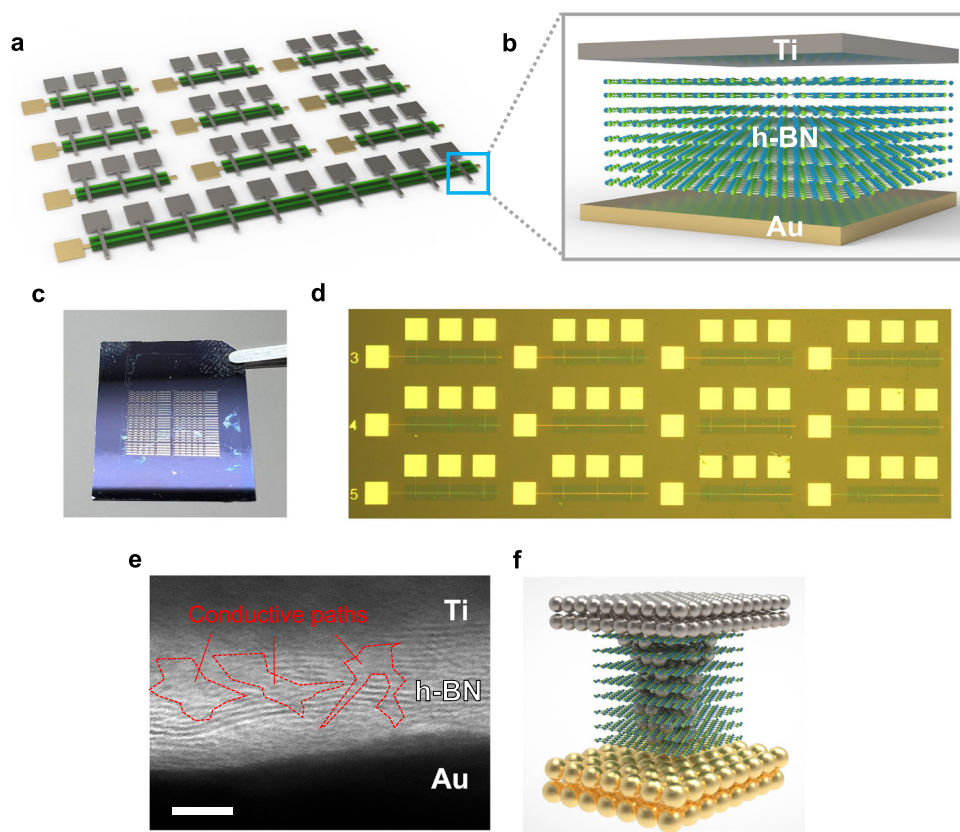


Fig. 1 hexagonal Boron Nitride (h-BN) memristor arrays. **a** Schematic of the Au/h-BN/Ti memristor arrays and **b** cross-sectional schematic of single memristor **c** Photograph of Au/h-BN/Ti memristor arrays on 90 nm SiO₂/Si wafer under ambient light, and **d** micrograph of arrays with 3 μm × 3 μm active areas. **e** Cross-sectional TEM image of the Au/h-BN/Ti memristor indicating local defects responsible for the formation of conductive paths. Scale bar, 5 nm. **f** A representation of conductive nanofilaments on the Au/h-BN/Ti memristors.

arrays are shown). Figure 1b illustrates the cross-section of the Au/h-BN/Ti memristor. Figure 1c is a photograph of the memristor arrays on a 2 cm by 2 cm SiO₂/Si wafer. A micrograph of the fabricated h-BN memristor arrays shown in Fig. 1d corroborates the dimensions of the 100 μm × 100 μm squared pads and the electrodes with 3 μm × 3 μm active areas (see Supplementary Fig. 1 for 20 μm × 20 μm and 50 μm × 50 μm active areas). Figure 1e shows a cross-section transmission electron microscopy (TEM) image of a typical Au/h-BN/Ti memristor. From the TEM image we confirm the thickness of the CVD-grown multilayer h-BN film (~8–10 nm) corresponding to approximately 15–20 atomic layers. Moreover, we can observe local defects that facilitate metallic penetration from the top electrode (Ti) to form conductive paths (i.e., conductive nanofilaments) responsible for the resistive switching behavior in the h-BN memristors.

Resistive-switching properties

Individual h-BN memristors from the arrays were measured electrically to evaluate their resistive-switching properties (see “Methods” for details on electrical characterization). Current–voltage (*I*–*V*) characteristics were obtained by sweeping a voltage across the top and bottom electrodes while measuring current. Figure 2a plots 100 consecutive cycles of *I*–*V* measurements on an Au/h-BN/Ti memristor with a 3 μm × 3 μm active area. A compliance of 0.1 mA was activated for positive applied voltages. The numbered labels indicate the sweeping process during the *I*–*V* measurement. As shown, clear transitions occur between resistive states, evidence of a forming-free bipolar resistive-switching (RS) operation with low cycle-to-cycle resistance variability and low set and reset voltages (approximately 1

and –1 V). The cumulative distribution plot of the resistive states extracted at a read voltage of 0.1 V from all 100 cycles is shown in Fig. 2b. Two distinct states labeled as HRS (high resistance states) and LRS (low resistance state) are easily observed as their distributions are separated by approximately two orders of magnitude. Another illustration of the HRS and LRS distributions is provided in Fig. 2c where the resistances are plotted as a function of the cycle number. A histogram of the set and reset voltages corresponding to transitions between HRS and LRS is shown in Fig. 2d. All results indicate a stable and reliable RS bipolar operation.

We also explore the dependence of the *I*–*V* characteristics and of the HRS and LRS statistics on h-BN memristor active area. In Fig. 2e we compare the *I*–*V* characteristics from devices with 3 μm × 3 μm, 20 μm × 20 μm, and 50 μm × 50 μm active areas. All devices were measured for 100 cycles and the results show good repeatability with limited cycle-to-cycle variation. The difference in active area has a larger effect on the HRS and this is easier to identify in the cumulative distribution plot shown in Fig. 2f. Here, the HRS and LRS resistances are shown for the three devices (all 100 cycles) extracted at a read voltage of 0.1 V. While distributions of LRS are only minimally affected by active area we see a clear trend in HRS. The HRS resistance goes down with increasing the active area. This trend in HRS and LRS with active area has been previously reported for different filamentary-based RS memory^{36,37}. Figure 2g is a box plot showing the distribution of HRS and LRS as a function of cell area side length (3, 20, and 50 μm). The plot includes the raw data (circles), the standard deviation (size of box), and the mean values (solid horizontal lines). We note that while cycle-to-cycle variability is comparable to previous resistive-switching technologies (e.g., oxide-based RRAM³⁸),

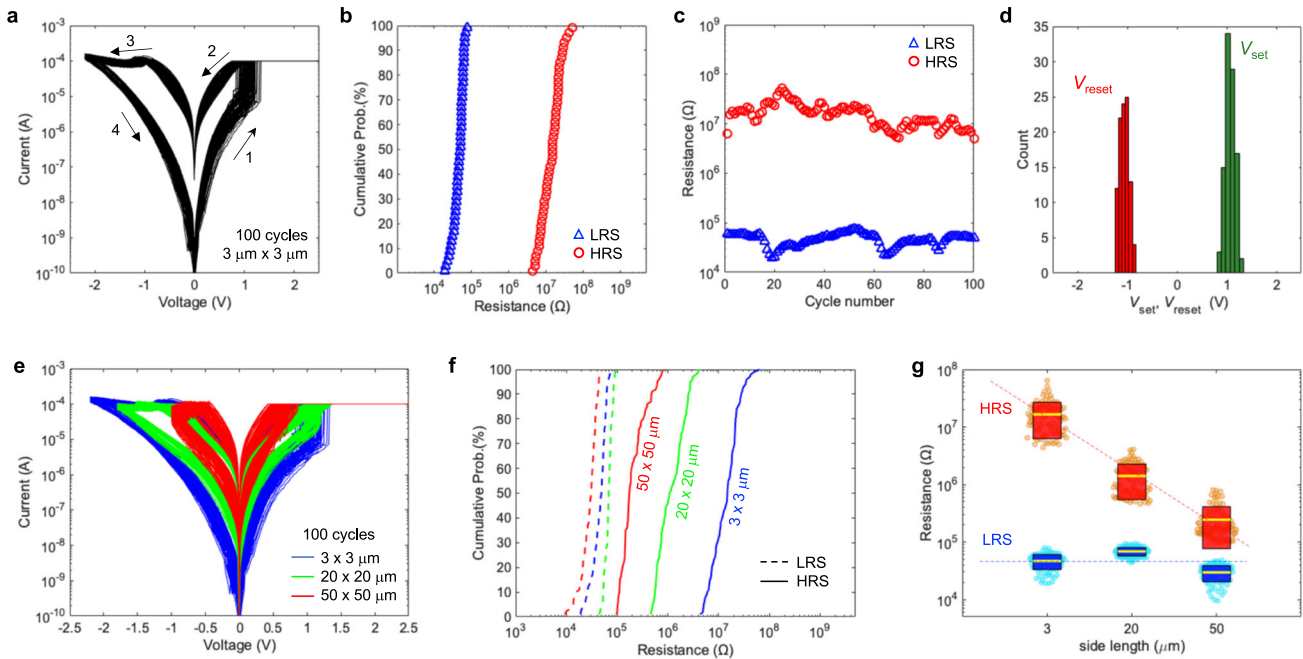


Fig. 2 Resistive switching characteristics of h-BN memristors. **a** Representative I - V characteristics measured during 100 cycles in one single $3\ \mu\text{m} \times 3\ \mu\text{m}$ Au/h-BN/Ti memristor with 0.1 and 1 mA compliance respectively for the positive and negative sides of the sweep. **b** Cumulative probability distribution of the HRS and LRS (read at 0.1 V) **c** resistance vs cycle number plot, and **d** histogram of set and reset voltages. **e** Comparison of 100 I - V cycles from Au/h-BN/Ti memristors with different active areas. **f** Cumulative probability distribution of the HRS and LRS (read at 0.1 V) and **g** statistical analysis of resistance (HRS, LRS) as a function of the active area side length.

device-to-device variability remains large, likely due to nonuniformity of the h-BN film and may be improved by optimizing the synthesis and transfer methods.

Multistate non-volatile pulse programmability

Achieving multiple conductive states through the application of programming pulses is critical for the implementation of neuromorphic hardware and for the analog-based implementation of machine learning functions in memristor arrays. We investigate the multistate pulse programmability of the Au/h-BN/Ti memristors by applying a sequence of positive/negative voltage pulses (pulse width is 500 ns, amplitudes indicated in Fig. 3). After each pulse a small read of 0.1 V is applied to read the current (conductive state) of the device (see Fig. 3a top panel). The results are shown in Fig. 3b, where 100 cycles of 50 positive pulses followed by 50 negative pulses were applied. The gray lines are the results from each individual cycle and the solid red line with circles is the average from all 100 cycles. The results show a gradual change in conductance (from ~ 4 to $10\ \mu\text{S}$) indicating good analog (i.e., multistate) programmability. Due to the fast-switching behavior (nanoseconds), a low energy consumption per programming pulse of $E_{\text{pulse}} = (I)(V)(t_{\text{pulse}}) \approx 125\ \text{fJ}$ is achieved. We note that this can be further reduced to aJ/pulse by applying a low compliance current as previously reported on h-BN memristors¹¹. The non-volatile property of the conductive states is also demonstrated by retention tests where current is sampled over 100 s (read voltage 0.1 V) following the application of the programming pulses (Fig. 3c, d). Figure 3c plots current for different programming cycles where the number of positive pulses was varied from two up to twenty. Immediately after the last positive pulse we apply and hold a 0.1 V read voltage and sample current every second for 100 s (see Fig. 3a bottom panel). After the retention test the negative pulses are applied and we then proceed to the next cycle. The results from the retention test are shown in Fig. 3d where the current is plotted as a function of the retention time (longer retention tests up to $10^4\ \text{s}$ confirming a

stable, non-volatile response are shown in Supplementary Fig. 6). The results confirm the endurance and robustness of the conductive filaments and demonstrate the multistate non-volatile pulse programmability of Au/h-BN/Ti memristors.

Dot product with h-BN memristor arrays

The dot-product operation is crucial for neuromorphic computing and machine learning hardware. For example, a dot-product operation is typically used in neural networks implemented on memristor crossbar arrays to accumulate currents at the outputs (i.e., the post-synaptic neurons). Here, the product of the input voltage signals (the input vector, v) multiply the conductances of the memristor arrays (the column vector, G) to accumulate an output current (I). This is achieved in hardware due to Ohm's and Kirchhoff's laws as given by $I = \sum vG$. This dot-product operation has been previously reported on oxide-based memristors^{34,39}, but not on recently developed h-BN memristor arrays. Here we demonstrate the most basic implementation of dot-product on an array of two h-BN memristors where the accumulated current is given by $I = v_1G_1 + v_2G_2$. The experimental setup is illustrated in Fig. 4a. As shown, for each memristor we can switch between a pulse source (used to program the memristor conductances G_1 , and G_2) and a voltage source to apply the read voltage on the memristors (v_1 , and v_2). During the read operation we measure the output current through the shared bottom electrode. Figure 4b plots the total current measured with a read voltage of 0.1 V ($v_1 = v_2 = 0.1\ \text{V}$) following the application of consecutive programming pulses (positive then negative). We show the case with both memristors pulsed (i.e., both are programmed with voltage pulses), the case with only one of the memristors pulsed, and with none pulsed (20 cycles shown for each case). For each cycle we also sweep the read voltage ($v_1 = v_2 = V_{\text{read}}$) between -0.15 and $+0.15\ \text{V}$ and measure the total current after all 30 positive programming pulses. The results from these voltage sweeps are shown in Fig. 4c. For the case where both memristor were pulsed (blue lines), the conductances G_1 and G_2 are both high (LRS) and

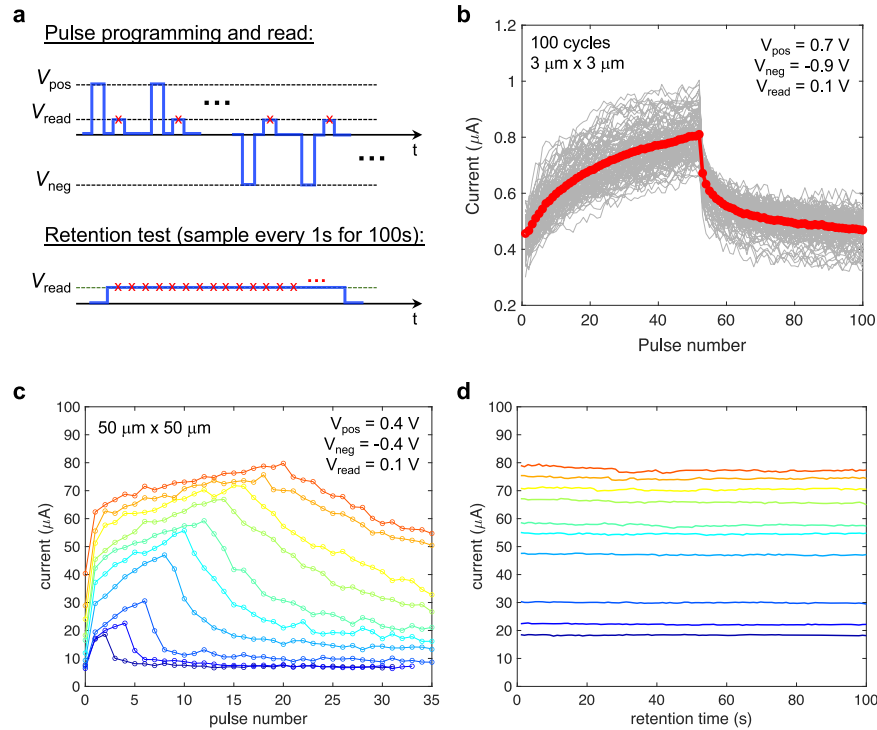


Fig. 3 Multi-state non-volatile pulse programming of h-BN memristors. **a** Diagram of the pulsed measurements and retention test. **b** 100 cycles of pulse programming for Au/h-BN/Ti memristor with $3 \mu\text{m} \times 3 \mu\text{m}$ active area (50 positive pulses, followed by 50 negative pulses for each cycle). Gray lines show 100 individual cycles, and the red line shows the average. **c** Pulse measurement cycles with increasing number of positive pulses. Deep blue to red colored curves corresponds to increasing the number of positive pulses from 2 up to 20. **d** Retention tests measured immediately after the last positive pulse for each cycle using a read voltage of $V_{read} = 0.1 \text{ V}$. The color of the curves in **d** match the color of the corresponding cycle in **c**.

therefore the current is the largest. When none of the memristors are pulsed (black lines), both G_1 and G_2 are low (HRS), and the current is the lowest. When only one memristor is pulsed, its conductance is high (LRS) while the other memristor's conductance is low (HRS), and the magnitude of the current is between the first two cases. The results in Fig. 4c indicate good linear behavior of the memristor I - V characteristics (needed for reliable dot-product operation)⁴⁰ and show good repeatability (small cycle-to-cycle variation).

DISCUSSION

We now demonstrate the implementation of stochastic multi-variable linear regression on an h-BN memristor array. In this implementation we use an h-BN memristor array to predict the profit of startup companies given their investment in marketing and in research and development (R&D). Our model is trained using a dataset from 50 startup companies available online⁴¹. In this implementation, the memristor conductances (G_1 and G_2) are the model parameters. The training process is illustrated in Fig. 5a. For each training step a single sample from the dataset is randomly selected (the sample includes profit, marketing, and R&D in \$K). The input variables (marketing and R&D) are translated (normalized) to voltages between 0 and 0.15 V. These voltages are applied to the h-BN memristors (v_1 and v_2). We have previously confirmed that for this range of read voltages the I - V response is linear, and the dot-product operation is reliable (see Fig. 4c). This is important for the implementation of linear regression as the prediction (h) is determined from the output current of the h-BN memristor array given by the dot product as

$$I = v^T G, v = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, G = \begin{bmatrix} G_1 \\ G_2 \end{bmatrix}. \quad (1)$$

The prediction is then compared against the training sample ($y = \text{profit}$) from which we determine the error and the required update for each of the model parameters (ΔG_1 and ΔG_2) (see "Methods" for details of the implementation). Here we use a hardware-compatible approach to update the model parameters whereby a single programming pulse is applied to each memristor^{42–44}, and the polarity of the pulse is determined by the sign of ΔG_1 and ΔG_2 . This programming pulse will slightly adjust the conductances to ultimately minimize the error in the prediction. To achieve good convergence, stochastic regression algorithms typically limit the parameter updates with a learning rate that is gradually reduced with training number^{42,43,45}. In our experiments the learning rate is implemented by gradually reducing the amplitude of the programming pulses. We reduce the amplitude of the programming pulses by 0.1% after each iteration (starting with $\pm 1 \text{ V}$, the pulse amplitude will be reduced to $\pm 0.67 \text{ V}$ after 400 training steps). The width of positive and negative programming pulses is kept fixed at 500 ns throughout the training process.

Figure 5b–d shows the results of the stochastic linear regression implementation. In Fig. 5b we plot the training data (black dots) as well as the model prediction before (magenta plane) and after 400 training steps (green plane). As shown, the trained model clearly predicts the profit of startup companies based on their investments in marketing and R&D much better than the before training. A more quantitative result is shown in Fig. 5c where we plot the mean squared error (MSE) as a function of the training step (i.e., iteration) as given by $\text{MSE} = (1/N) \sum_i \delta_i^2$ where N is the sample size (50 in this case) and $\delta_i = h_i - y_i$ is the error in the prediction. As shown, the MSE reduces with training indicating good convergence of the algorithm. Figure 5d shows the change in conductances G_1 and G_2 (the model parameters) during the

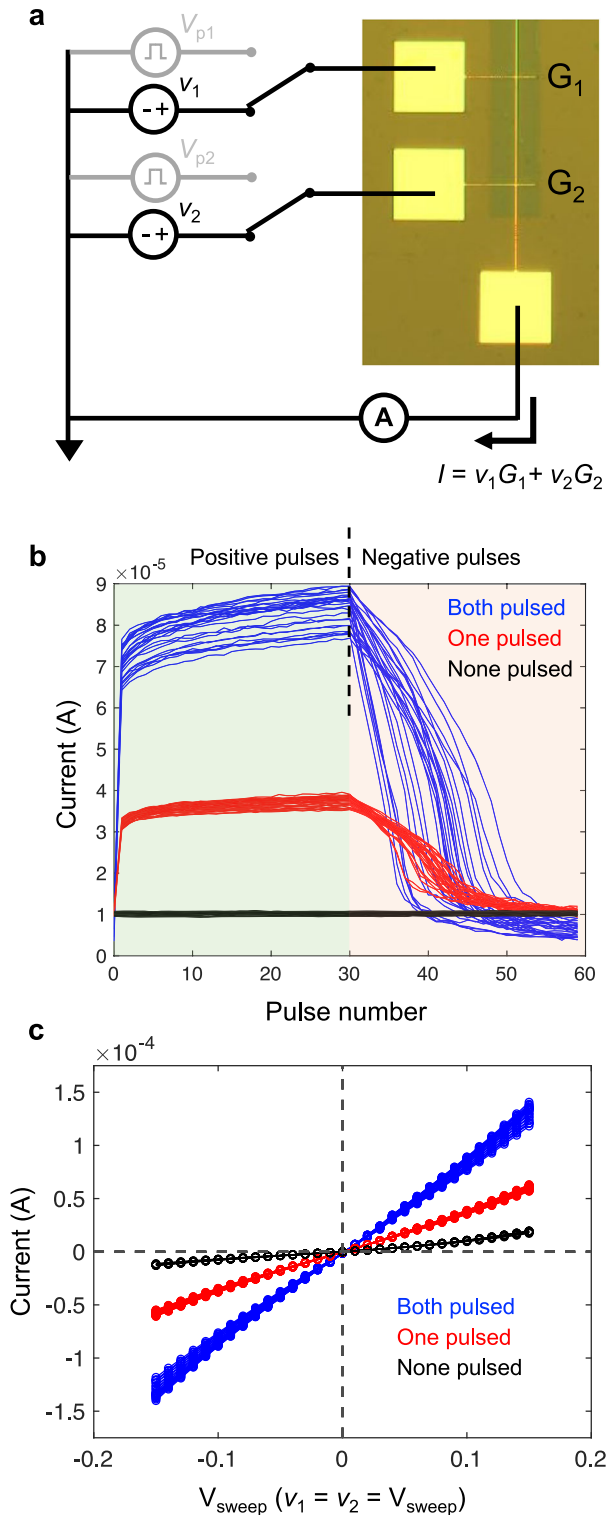


Fig. 4 Dot-product operation with h-BN memristor arrays. **a** Schematic of the experimental setup for demonstration of basic dot-product operation in h-BN memristor arrays. **b** Three different cases of pulse programming the memristor arrays: pulsing both memristors, pulsing just one, pulsing none (20 cycles for each case), a read voltage of $V_{\text{read}} = 0.1$ V used to measure current after each pulse. **c** For each cycle in part (b) we also sweep the read voltage V_{sweep} between -0.15 and $+0.15$ and measure total current to show the linearity and repeatability of the dot-product operation. The sweeps are done after the 30 positive pulses for each cycle.

training process. The mean absolute error (MAE) was also calculated and is shown in Supplementary Fig. 4. We see larger updates and fluctuations in the conductances during the initial training steps, and eventually convergence to the optimal values for the model parameters.

In this article, we have reported the fabrication and characterization of Au/h-BN/Ti memristor arrays. We have presented statistics for the nonvolatile resistive switching behavior of h-BN memristors, including the effects of cell active area. We have then focused on establishing the non-volatile multistate pulse programmability of the h-BN memristors based on multiple cycles of consecutive programming pulses, and retention tests. Our results show successful multistate programming of conductive states with good stability. Moreover, we have presented the implementation of the dot-product operations on h-BN memristor arrays, and show good linearity and repeatability, which is crucial for machine learning hardware. Finally, we have demonstrated the hardware implementation of stochastic multivariable linear regression on an h-BN memristor array. Our hardware-compatible implementation shows good convergence and represents an important milestone in advancing the research and implementation of 2D materials for machine learning hardware. It also paves the way for more sophisticated demonstrations of machine learning algorithms using 2D materials, devices, and circuits.

METHODS

h-BN memristor and memristor arrays fabrication

The Au/h-BN/Ti memristor arrays were fabricated on a 90 nm SiO_2/Si wafer. First, the bottom electrodes (5 nm Cr/35 nm Au) with 3, 20, and 50 μm width were patterned on the substrate via photolithography and e-beam evaporation methods. Second, CVD-grown multilayer h-BN on copper from Graphene Supermarket was transferred onto the prepared SiO_2/Si substrate by wet transfer method. Third, h-BN film was patterned to expose the 100 μm by 100 μm bottom electrodes pads using oxygen plasma. Finally, the top electrodes (70 nm Ti) were patterned with the same electrode width and the same methods as that of the bottom electrodes. The top electrodes are exposed to air and a thin surface layer may be oxidized over time. This oxidized layer can be easily penetrated with probe needles during measurements, and its impact on the resistive switching behavior has been ruled out by comparing against devices with Au-capped top electrodes that show very similar characteristics (see Supplementary Fig. 5). More details about fabrication process and a diagram of the fabrication flow are provided in Supplementary Fig. 2.

Electrical characterization

The electrical characterization was conducted on a Cascade semi-automatic probe station using a Keithley 4200 semiconductor characterization system. The DC I - V measurements were performed using source measure units (SMUs), while the pulse programming experiments used a combination of pulse measure units (PMU, model 4225) for programming pulses and SMUs for reading currents. In the pulse programming experiments we switched between PMU and SMU automatically using a Keithley remote amplifier/switch (4225-RPM). Supplementary Fig. 3 shows the experimental setup.

Linear regression test

Our implementation of multivariable stochastic linear regression on the Au/h-BN/Ti memristor arrays was trained using a dataset available online⁴¹. The experimental demonstration was done with a Keithley 4200 SCS using a custom test script developed in the Keithley user library tool (KULT) and executed in the Keithley interactive testing environment (KITE). The input parameters to the test script are the minimum and maximum conductance values for each memristor (predetermined based on pulse measurements, used to normalize output currents from the array), the initial values for the programming pulse amplitudes, the constant value for the width of the programming pulses, and the number of iterations. The test script loads the training data and normalizes the independent variables (in this case marketing and R&D investments in thousands of dollars) to voltages

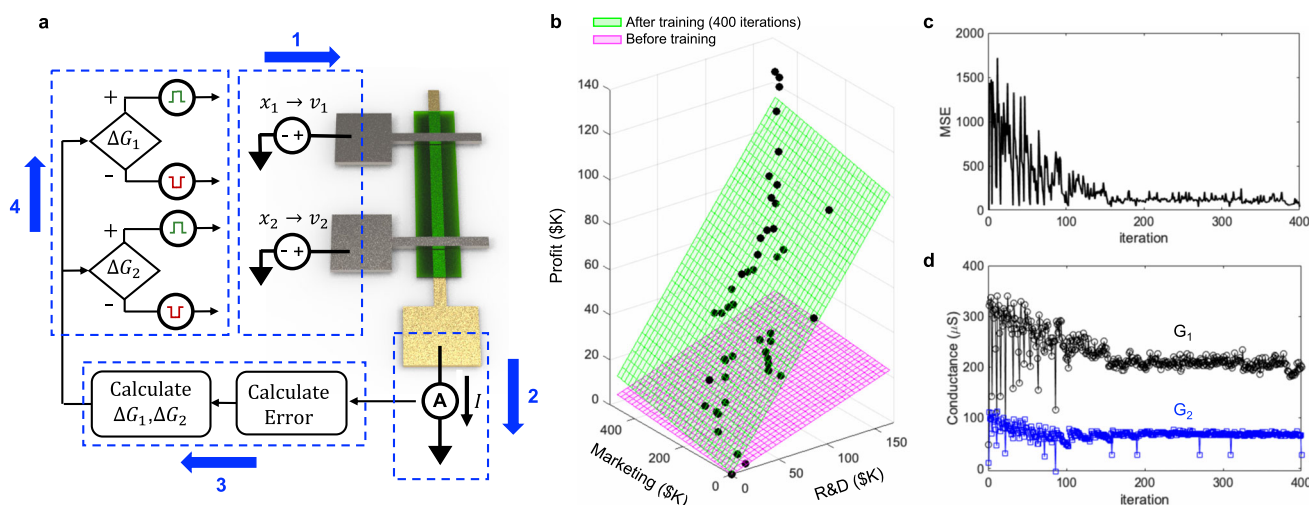


Fig. 5 Implementation of stochastic multivariable linear regression on h-BN memristor arrays. **a** Flow diagram for stochastic multivariable linear regression on h-BN memristor arrays (graphical description of one step in the training process): In step 1, the inputs (independent variables) are translated to DC voltages and applied to the array (top electrodes). In step 2, the total output current (the model prediction) is measured at the shared bottom electrode. In step 3, the prediction error is calculated by comparing against the training sample, and model parameter updates are obtained (ΔG_1 and ΔG_2). In step 4, a single programming pulse is applied to each memristor (polarity of the pulse determined by the sign of ΔG). Good convergence of the implementation is verified by **b** model prediction fit to training data before (magenta plane) and after (green plane) training. **c** Evolution of mean squared error (MSE) with training, and **d** evolution of h-BN memristor conductances (model parameters) with training step (iterations) reaching stable values that minimize prediction error.

between 0 and 0.15 V. We also subtract a constant offset (y-intercept) from the dependent variable (profit) so that the model is based only on two regression coefficients (model parameters represented by the memristor conductances). The script then goes into a loop where it randomly selects a sample for the data set and apply the read voltages (v_1 and v_2) that correspond to the independent variables of that sample. The current $I = v_1 G_1 + v_2 G_2$ is read at the output of the h-BN memristor array (shared bottom electrode) and is translated from Amps to dollars to be compared against the training sample. This read operation is conducted with the Keithley SMUs. We then calculate the error (δ) in the prediction as well as the required update for each model parameter (i.e., ΔG_1 and ΔG_2). From the minimization of the cost function (i.e., $\delta^2/2$) the updates are calculated as $\Delta G = -\delta v$. Here we propose a simplified hardware-compatible regression approach where the memristor conductances (i.e., the model parameters) are updated through the application of a single programming pulse, and the polarity of the pulse is determined by the sign of the corresponding ΔG . The programming pulses are applied using the Keithley's 4225 PMU (pulse width is fixed to 500 ns). Gradient descent algorithms typically use learning rate decay to improve convergence, where model parameter updates are weighted by a learning rate (α) that is reduced gradually as training advances. In our hardware demonstration we introduce learning rate decay by gradually reducing the amplitude of the programming pulses (we have reduced the amplitude of the programming pulses by 0.1% after each iteration).

DATA AVAILABILITY

Data that supports the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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REFERENCES

- Huyghebaert, C. et al. 2D materials: Roadmap to CMOS integration. In *2018 Intentional Electron Devices Meeting (IEDM)*, 512–515 (IEEE, 2018).
- Li, M.-Y., Su, S.-K., Wong, H.-S. P. & Li, L.-J. How 2D semiconductors could extend Moore's law. *Nature* **567**, 169–170 (2019).
- Su, S.-K. et al. Layered semiconducting 2D materials for future transistor applications. *Small Struct.* **2**, 2000103 (2021).
- Robinson, J. A. Perspective: 2D for beyond CMOS. *APL Mater.* **6**, 058202 (2018).
- Lemme, M. C., Akinwande, D., Huyghebaert, C. & Stampfer, C. 2D Materials for future heterogeneous electronics. *Nat. Commun.* **13**, 1392 (2021).
- Quellmalz, A. et al. Large-area integration of two-dimensional materials and their heterostructures by wafer bonding. *Nat. Commun.* **12**, 1–11 (2021).
- Yu, L. et al. High-performance WSe₂ complementary metal oxide semiconductor technology and integrated circuits. *Nano Lett.* **15**, 4928–4934 (2015).
- Lin, Z. et al. Solution-processable 2D semiconductors for high-performance large-area electronics. *Nature* **562**, 254–258 (2018).
- Amani, M., Burke, R. A., Proie, R. M. & Dubey, M. Flexible integrated circuits and multifunctional electronics based on single atomic layers of MoS₂ and graphene. *Nanotechnology* **26**, 115202 (2015).
- Xie, J. et al. Analysis of Schottky barrier heights and reduced Fermi-level pinning in monolayer CVD-grown MoS₂ field-effect-transistors. *Nanotechnology* **33**, 225702 (2022).
- Chen, S. et al. Wafer-scale integration of two-dimensional materials in high-density memristive crossbar arrays for artificial neural networks. *Nat. Electron.* **3**, 638–645 (2020).
- Wang, L. et al. Electronic devices and circuits based on wafer-scale polycrystalline monolayer MoS₂ by chemical vapor deposition. *Adv. Electron. Mater.* **5**, 1–10 (2019).
- Das, S., Chen, H. Y., Penumatcha, A. V. & Appenzeller, J. High performance multilayer MoS₂ transistors with scandium contacts. *Nano Lett.* **13**, 100–105 (2013).
- Lembke, D., Bertolazzi, S. & Kis, A. Single-layer MoS₂ electronics. *Acc. Chem. Res.* **48**, 100–110 (2015).
- Schwierz, F. Graphene transistors. *Nat. Nanotechnol.* **5**, 487–496 (2010).
- Reddy, D., Register, L. F., Carpenter, G. D. & Banerjee, S. K. Graphene field-effect transistors. *J. Phys. D: Appl. Phys.* **44**, 313001 (2011).
- Ge, R. et al. Atomistic: Nonvolatile resistance switching in atomic sheets of transition metal dichalcogenides. *Nano Lett.* **18**, 434–441 (2018).
- Rehman, S. et al. Thickness-dependent resistive switching in black phosphorus CBRAM. *J. Mater. Chem. C* **7**, 725–732 (2019).
- Ahmed, T. et al. Mixed ionic-electronic charge transport in layered black-phosphorus for low-power memory. *Adv. Funct. Mater.* **32**, 1–11 (2022).
- Pradhan, S. K., Xiao, B., Mishra, S., Killam, A. & Pradhan, A. K. Resistive switching behavior of reduced graphene oxide memory cells for low power nonvolatile device application. *Sci. Rep.* **6**, 1–9 (2016).
- Romero, F. J. et al. Resistive switching in graphene oxide. *Front. Mater.* **7**, 1–5 (2020).
- Shi, Y. et al. Electronic synapses made of layered two-dimensional materials. *Nat. Electron.* **1**, 458–465 (2018).
- Zhu, K. et al. Graphene-boron nitride-graphene cross-point memristors with three stable resistive states. *ACS Appl. Mater. Interfaces* **11**, 37999–38005 (2019).

24. Wu, X. et al. Thinnest nonvolatile memory based on monolayer h-BN. *Adv. Mater.* **31**, 1–7 (2019).
25. Nikam, R. D., Rajput, K. G. & Hwang, H. Single-atom quantum-point contact switch using atomically thin hexagonal boron nitride. *Small* **17**, 1–8 (2021).
26. Derhacopian, N., Hollmer, S. C., Gilbert, N. & Kozicki, M. N. Power and energy perspectives of nonvolatile memory technologies. *Proc. IEEE* **98**, 283–298 (2010).
27. Ge, J. et al. A sub-500 mV monolayer hexagonal boron nitride based memory device. *Mater. Des.* **198**, 109366 (2021).
28. Lee, J. et al. Synaptic characteristics of amorphous boron nitride-based memristors on a highly doped silicon substrate for neuromorphic engineering. *ACS Appl. Mater. Interfaces* **12**, 33908–33916 (2020).
29. Liang, X. et al. 150 nm × 200 nm cross point hexagonal boron nitride based memristors with ultra-low currents in high resistive state. In *2019 Electron Devices Technol. Manuf. Conf. EDTM 2019* 258–260 (IEEE, 2019).
30. Sanchez Esqueda, I., Zhao, H. & Wang, H. Efficient learning and crossbar operations with atomically-thin 2D material compound synapses. *J. Appl. Phys.* **124**, 152133 (2018).
31. Musisi-Nkambwe, M., Afshari, S., Barnaby, H., Kozicki, M., & Sanchez Esqueda, I. The viability of analog-based accelerators for neuromorphic computing: A survey. *Neuromorphic Comput. Eng.* **1**, 012001 (2021).
32. Huh, W., Lee, D. & Lee, C. H. Memristors based on 2D materials as an artificial synapse for neuromorphic electronics. *Adv. Mater.* **32**, 2002092 (2020).
33. Mahmoodi, M. R., Prezioso, M. & Strukov, D. B. Versatile stochastic dot product circuits based on nonvolatile memories for high performance neurocomputing and neurooptimization. *Nat. Commun.* **10**, 1–10 (2019).
34. Hu, M. et al. Dot-product engine for neuromorphic computing: Programming 1T1M crossbar to accelerate matrix-vector multiplication. In *2016 53rd ACM/EDAC/IEEE Design Automation Conference (DAC)* 1–6 (IEEE, 2016).
35. Berggren, K. et al. Roadmap on emerging hardware and technology for machine learning. *Nanotechnology* **32**, 012002 (2021).
36. Ma, G. et al. Ultra-high ON/OFF ratio and multi-storage on NiO resistive switching device. *J. Mater. Sci.* **52**, 238–246 (2017).
37. Wong, H. S. P. et al. Metal-oxide RRAM. *Proc. IEEE* **100**, 1951–1970 (2012).
38. Fantini, A. et al. Intrinsic switching variability in HfO₂ RRAM. In *2013 5th IEEE Int. Mem. Work. IMW 2013* 30–33 (IEEE, 2013).
39. Merced-Grafals, E. J., Dávila, N., Ge, N., Williams, R. S. & Strachan, J. P. Repeatable, accurate, and high speed multi-level programming of memristor 1T1R arrays for power efficient analog computing applications. *Nanotechnology* **27**, 365202 (2016).
40. Li, C. et al. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* **1**, 52–59 (2018).
41. Farhan. 50 Startups. <https://www.kaggle.com/datasets/farhanmd29/50-startups> (2022).
42. Afshari, S., Musisi-Nkambwe, M. & Sanchez Esqueda, I. Analyzing the impact of memristor variability on crossbar implementation of regression algorithms with smart weight update pulsing techniques. *IEEE Trans. Circuits Syst. I Regul. Pap.* **69**, 2025–2034 (2022).
43. Nair, M. V. & Dudek, P. Gradient-descent-based learning in memristive crossbar arrays. In *Proc. Int. Jt. Conf. Neural Networks* 1–7 (IEEE, 2015).
44. Prezioso, M. et al. Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* **521**, 61–64 (2015).
45. Wen, S. et al. Adjusting learning rate of memristor-based multilayer neural networks via fuzzy method. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **38**, 1084–1094 (2019).

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AUTHOR CONTRIBUTIONS

J.X. fabricated the h-BN memristor arrays and tested individual memristors. J.X. and S.A. performed experiments h-BN memristor arrays. J.X., S.A., and I.S.E. analyzed the experimental results and wrote the manuscript. I.S.E. conceived and designed the experiments.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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