Design Automation of CMOS Op-Amps Using Statistical Geometric Programming

Sangjukta R. Chowdhury, Sumit Bhardwaj, and Jennifer Kitchen
Department of Electrical, Computer, and Energy Engineering, Arizona State University
Tempe, Arizona, USA
srchowd1@asu.edu

***Abstract*—This work proposes a novel design automation (DA) technique that uses a multifaceted approach combining Multivariate Regression with Geometric Programming (GP) to design analog circuits. Previous DA methods employing GP have typically used analytical derivations of the various design equations representing an analog circuit. The proposed DA method eliminates the need for analytical derivations by using simulation data and multivariate regression to generate statistical models combined with GP to solve these statistical expressions with respect to optimum circuit design parameters. This presented statistical GP method has been applied to successfully design a five-transistor two-stage operational amplifier and a folded cascode amplifier in a TSMC 65nm CMOS technology. The presented statistical GP DA results are comparable to the design results obtained from both analytical GP and manual design by an experienced analog design engineer.**

***Index Terms*—CMOS Op-Amps, Design Automation, Geometric Programming, Linear Regression, Statistical GP**

I. Introduction

Complex analog circuits remain a design automation challenge that have most commonly been synthesized with either simulation or model-based methods [1]. Within model-based approaches, Geometric Programming (GP) has a variety of advantages, as large-scale GP's can be efficiently solved using simple mathematical toolboxes within a few seconds to come to an optimum solution after only a few iterations. Analytical GP methods can therefore be executed with little computational power and time [2]. Circuit design problems have historically been well formulated using GP [3], and various low transistor count analog circuits have been successfully designed using analytical-based GP [4]. Unfortunately, it's more difficult to derive equations for complex analog circuits, and performing such a systematic process would render costly and require high designer effort to derive the analytical expressions, thus defeating the intent of automation.

On the other hand, simulation-based DA methods are currently most popular with access to large computational power and machine learning (ML) algorithms as optimization tools. Some notable simulation methodologies include DELIGHT.SPICE, FRIDGE, FASY, ANACONDA, MAELSTROM and DARWIN [5], [6]. Additionally, recent works employ simulation based methodologies along with machine learning algorithms for analog synthesis [1], [7]–[9]. Batch Bayesian Optimization is used in [1], [7] with small number of data samples, but requires multiple iterations/runs to reduce random fluctuations in output results. Reinforcement learning has been used to size circuits and meet target specifications on 96.3% of the design goals tested, however, this method requires large number of data samples [8]. Problems with prediction error and machine learning costs are addressed in [9] using an artificial neural network with a small dataset, but this approach requires large computational time. The Prism tool uses automatic generation of posynomial response models to describe performance characteristics of ASICs [10]. While this method also eliminates the need for analytical derivations, it does so using various mathematical techniques rather than ML algorithms.

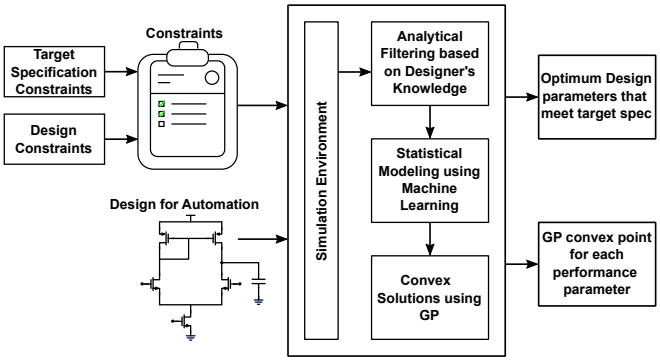

Fig. 1. Overview of Proposed Design Automation

This work presents a simulation-based method using multivariate regression to form design expressions that statistical GP uses to optimize an analog circuit's performance. The overall algorithm is described in Fig. 1, where design constraints, target performance, and circuit topologies are fed into the algorithm that outputs optimum design variables and corresponding performance parameters. The setup time when compared with analytical GP is significantly reduced by using simulation data. Additionally, the proposed statistical GP method presents with low computational power comparable to other state-of-the-art simulation-based methods.

The presented statistical GP collects data through simulation only one time and doesn't require multiple iterations. The work presented here can later be expanded to include other ML algorithms that decrease computational power by collecting smaller number of data samples more iteratively to create the statistical models. Section II presents the design automation methodology, detailing the combination of regression and statistical GP for DA. Section III uses the presented algorithm

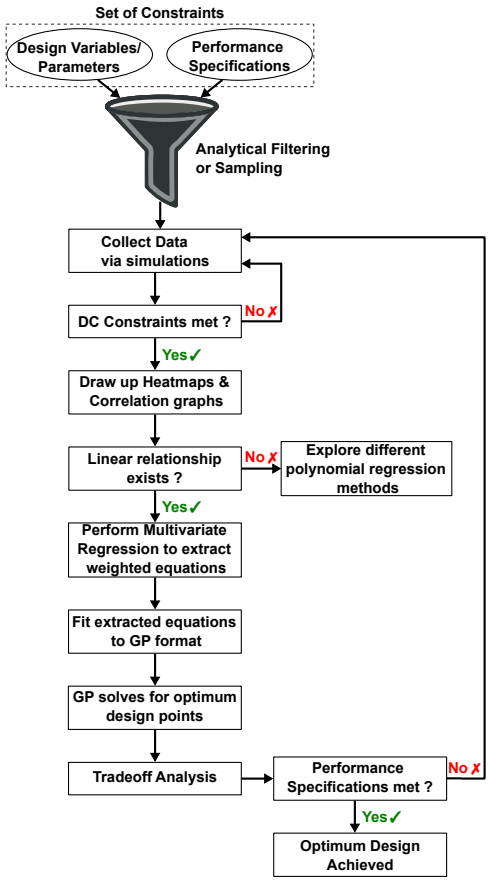

Fig. 2. Proposed Design Automation Procedure

to automate a 2-stage CMOS operational amplifier (op-amp) in a 65nm TSMC process and compares the presented statistical GP with analytical GP results. Finally, Section IV presents the experimental results on a folded cascode amplifier to validate the presented DA method and compare to other simulation-based approaches. Section V concludes this work.

II. Proposed Design Automation Flow

Fig. 2 details the proposed design automation flow, where design and performance parameter constraints are inputs that are filtered through specific knowledge based models built from basic analog circuit knowledge. This allows for smart sampled data collection. The important data is then checked against the circuit's DC constraints, for instance, checking that all devices are operating in saturation. If DC constraints are met, heatmaps are then drawn to check for correlation strengths between design variables and performance parameters. If linear relationships are found, then a multi-variate regression (MVR) model is created. The extracted MVR model is then formatted to fit a GP optimization problem. The GP solves for an optimum solution and a tradeoff analysis is performed between the various performance parameters. If the input performance specifications are achieved, then an optimum circuit design has been reached. Otherwise, the automation loops back to collect more data that will expand the design space to a potential region where the performance specifications can be met.

Creating analytical, equation based models for larger circuits when using analytical GP can be time consuming and complicated. In this work, analytical derivations are bypassed by drawing relations between circuit design variables and circuit performance parameters using simulation data. These relationships are determined by feeding the collected simulation data to ML algorithms, namely regression for this work, and fitting the data using trend lines predicted by the regression algorithm.

A. Linear and Multi-Variate Regression

Linear Regression assumes a linear relationship between the input variable X and output variable Y, and it has the lowest mean-squared error compared with other ML methodologies and allows for interpolation of the relationship, which means that design predictions can be made in regions where simulation data has not been collected.

While a linear relationship draws a line to compare a single independent variable with a single dependent, MVR describes the relationship between multiple independent variables to a single dependent variable [X,Y]. Once linear relationships between certain design variables and performance parameters in the circuit are confirmed, MVR is performed on those design variables to link them to each single performance parameter. Heatmaps are first created in MVR to determine the correlation coefficients between each of these design variables and the performance parameters. The strongest correlations become the features, or design variables, used in the MVR model. The collected data is divided into test samples and training samples for the regression model. A cost function is selected and a minimization algorithm, such as a Gradient Descent algorithm in this work, is used to find the most accurate expressions describing the relationships between the performance parameters and the design variables. A Regression Score parameter (R^2) is also output to judge the correlation strength between design parameters and performance parameters.

B. Geometric Programming

GP is an optimization problem that is able to output the optimal circuit solution given a set of design parameter constraints [3]. The presented statistical GP uses the weighted equations derived from the MVR algorithm that links the design parameters/variables with the performance parameters. The objective function needs to be in the form of posynomials (positive polynomials) for GP; and therefore, the weighted functions extracted from MVR are an excellent fit for the optimization problem. The few MVR curve fit equations that are not suitable for GP are fitted mathematically to suit the GP format. This formatting includes transformations such as drawing inverse relationships between a design variable and a performance parameter. Using statistical GP, the circuit's performance parameters are optimized within its design constraints. In this work, the GP algorithm was also performed using analytical derivations (equations) that describe the circuit to compare the results and prove the validity of statistical GP with MVR.

III. Basic Op-Amp Design Using Proposed Method

A. Design Automation Procedure

The presented algorithm was used to design a basic 2-stage CMOS op-amp driving a load capacitor (C_L) of 100 fF, as shown in Fig. 3. The op-amp was designed in the TSMC 65nm process technology, where the number of fingers for each of the transistors (M_1-M_7) is varied with fixed width (W) per finger of 1.2 μm and fixed Length (L) of 100 nm. A fixed width per finger and length were chosen for this test case, but the designer may also include varying width per finger and length in this automation algorithm. The input transistors (M_1-M_2) were varied together to maintain differential op-amp behavior. The op-amp's bias current I_{bias} was also varied. Simulation data was collected for 7 performance parameters using Cadence Spectre: DC Gain (dB), Unity-Gain Bandwidth (UGB), Phase Margin (PM), Power Consumption (Power), Common Mode Rejection Ratio (CMRR), Positive Power Supply Rejection Ratio (PSRR+), and Negative Power Supply Rejection Ratio (PSRR-). A Heatmap was then created to understand the correlation factors between design variables and these performance parameters, as given in Fig. 4. This information was used to reduce the number of variables in the MVR models. The Heatmap suggested that correlation of the performance parameters with transistor fingers $f_{M3,4}$ and f_{M6} was weak, and hence while creating the MVR models, these were removed. The R^2 results of each relationship are presented in Table I, and show strong correlation between design variables and performance parameters, with R^2 scores above 40% in many cases. The optimum point for each performance parameter was then solved using GP on the seven extracted weighted equations from MVR that describe the seven performance parameters. The final design results results from the proposed statistical GP algorithm are compared with design results obtained from an analytical GP [4] in Table II. The final results are very similar, but statistical GP requires minimal designer effort.

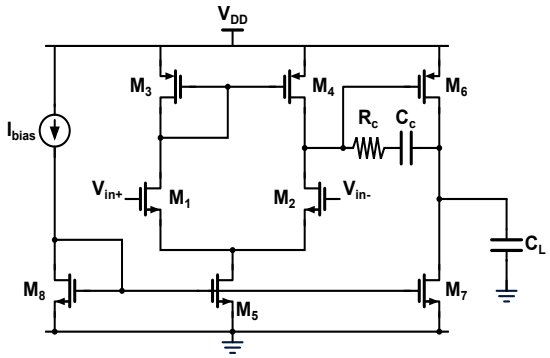

Fig. 3. Schematic diagram of the 2-stage CMOS Op-Amp

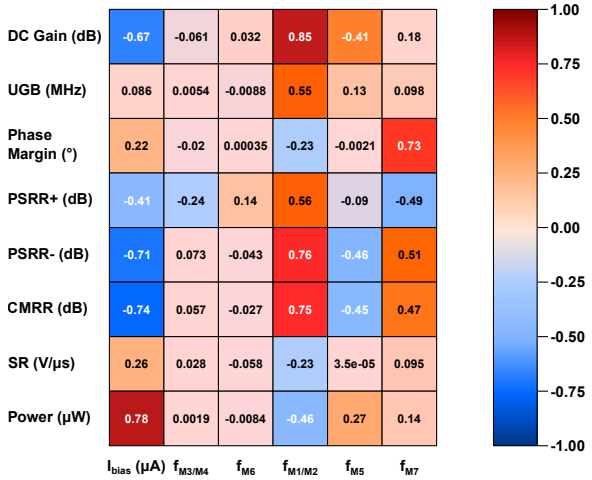

Fig. 4. Correlation Heatmap for the CMOS Op-Amp

TABLE I
Regression Score (R^2) for Various Performance Parameters versus Design Variables

	I_{bias}	$f_{M1,M2}$	f_{M5}	f_{M7}	MVR
DC Gain (dB)	0.44	0.79	0.70	0.02	0.95
UGB (MHz)	0.22	0.48	0.72	0.05	0.67
Power (μW)	0.63	0.21	0.49	0.80	0.93
Phase Margin (°)	0.01	0.18	0.14	0.92	0.51
Pos. PSRR (dB)	0.05	0.49	0.11	0.77	0.60
Neg. PSRR (dB)	0.53	0.58	0.50	0.65	0.82
CMRR (dB)	0.55	0.60	0.60	0.58	0.95

TABLE II
Comparison of Design Specifications, Analytical GP and Statistical GP Results

Constraint	Specification	Analytical GP	Statistical GP
ICMR	[0,1]V_{DD}	[0,1]V_{DD}	[0,1]V_{DD}
OCMR	[0.1,0.9]V_{DD}	[0.1,0.9]V_{DD}	[0.08,0.875]V_{DD}
Power	$\leq$ 500 μW	$\leq$ 168 μW	$\leq$ 132.6 μW
DC Gain	$\geq$ 35 dB	39.79 dB	40.26 dB
UGB	$\geq$ 500 MHz	655.32 MHz	647.37 MHz
PM	$\geq$ 45°	60°	54.27°
CMRR	$\geq$ 30 dB	45.08 dB	45.02 dB
PSRR-	$\geq$ 40 dB	58.44 dB	55.94 dB
PSRR+	$\geq$ 40 dB	46.89 dB	46.75 dB

B. Tradeoff Analysis

Once each performance parameter is individually optimized against the design variables, a tradeoff analysis is performed such that designers may decide upon the optimum overall circuit performance. A sample set of plots are shown in Fig. 5 and 6 for the 2-stage op-amp, where the performance data is

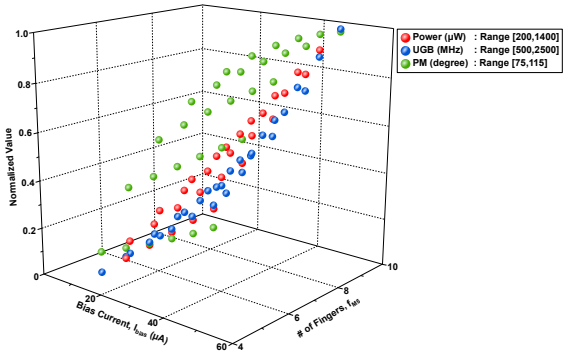

Fig. 5. Tradeoff Analysis for Power, UGB and PM against Bias Current (I_{bias}), and Number of tail transistor Fingers (f_{M5})

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART SIMULATION-BASED DA

Parameters	[1] (DAC 2020)	[7] (TCAD 2021)	[8] (DATE 2020)	[9] (TCAD 2021)	**This Work**
Methodology	Easy-BO	MACE	AutoCkt: Deep Reinforcement Learning	ESSAB using ANN	Statistical GP using MVR
Op-Amp Design	2-Stage	2-Stage	2-Stage	Folded Cascode	Folded Cascode
No. of Performance Parameters Optimized	3	3	4	9	7
Training Samples	150 (20 times)	270 (20 times)	17 x 10^4	500	2700
CPU Specification	2 Intel Xeon X5650 CPUs and 128 GB memory	2 Intel Xeon CPUs and 128 GB memory	8 Core CPU machine	Intel Xeon CPU and 128 GB memory	Intel Xeon(R) E5-2650 and 256 GB memory
Process	180 nm	SMIC 180 nm	45 nm BSIM	180 nm	TSMC 65 nm
Computation Time	1 Hr 36 mins	–	1 Hr 18 mins	2 Hrs 30 mins	40 mins
Simulation Platform	HSPICE	HSPICE	AutoCkt interfaced with Cadence Spectre & BAG	Cadence Spectre	Cadence Spectre

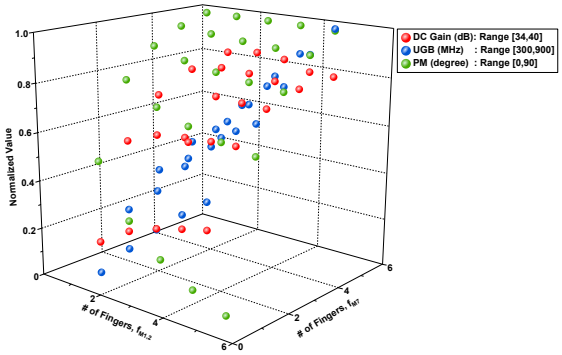

Fig. 6. Tradeoff Analysis for DC Gain, UGB and PM against Number of Fingers of transistors, $f_{M1,2}$ & f_{M7}

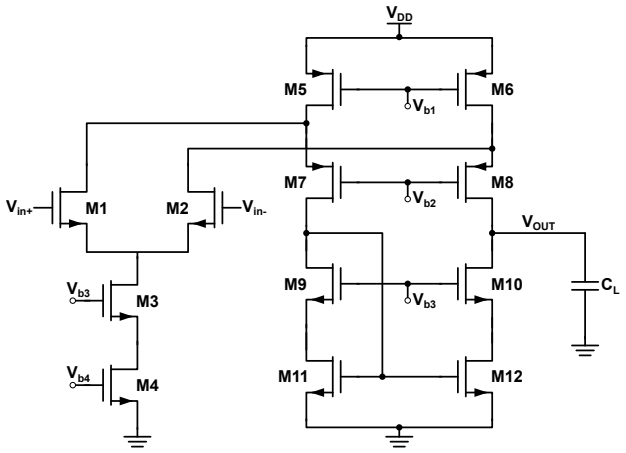

Fig. 7. Schematic diagram of the Folded Cascode CMOS Op-Amp

normalized in the plot to fit to a single scale. For instance, in Fig. 5, if the designer wants to save static power by dissipating less bias current, then the UGB of the op-amp needs to be sacrificed in order to achieve a particular PM. Furthermore, optimum sizing of input and tail transistors can be chosen based on tradeoffs amongst DC Gain, UGB and PM, as depicted in Fig. 6.

IV. EXPERIMENTAL RESULTS WITH TEST CIRCUIT

The presented DA algorithm was validated through design of a folded cascode CMOS op-amp with a C_L of 1 pF, as shown in Fig. 7. The automated design results were comparable to results obtained from manual design by an experienced analog circuit designer, as summarized in Table IV. Instead of varying the widths of all transistors, the simulation data was collected using analytical techniques such as those in [11] to reduce simulation time. Cadence Spectre was used to collect the simulation data. The regression models were created using Scikit Learn libraries in Python, which produced models within seconds. Finally, the GP took approximately 2-3 seconds to output the optimized results for all performance parameters. An overall comparison of the presented DA methodology with other simulation-based methods that use machine learning algorithms is given in Table III. Although the presented method collects higher number of initial samples, it does not require iterations and therefore has comparable simulation times and performance to other state-of-the-art simulation-based techniques.

TABLE IV
COMPARISON OF SPECIFICATIONS, DESIGNER RESULTS, AND STATISTICAL GP RESULTS

Constraint	**Specification**	**Designer's Result**	**Statistical GP**
ICMR	[0,1.0]V_{DD}	[0,1.0]V_{DD}	[0,1.0]V_{DD}
OCMR	[0.2,0.8]V_{DD}	[0.2,0.8]V_{DD}	[0.15,0.85]V_{DD}
Power	$\leq$ 1000 μW	$\leq$ 609.6 μW	$\leq$ 598.73 μW
DC Gain	$\geq$ 40 dB	43.56 dB	44.16 dB
UGB	$\geq$ 100 MHz	109.8 MHz	119.01 MHz
PM	$\geq$ 60°	67.23 °	68.62°
CMRR	$\geq$ 60 dB	85.29 dB	87.76 dB
PSRR-	$\geq$ 40 dB	47.78 dB	48.02 dB
PSRR+	$\geq$ 40 dB	48.42 dB	49.76 dB

V. CONCLUSION

This work presents a statistical GP DA approach that uses a combination of simulation data, MVR, and GP to design analog op-amps. Statistical GP is a better alternative to analytical GP when designing more commonly used complex analog circuits. The presented approach was successfully verified through design of two test circuits in a 65nm TSMC process: a 2-stage basic op-amp and a more complex folded cascode op-amp. The proposed method may be applied to any arbitrary analog circuit using the presented looping design flow as a streamlined step-based automation approach.

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