Schottky diode characteristics on high-growth rate LPCVD β-Ga_2O_3 films on (010) and (001) Ga_2O_3 substrates

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High crystalline quality thick β-Ga_2O_3 drift layers are essential for multi-kV vertical power devices. Low-pressure chemical vapor deposition (LPCVD) is a suitable technique to achieve high growth rates. This paper presents a systematic study of the Schottky barrier diodes fabricated on four different Si-doped homoepitaxial β-Ga_2O_3 thin films grown on Sn-doped (010) and (001) β-Ga_2O_3 substrates by LPCVD with fast growth rate varying from 13 μm/h to 21 μm/h. A higher temperature growth results in the highest reported growth rates to date. Room temperature current density-voltage data for different Schottky diodes is presented and diode characteristics such as ideality factor, barrier height, specific on-resistance, and breakdown voltage are studied. Temperature dependence (25 ^{0}C-250 ^{0}C) of the ideality factor, barrier height, and specific on-resistance is also analyzed from the *J-V-T* characteristics of the fabricated Schottky diodes. The reported work shows the promise of the LPCVD growth technique with a high growth rate to grow β-Ga_2O_3 on native substrates for vertical power devices with thick active layers.

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Recently, there has been a growing interest in developing power electronics technology based on ultra-wide bandgap (UWBG) semiconductors because of the potential for significantly higher switching efficiency and higher power conversion densities [1–5]. These technologies could potentially surpass the performance of the current commercialized WBG technologies of Silicon Carbide (SiC) and Gallium Nitride (GaN). UWBGs with their high Baliga's figure of merit (BFOM= $\varepsilon.\mu.E_c^3$, where ε, μ, and E_c are the dielectric constant, carrier mobility, and critical breakdown field strength, respectively) can provide more efficient performance such as high breakdown voltage, small size, low on-state resistance, and low switching losses [6–11]. Monoclinic beta-phase gallium oxide (β-Ga_2O_3, referred to hereinafter as Ga_2O_3) has recently attracted tremendous interest as a high-performing and economically viable UWBG power device technology. It has an ultrawide-bandgap 4.8 eV, predicted breakdown field of ~ 8MV/cm, n-doping control over a larger range, and most importantly, a unique advantage of free-standing native substrates synthesis technology by low-cost methods [12–17]. The large experimentally measured field strengths also make it attractive for multi-kV (>10 kV) devices for medium voltage grid applications. High-quality epitaxy layers with low compensating defects and heterostructures have been demonstrated [18]. Taking advantage of these properties, several groups have demonstrated high voltage breakdown devices and high-frequency RF devices [6,19–24] further confirming its potential for power and RF technology.

Vertical devices are generally preferred over lateral geometries for power electronics applications due to the absence of surface effects. For beyond-10kV devices, this requires high quality low-doped thick (10 -100 μm) drift layers with low-compensation doping ruling out slow rate methods such as molecular beam epitaxy (MBE). While other techniques such as low-pressure chemical vapor deposition (LPCVD) [25,26], metal-organic chemical vapor deposition

(MOCVD) [27,28], pulsed laser deposition (PLD) [29], and halide vapor phase epitaxy (HVPE) [30–33] can provide higher growth rates. HVPE films with a growth rate of 5 μm/h on (001) [30] and LPCVD with a growth rate of ~2 μm/h on (010) substrates [25] have been reported. LPCVD in particular has demonstrated high-quality Ga_2O_3 homo-epitaxy with controllable doping [34], characterized by the high room-temperature and low-temperature mobility and commensurate low compensating acceptor impurity concentration. Additionally, the lower cost of LPCVD makes it a preferred growth technique for multi-kV vertical Ga_2O_3 power devices.

In this work, we investigated the LPCVD growth of Si-doped n-type Ga_2O_3 homoepitaxial drift layers on both (010) and (001) Sn-doped Ga_2O_3 substrates. The growth rates of ≥ 13 μm/h is achieved using LPCVD on both (010) and (001) substrates, highest reported homoepitaxial growth rate for Ga_2O_3. The surface morphology and crystal quality of the grown films were characterized by atomic force microscopy (AFM), and X-ray diffraction (XRD), revealing promising crystalline quality. We report a detailed study on the electrical behavior, both at room temperature and as a function of elevated temperature, of four LPCVD grown Ga_2O_3 Schottky diode samples of different surface smoothness and substrate crystal orientations. The films on (001) grown with a growth rate of 13 μm/h show the best device performance in terms of ON/OFF ratio, on-resistance, and breakdown showing the potential of this growth method for future Ga_2O_3 technology.

Four Ga_2O_3 films were grown via high-temperature (1050 °C) low-pressure chemical vapor deposition (HT-LPCVD) [25,26,34–37] on Sn-doped (001) and (010) oriented Ga_2O_3 substrates (commercially acquired from Novel Crystal Technology, Inc.), labeled as S1, S2, S3, and S4. The substrates were first cleaned with isopropanol, rinsed with de-ionized water, and dried with nitrogen flow prior to loading to the growth system. High-purity metallic Ga (Alfa Aesar, 99.999

99%) was used as the Ga precursor, which was placed in a quartz crucible the upstream of the substrates. High-purity O_2 gas was used as the O precursor. In this study, a fixed flow rate of O_2 at 30 standard cubic centimeters per minute (sccm) was used. Argon (Ar) was used as a carrier gas with a flow rate of 200 sccm. Diluted silicon tetrachloride ($SiCl_4$) was used as an n-type dopant source. The growth temperature was set at 1050 °C, and the growth pressure was fixed at ~2.8 Torr, the growth duration was 50-60 min. Under this growth condition, the growth rates of 13, 15.6, 21, and 19 μm/h were obtained for S1, S2, S3, and S4 respectively. The detailed growth conditions of Ga_2O_3 films on Sn-doped Ga_2O_3 substrates are listed in Table I. As specified in the Table, there is macro-scale roughness observed in these films (see Supplementary Materials). The surface morphology of the films in the smooth area was characterized by atomic force microscopy (AFM). Fig. 1 shows the AFM images of the 5 × 5 μm^2 scan for the homoepitaxial thin films surfaces. The RMS values for the S1, S2, S3, and S4 homoepitaxial thin films were 7.35 nm, 6.95 nm, 5.99 nm, and 1.41 nm respectively. The film morphology for S1 is different from other samples. The RMS roughness values for S1, S2, and S3 were higher than previously reported thin films grown by LPCVD (~3-4 nm) [35,38]. This was due to the much faster growth rate of the films grown in this study compared to the ones grown previously. Although in micron-scale (for 5 × 5 μm^2 scan), S1 seems to have the roughest surface out of the four samples surfaces, this sample contains the most area with smooth surface compared to the other three samples (see Supplementary Materials).

The LPCVD β-Ga_2O_3 films crystalline quality was characterized by Bruker D8 Discover XRD. Figure 2(a) and 2(b) show the XRD ω-2θ scan of (010) and (001) β-Ga_2O_3 homoepitaxial films grown on (010) and (001) β-Ga_2O_3 substrates, respectively. Even at the high growth temperatures where other phases of Ga_2O_3 are known to be stable [39–41], no peaks associated with α, γ, δ, and ε

phases of Ga_2O_3 were detected, which indicates the high-quality β-Ga_2O_3 homoepitaxial thin films on (010) and (001) β-Ga_2O_3 substrates.

Schottky diodes are used to further verify the electrical characteristics of these films. A schematic cross-section of the Schottky diode structures fabricated is shown in Fig. 3(a). The device fabrication commenced with BCl_3-based reactive-ion etching (RIE) of the backside, a total of 1 μm thick Ga_2O_3 was etched in this step. A Ti/Au Ohmic metal stack was deposited by electron beam evaporation followed by rapid thermal annealing (RTA) in N_2 ambient at 470 ^{0}C for 1 minute. Finally, the top Ni/Au Schottky contacts were defined by electron beam lithography. After device fabrication, current density-voltage *(J-V)* measurements were performed using HP 4155B semiconductor parameter analyzer. Schottky barrier height ($\boldsymbol{\Phi}_B$), ideality factor (η), and specific on-resistance ($R_{on,sp}$) for each sample was calculated using the method of Cheung *et al.*[42]. The measurements were repeated for elevated temperatures up to 250 ^{0}C. A room temperature reverse breakdown measurement was also performed.

As seen in Fig. 3(b), all the samples show rectifying behavior. In the semi-log Fig. 3(c), at low bias voltage ($V < 1$ *V*), the current varies linearly. At high bias voltage ($V > 1$ *V*), the linearity is deviated with increasing bias voltage due to the series resistance for all four samples. The measured forward bias *I-V* characteristics were analyzed using the ideal thermionic emission (TE) model [43,44]

$$J = J_S \left(e^{\frac{qV}{\eta kT}} - 1\right), \tag{1}$$

Where

$$J_S = A^* T^2 \left(e^{\frac{q\boldsymbol{\Phi}_B^{IV}}{\eta(T)kT}}\right) \tag{2}$$

Here, J_S is the saturation current density, η is the ideality factor, V is the forward bias voltage, T is the absolute temperature, q is the electron charge, k is the Boltzmann constant, $\boldsymbol{\Phi}_B^{JV}$ is the apparent Schottky barrier height, A is the effective diode area, and A^* is the effective Richardson constant, calculated to be 41.04 $Acm^{-2}T^{-2}$ [45]. The electrical properties extracted from the *J-V* measurements are shown in Table II. The accuracy of $\boldsymbol{\Phi}_B$ obtained from Eqn. (2) depends on the corresponding value of the ideality factor. The measured Schottky barrier height from Eqn. (2) is closer to the actual value if the ideality factor is close to 1, as described by Wagner *et al.* [46]. As the ideality factor is >1 in our case, the corrected Schottky barrier height, $\boldsymbol{\Phi}_B$ is obtained using the following equation [46]

$$\boldsymbol{\Phi}_B = \left[\boldsymbol{\Phi}_B^{JV} - \left(\frac{\eta-1}{\eta}\frac{kT}{q} ln\frac{N_C}{N_D}\right)\right]\eta \quad (3)$$

Where N_C is the conduction density of states for Ga_2O_3 calculated using electron effective mass of 0.34 m_0 with all other constants at their standard values [47,48]. N_D is the donor concentration of the Ga_2O_3.

As seen in Table II, S1 has excellent rectifying behavior with the highest forward current densities (527.5 A/cm^2 at 5 V), lowest specific on-resistance, lowest reverse leakage current (2.24×10^8 A/cm^2 at -5 V), and highest ON-OFF ratio (>10^{10}). The ideality factor (η) for S1 is 1.37 which could be attributed to the roughness seen in AFM. While the ideality factor values of S1 and S2 are closer to unity, S3 and S4 have higher ideality factors representing the dominance of non-ideal effects such as spatial inhomogeneity of the Schottky barriers. Inhomogeneous Schottky barriers are believed to result from surface roughness at the metal-semiconductor interfaces. The highest ideality factor was observed for S3 which has the highest growth rate, the larger value of η represents the dominance of non-ideal effects such as thermionic field emission,

and/or trap-assisted tunneling currents, metal adhesion quality, and interface quality. The calculated Schottky barrier heights for S2, S3, and S4 agree with the values reported in the literature [49,50]. For S1, the obtained Schottky barrier height is 0.99 eV, which is at the lower end but within the range of previously reported values [49,51]. However, for the S1 diode, the values of specific on-resistance, $R_{on,sp}$ was found to be 4.29 mΩ-cm^2, which is the lowest among the four samples. The maximum value of $R_{on,sp}$ has been found for S4, as seen in Table II. The macroscale roughness and growth rate seem to correlate with the $R_{on,sp}$ as with the increase of surface roughness, increased of $R_{on,sp}$ is observed.

Fig. 4(a) shows the temperature dependence of semi-logarithmic of *J-V* characteristics of the S1 sample (see Supplementary Materials for other samples). The forward *J-V* curves of all the samples show that in low bias voltage, the turn-on voltage shifts gradually toward the lower bias side with increasing temperature representing an increase of the thermal contribution of electron transport. At higher bias voltages, the linearity has deviated with the increase of bias voltage due to the increase of the series resistance for all four structures. The series resistance component dominates the transport and increases with the increase of temperature. The reverse *J-V* characteristics show that with an increase in temperature the leakage current densities increase almost monotonically for all four samples. This is because electrons gain higher energies at elevated temperatures to climb over the metal-semiconductor barrier which attributes leakage. As a result, ON-OFF current ratios reduce by two to four orders of magnitude due to an increase of reverse current densities with temperature.

Fig. 4(b) shows a plot of the temperature dependence of ideality factor, η, and the barrier height, $\boldsymbol{\Phi_B}$ of S1(see Supplementary Materials for other samples). The ideality factor, η was found to decrease linearly from 1.37 to 1.13 when room temperature increases to 150^{0}C. Beyond this

temperature, η starts increasing with temperature. The reduction in the values of η with an increase of temperature up to a certain temperature is observed when there is marginal improvement in the pure thermionic emission current part over thermionic field emission current transport mechanism in the device. However, the increase of η with temperature beyond that certain temperature has often been accredited to the current transport mechanism not following the ideal thermionic emission theory. Schottky barrier inhomogeneities in the transport current due to different interface qualities can be the cause of this nonideal dependence. Pure thermionic emission barrier height reduces with the elevation of temperature [52]. $\boldsymbol{\Phi}_B$ decreases from 1 eV to 0.92 eV when temperature increases from room temperature to 100^0C which indicates they are corresponding to thermionic emission. Interestingly, a gradual increase in $\boldsymbol{\Phi}_B$ from 0.92 eV to 1.13 eV has been observed when temperature increases from 100 ^{0}C to 250 ^{0}C. The slight increase of $\boldsymbol{\Phi}_B$ beyond 100 ^{0}C is due to the deviation of the dominant conduction mechanism, from thermionic emission current to thermionic field emission or field mission. An almost similar trend of dependency of η and $\boldsymbol{\Phi}_B$ on the temperature is observed for the other three samples as well. Such non-monotonic behavior for η and $\boldsymbol{\Phi}_B$ has also been observed in previous studies [48].

Fig. 5 shows a plot of specific on-resistance, $R_{on,sp}$ as a function of temperature. As seen in Fig. 5(a), $R_{on,sp}$ was found to increase linearly from a value of 4.29 mΩ-cm^2 to 8.82 mΩ-cm^2 for S1 when temperature increases from room temperature to 250 ^{0}C. On the contrary, $R_{on,sp}$ decreases linearly from 117.38 mΩ-cm^2 to 12.08 mΩ-cm^2 for S2 as temperature increases from room temperature to 250 ^{0}C, as seen in Fig. 5(b). S3 and S4 also follow the same trend as S2. $R_{on,sp}$ is a combined result of contact and bulk resistance values. Bulk resistance increases with increasing temperature due to the decrease in mobility with the elevation of temperature. The contact

resistance decreases with increasing temperature in Ga_2O_3 due to the reduction of the barrier height [53]. In the case of S1, bulk resistance dominates whereas contact resistance dominates over the bulk resistance for S2, S3, and S4. However, any other explanations for the S2, S3, and S4 remain plausible. Future work will investigate such discrepancies for Ni/Au Schottky contacts for LPCVD Ga_2O_3 material. The reverse *J-V* characteristics of S1 and S2 diodes are shown in Fig. 6. A destructive breakdown is observed for S1 with a breakdown voltage (V_{br}) of -385 V and S2 with V_{br} = -435 V. The moderate breakdown voltage is limited by the lower barrier height, high surface roughness of the samples, and edge effects of the anode. Using field-plates, trench MOS diodes, and electric field engineering will improve the breakdown voltage. Improving surface smoothness through chemical mechanical polishing is also expected to significantly improve reverser characteristics. Nevertheless, the modest breakdown voltages show that LPCVD films can be used for high-voltage devices. The samples S1 and S2 with growth rates of 13 and 15.6 μm/h show reliable device characteristics, while films with growth rates >19 μm/h show high resistances.

In conclusion, four different Si-doped homoepitaxial Ga_2O_3 thin films were grown on Sn-doped (010) and (001) Ga_2O_3 substrates via LPCVD with fast growth rates varying from 13 μm/h to 21 μm/h. (001) and (010) homoepitaxial Ga_2O_3 thin films with RMS surface roughness varying from 1.41nm to 7.35 nm were obtained. Though the RMS value is highest, Si-doped homoepitaxial Ga_2O_3 thin films on (001) Sn-doped Ga_2O_3 substrate grown at 13 μm/h growth rate turns out to be the best among the four samples as it contains less macro-scale roughness, offering the maximum amount of smooth surface for device fabrication. We also demonstrated Schottky diodes using the four LPCVD-grown homoepitaxial Ga_2O_3 films. Schottky diodes fabricated on (001) Sn-doped Ga_2O_3 substrate followed by Si-doped homoepitaxial Ga_2O_3 thin

films exhibits the highest forward current densities (527.56 A/cm^2 at 5 V), lowest leakage current (2.24×10^8 A/cm^2 at -5 V), highest ON-OFF ratio (>10^{10}), lowest specific On-resistance (4.29 mΩcm^{-2}), and breakdown voltage of -385 V indicating the viability of LPCVD as a growth technique for vertical power electronic devices. The specific On-resistance of this sample also increases with increasing temperature, from 4.29 mΩ-cm^2 at room temperature to 8.82 mΩ-cm^2 at 250 ^{0}C. For all the samples, ideality factor and barrier height decrease first with temperature elevation and increase with temperature increase beyond a certain temperature. Overall, the growth rate of 13-15.6 μm/h turns out to be optimum for fabricating vertical devices on LPCVD grown β- Ga_2O_3 samples in terms of surface morphology and reliable device characteristics. The reported work shows the promise of the LPCVD growth technique with a high growth rate to grow β- Ga_2O_3 on native substrates for fabricating vertical power devices with thick active layers.

Acknowledgments

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Table Captions:

Table I. HT-LPCVD growth conditions of β-Ga_2O_3 films on Sn-doped β-Ga_2O_3 substrate with

1050 ^{0}C temperature and 0.5 sccm diluted $SiCl_4$ flow

Table II. Extracted electrical properties at room temperature from *J-V*, and *J-V-T* measurements for S1, S2, S3, and S4

Figure Captions:

Fig. 1. AFM images of HT-LPCVD grown β-Ga_2O_3 films on (a) (001) Sn-doped β-Ga_2O_3 substrate, film thickness~13μm (sample S1); (b) (001) Sn-doped β-Ga_2O_3 substrate, film thickness~21μm (sample S3); (c) (010) Sn-doped β-Ga_2O_3 substrate, film thickness~13μm (sample S2); (d) (010) Sn-doped β-Ga_2O_3 substrate, film thickness~16μm (sample S4).

Fig. 2. XRD ω-2θ scan of (a) (001); and (b) (010) β-Ga_2O_3 homoepitaxial films grown on (001) and (010) β-Ga_2O_3 substrates, respectively. Prominent characteristic diffraction peaks from (a) (020) plane; and (b) (00l) planes from the wide scan range.

Fig. 3. (a) Schematic cross-section of the vertical Schottky diode structures fabricated on LPCVD (010 and 001) β-Ga_2O_3 substrates. (b) Room temperature forward current density (*J) vs* Voltage *(V)* characteristics for S1, S2. S3, and S4 Schottky barrier diodes. Inset shows forward characteristics of S2, S3, and S4. (c) Room temperature semilogarithmic current density (*J) vs* Voltage *(V)* characteristics for S1, S2. S3, and S4 Schottky barrier diodes.

Fig. 4. (a) Semi-logarithmic current density (*J) vs* Voltage *(V)* characteristics at different temperatures showing variation in forward and reverse current densities with temperature for S1. Inset shows the forward *J-V* characteristics in the high-bias region. (b) The temperature dependence of ideality factor, η, and the barrier height, $\boldsymbol{\Phi}_B$ of S1 Schottky diode.

Fig. 5. The temperature dependence of specific On-resistance, $R_{on,sp}$ of (a) S1 (b) S2 Schottky diodes.

Fig. 6. (a) Reverse *J-V* characteristics of S1 β-Ga_2O_3 Schottky diode, where the destructive breakdown was observed at V_{br} = -385 V. (b) Reverse *J-V* characteristics of S2 β-Ga_2O_3 Schottky diode, where the destructive breakdown was observed at V_{br} = -435 V.

Tables:

Table I.

Sample No	Substrate Orientation	Estimated Doping	Growth Duration	Estimated Thickness[b] (μm)	Growth Rate (μm/h)	% Smooth area of overall sample	Backside Growth
S1	(001)	1.0×10^{16}	1 h.	13	13	75	Less
S2	(010)	1.2×10^{16}	50 min.	13	15.6	60	Medium
S3	(001)	1.5×10^{16}	1 h.	21	21	40	More
S4	(010)	2×10^{16}	50 min.	16	19	45	Medium

a Estimated doping is measured from co-loaded c-sapphire samples
b Estimated thickness is measured from co-loaded Fe-doped substrates with AlGaO buffer

Table II.

Sample No	Ideality Factor, η	Φ_B *(eV)*	$R_{on,sp}$ ($m\Omega cm^{-2}$)	Leakage current @ -5V (A/cm^2)
S1	1.37	1.0	4.29	2.24×10^{-8}
S2	1.28	1.5	117.38	1.464×10^{-7}
S3	2.36	1.58	528.65	4.374×10^{-7}
S4	1.63	1.53	62550	9.745×10^{-8}

Figures:

Fig. 1.

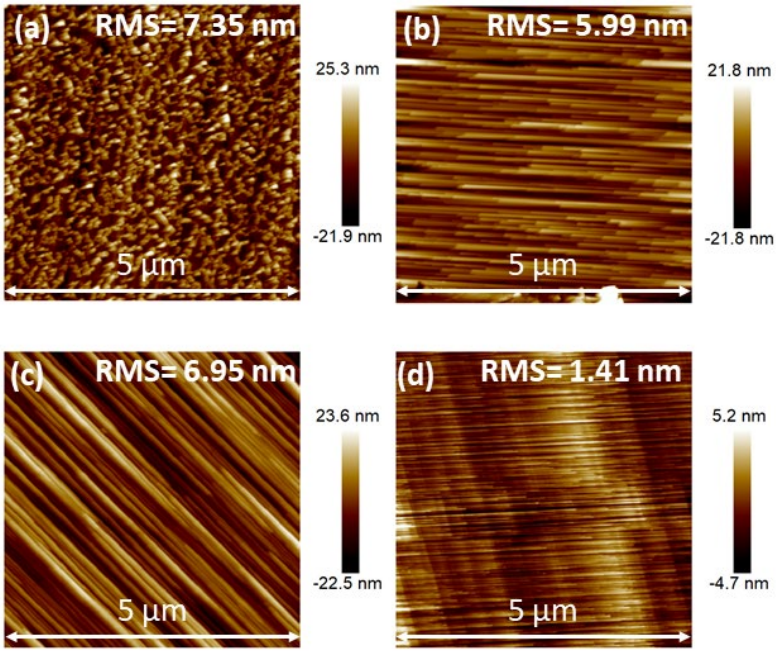

(a)
RMS= 7.35 nm
25.3 nm
-21.9 nm
5 µm
(b)
RMS= 5.99 nm
21.8 nm
-21.8 nm
5 µm
(c)
RMS= 6.95 nm
23.6 nm
-22.5 nm
5 µm
(d)
RMS= 1.41 nm
5.2 nm
-4.7 nm
5 µm

Fig. 2.

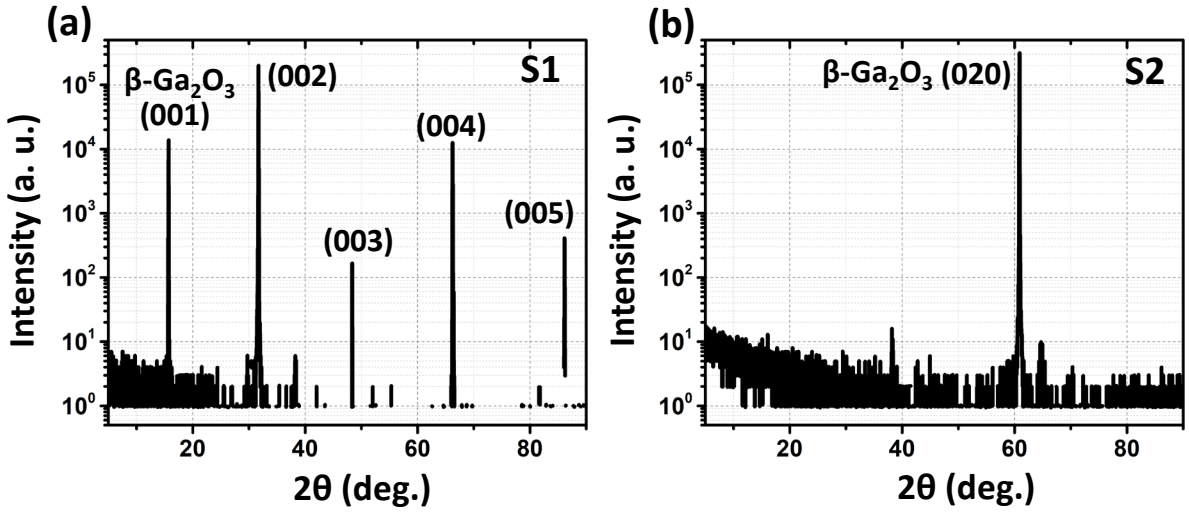

(a)
β-Ga2O3
(001)
(002)
(003)
(004)
(005)
S1
Intensity (a. u.)
2θ (deg.)
(b)
β-Ga2O3 (020)
S2
Intensity (a. u.)
2θ (deg.)

Fig. 3.

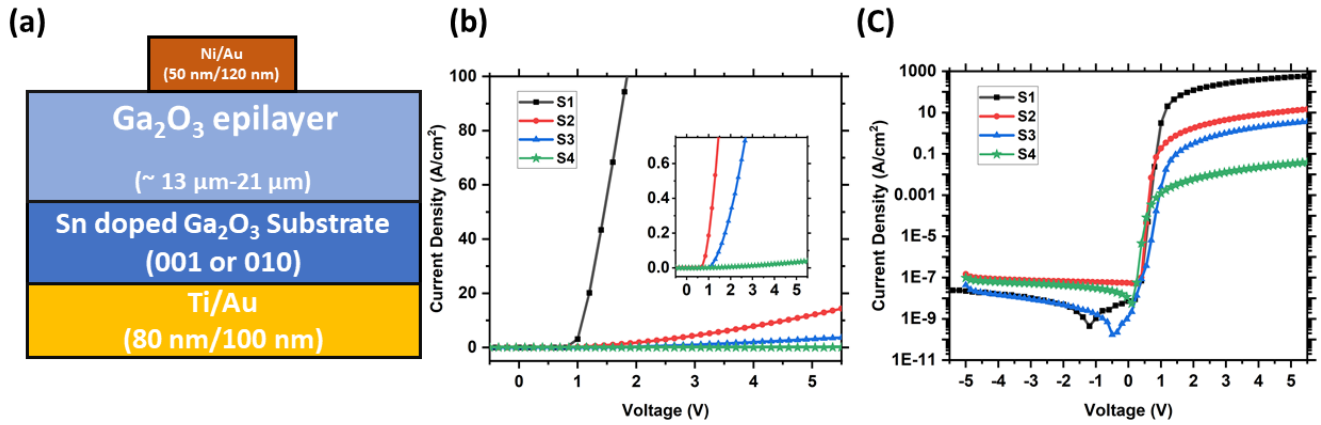

(a)
Ni/Au
(50 nm/120 nm)
Ga2O3 epilayer
(~ 13 µm-21 µm)
Sn doped Ga2O3 Substrate
(001 or 010)
Ti/Au
(80 nm/100 nm)
(b)
Current Density (A/cm2)
Voltage (V)
S1
S2
S3
S4
(C)
Current Density (A/cm2)
Voltage (V)
S1
S2
S3
S4

Fig. 4.

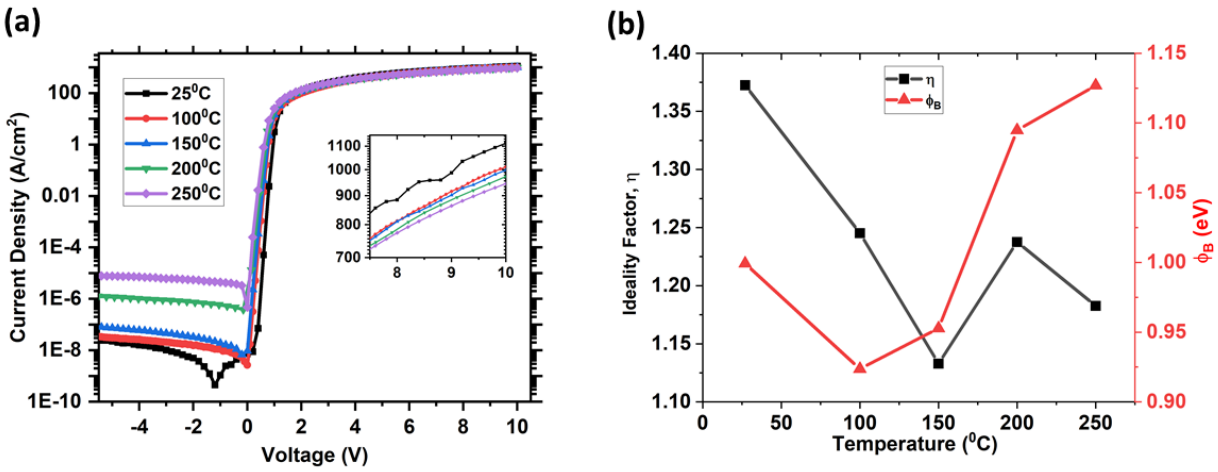

(a)
Current Density (A/cm2)
Voltage (V)
25°C
100°C
150°C
200°C
250°C
(b)
Ideality Factor, η
ϕB (eV)
Temperature (°C)
η
ϕB

Fig. 5.

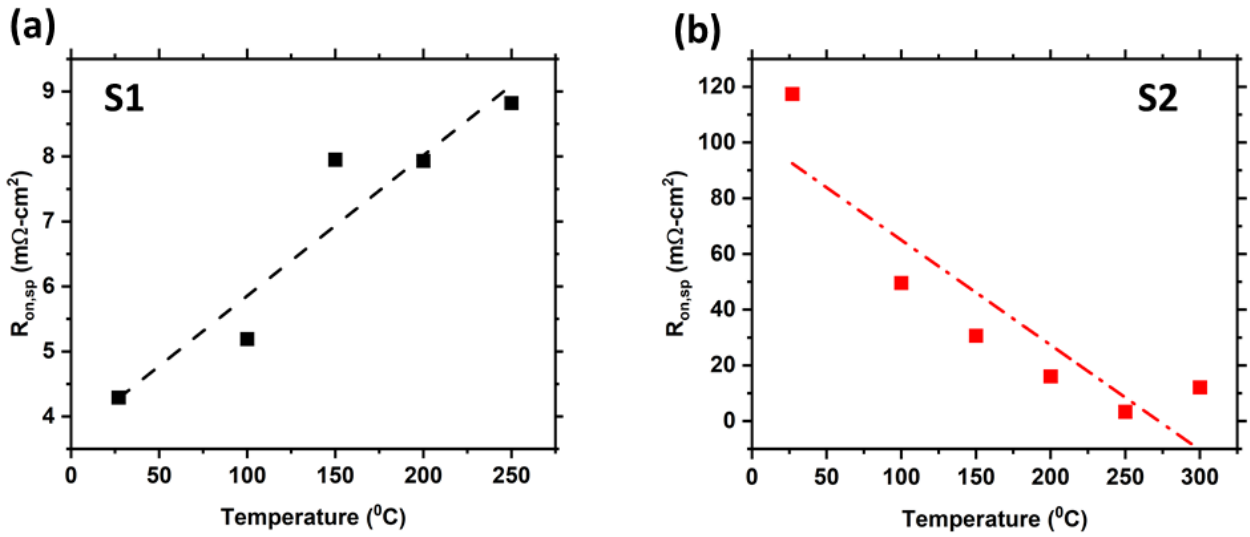
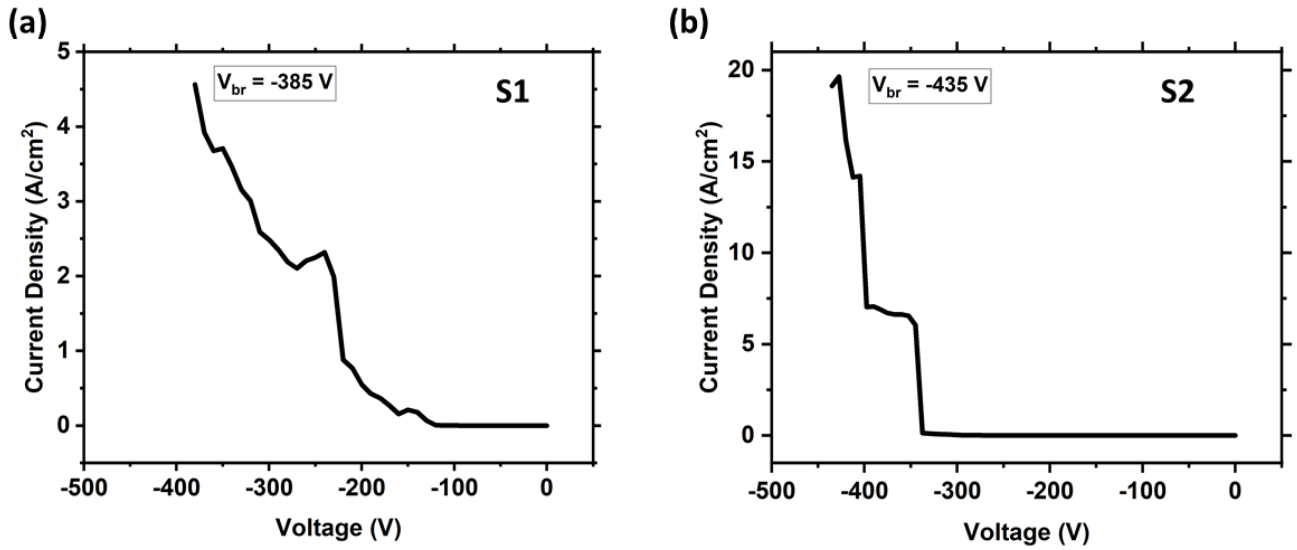

(a)
S1
$R_{on,sp}$ (mΩ-cm^2)
Temperature (^{0}C)
(b)
S2
$R_{on,sp}$ (mΩ-cm^2)
Temperature (^{0}C)

Fig. 6.


(a)
V_{br} = -385 V
S1
Current Density (A/cm^2)
Voltage (V)
(b)
V_{br} = -435 V
S2
Current Density (A/cm^2)
Voltage (V)