

Temperature dependent pulsed IV and RF characterization of β -(Al_xGa_{1-x})₂O₃/Ga₂O₃ hetero-structure FET with *ex situ* passivation

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ABSTRACT

In this work, we report a study of the temperature dependent pulsed current voltage and RF characterization of b-(Al_xGa_{1-x})₂O₃/Ga₂O₃ hetero-structure FETs (HFETs) before and after silicon nitride (Si₃N₄) passivation. Under sub-microsecond pulsing, a moderate DC-RF dispersion (current collapse) is observed before passivation in gate lag measurements, while no current collapse is observed in the drain lag measurements. The dispersion in the gate lag is possibly attributed to interface traps in the gate-drain access region. DC-RF dispersion did not show any strong dependence on the pulse widths. Temperature dependent RF measurements up to 250 °C do not show degradation in the cutoff frequencies. After Si₃N₄ deposition at 350 °C, a shift of the threshold voltage is observed which changed the DC characteristics. However, the current collapse is eliminated; at 200 ns pulse widths, a 50% higher current is observed compared to the DC at high drain voltages. No current collapse is observed even at higher temperatures. RF performance of the passivated devices does not show degradation. These results show that *ex situ* deposited Si₃N₄ is a potential candidate for passivation of b-(Al_xGa_{1-x})₂O₃/Ga₂O₃ HFETs.

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b-Ga₂O₃ is an extensively investigated ultra-widebandgap semiconductor for next generation power electronics and RF applications because of its favorable material properties.¹ Due to its larger calculated Baliga figure of merit (BFoM),² it has been explored for high voltage power devices. Several groups have reported transistors and diodes with kV range breakdown voltages^{3–7} further validating its potential. Additionally, due to its high calculated electron saturation velocities,⁸ b-Ga₂O₃ (Ga₂O₃) has a higher Johnson's figure of Merit (JFoM) making it attractive for potential RF applications such as high power amplifiers and GHz switches. Due to its large bandgap, Ga₂O₃ devices can also operate at higher temperatures. Both MOSFETs and MESFET devices with high frequency have been reported.^{9,10} Recently, a record current gain cut off frequency (f_T) of 30 GHz and a power gain cut off frequency (f_{MAX}) of 37 GHz have been reported for b-(Al_{0.19}Ga_{0.81})₂O₃/Ga₂O₃ (AlGaO/GaO) hetero-structure FETs (HFETs)¹¹ with ultra-scaled gate lengths and regrown Ohmic contacts.

Another important aspect of high frequency performance of a device is DC-RF dispersion. This is typically characterized by a decrease in the drain current and trans-conductance in unpassivated devices at higher frequencies resulting in lower RF output power. The

DC-RF dispersion or current collapse is caused by the finite amount of time taken by any traps, located either at an air/device interface in a gate drain access region or in the bulk semiconductor under the gate in response to either gate or drain voltage transients. Pulsed current voltage (IV) measurements are popular method to analyze the DC-RF dispersion and to identify the location of the traps.^{12–15}

There have been a number of studies on the pulsed IV characterization for Ga₂O₃ devices. Wong *et al.*¹⁶ reported no current collapse at 100 ns pulse width with SiO₂ passivation in high voltage devices. Moser *et al.*¹⁷ reported large signal power performance with continuous and pulsed conditions^{17,18} and found that the interface trap in the gate drain region is the source of dispersion. Singh *et al.*¹⁹ reported that Al₂O₃/SiO₂ passivated devices do not show any current collapse at 1 ns pulse width at room temperature. McGlone *et al.*^{20–22} explored buffer traps in delta doped MESFETs using the double pulsed IV condition. Joishi *et al.*²³ used 5 ns double pulsed measurement to show that *in situ* passivation by an UID Ga₂O₃ layer can improve the current significantly even though the channel was exposed to reactive ion etching (RIE). However, sub-microsecond pulsed IV is necessary to understand the device performance at GHz frequencies as is the case for AlGaIn/GaN devices.^{15,24}

Recently, sub-microsecond pulsed-IV characterization of gate recessed Ga₂O₃ MOSFETs was reported, which shows severe DC-RF dispersion in unpassivated devices.²⁵ Although dispersion was reduced (50%) after silicon nitride (Si₃N₄) passivation, it was not eliminated. It is important to completely eliminate current collapse in Ga₂O₃ devices to achieve the predicted RF performance. In this work, we report a temperature dependent pulsed IV characterization of AlGaO/GaO HFETs. We show that *ex situ* deposited Si₃N₄ passivation can eliminate current collapse up to 200 ns pulse widths. We also report the temperature dependent high frequency performance of AlGaO/GaO HFETs.

A cross section schematic of the completed AlGaO/GaO HFET is shown in Fig. 1(a). Details of ozone MBE growth and device fabrication are discussed in Refs. 11 and 26. The salient features of the device are the use of source/drain regrowth for contacts and the absence of any RIE exposure to the device access regions. It has been reported that RIE damage to the channel layer can cause surface traps resulting in significant DC-RF dispersion.^{18,25} The gate length (L_G) was scaled to 160–200 nm, and the source access distance (L_{SG}) was scaled down to 55 nm using electron beam lithography. After pre-passivation electrical characterization, a 300 nm thick low stress Si₃N₄ was deposited using plasma enhanced chemical vapor deposition (PECVD) at 350 °C temperature with 20 sccm SiH₄ and 30 sccm NH₃ at 1900 mTorr pressure. Standard solvent clean was carried out before the deposition. Finally, Si₃N₄ was removed using CF₄ based RIE on top of the contacts for electrical characterization. The contacts have a co-planar waveguide (CPW) layout for high frequency measurements.

Figure 1(b) shows the output characteristics of a 160 nm gate length unpassivated device at room temperature and 250 °C, and the device shows a normally off behavior (V_{th} ≈ 0.5 V) with lower drain current at higher temperatures. The reduction in the drain current at higher temperatures is due to the reduction in the channel mobility at higher temperatures. For DC-RF dispersion studies, gate lag, drain lag, and double pulsed measurements were carried out. In the drain lag, the drain was pulsed from the off state (0 V) to the on state (5 or 7 V) (referred to as drain turn-on) while the gate bias was constant. For gate lag, the gate terminal was pulsed from the off state (below V_{th}) to the on state (referred to as gate turn-on) while maintaining a constant drain bias. Finally, for a double pulsed technique, both gate and drain were pulsed from the off state to the on state (or vice versa) and a combination of on and off biases. The pulsed IV measurement was carried

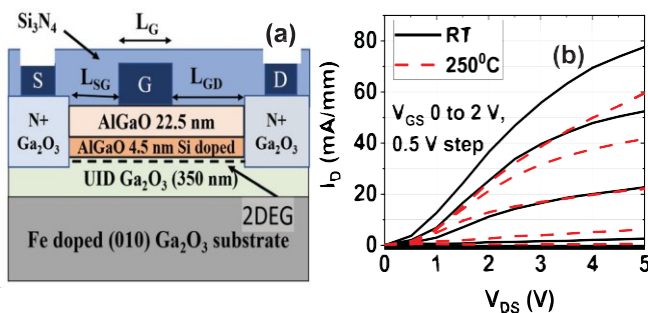


FIG. 1. (a) Final cross section of a device after passivation. The gate metal stack is Pt/Au ≈ 20/180 nm and (b) DC output curve for a device (L_G ≈ 160 nm) at room temperature and 250 °C.

out using an Auriga AU-5 high voltage Pulsed IV setup with 20 nano-second (ns) rise and fall time, and the pulse width was varied from 1 ms to 200 ns with low duty cycle (<1%). The system was calibrated at each temperature before measuring the devices. The drain current collapse is quantified by

$$DI_{cc} \approx \frac{I_{d,DC} - I_{d,PW}}{I_{d,DC}}; \quad (1)$$

where I_{d,DC} is the drain current value during DC measurement and I_{d,PW} is the drain current measured at the corresponding pulse width. The gate current was monitored during the pulsed measurements and was always very low compared to the drain current.

Drain lag measurements are used to study buffer traps/bulk traps in the device as they respond to a drain pulse.²⁷ Figure 2(a) shows the DC and drain turn-on measurements of the unpassivated device at constant gate bias, and negligible dispersion is observed. A slight increase in the current is observed at smaller pulse widths, which could be due to the reduced self-heating effect. These measurements rule out the presence of any buffer traps as was the case for ozone MBE grown MOSFET devices.²⁵ Figure 2(b) shows the DC and gate pulsed output curve of the same device; as seen in the figure, a moderate DC-RF dispersion or current collapse (22%) is observed. The recessed channel MOSFETs by Vaidya and Singiseti had increasing DC-RF dispersion with decreasing pulse width, and 60% current collapse was reported at 200 ns pulse width. Yet here, we observe that the amount of current collapse does not depend strongly on the pulse widths. The dispersion can be attributed to the interface traps either under the gate or in the gate drain access region forming a virtual gate.^{13–15} Figure 2(c) shows

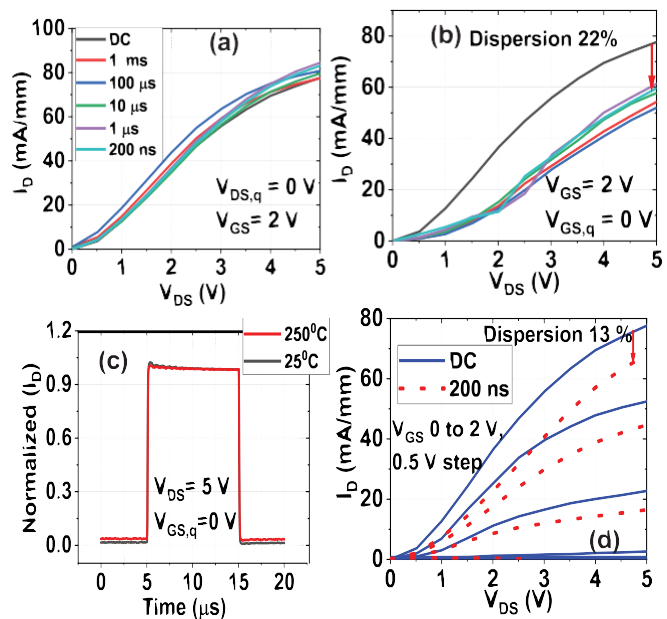


FIG. 2. (a) Drain lag/pulse measurement at V_{GS} ≈ 2 V showing no DC-RF dispersion, (b) gate lag measurement at V_{GS} ≈ 2 V showing DC-RF dispersion, (c) temperature dependent I_D pulse shape for 10 μs gate turn on pulse measured at V_{GS} ≈ 2 V before passivation, and (d) double pulse measurement (V_{GS,q} ≈ 0 V, V_{DS,q} ≈ 0 V) showing reduced current collapse at room temperature.

the measured drain current transient for the 10 ns pulse gate turn-on signal, and the pulse shows fast drain current turn-on and turn-off. This is in contrast to the recessed channel MOSFETs,²⁵ where slow turn-on and turn-off was observed which was attributed to RIE induced traps. The observed pulse shape explains why the DC-RF dispersion does not depend on pulse widths. The pulse shape remains unchanged even at 250°C as seen in Fig. 2(c).

Double pulsed IV-measurements, where both the drain and gate are pulsed from different gate and drain quiescent points ($V_{GS,q}$, $V_{DS,q}$), can simulate the device conditions during its operation as an amplifier or switch, thus provide more insight. Figure 2(d) compares the DC and double pulsed output characteristics, and $V_{GS,q} \approx 0$ and $V_{DS,q} \approx 0$ were used to minimize self-heating effects. At the highest pulsed or non-quiescent gate bias ($V_{GS,q} \approx 2$ V), a low dispersion of 13% is observed, which is lower than the current collapse in the gate pulsed measurements. This current collapse is attributed to the possible traps in the gate-drain access region that were responsible to the current collapse seen in Fig. 2(b). Here, the dispersion was observed without a finite gate-drain bias in the quiescent condition. The traps could be charged due to the built-in bias or charged after pulses have been applied. Further analysis is needed in the future to fully understand the origin of this. Double pulsed I_{DS} - V_{GS} transfer curves (see the [supplementary material](#)) using different quiescent bias conditions did not show any change in the threshold voltage ruling out traps under the gate,^{14,19,28} leaving the gate-drain access region interface traps as the likely source of the observed dispersion. It is noted that the presence of deep-level traps is not probed in these pulsed IV measurements.

Figure 3(a) shows the measured current collapse as a function pulse width for different quiescent gate and drain biases. All I_D values were measured at $V_{GS} \approx 2$ V and $V_{DS} \approx 5$ V for this calculation. The

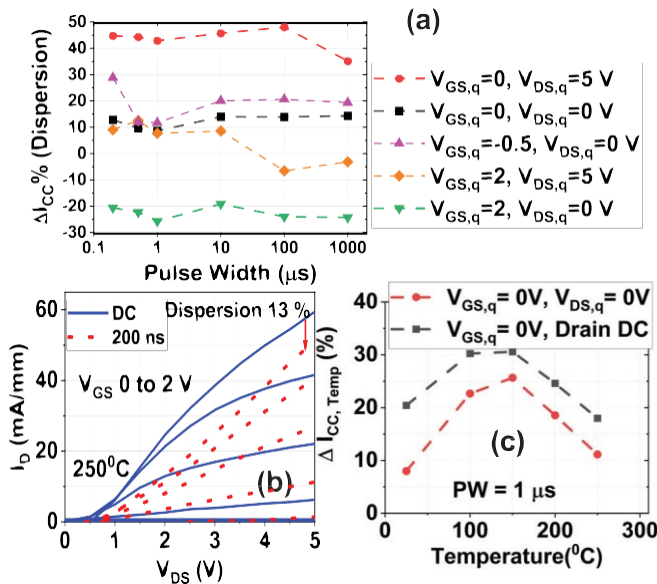


FIG. 3. (a) Comparison of current collapse for output curves at different quiescent bias conditions before passivation ($L_G \approx 160$ nm), (b) DC and pulsed IV curve ($V_{GS,q} \approx 0$ V, $V_{DS,q} \approx 0$ V) at 250°C showing similar dispersion at room temperature, and (c) temperature dependent dispersion for 1 μs PW showing lower current collapse for the double pulsed technique.

maximum current collapse (40%) is observed for $V_{GS,q} \approx 0$ V and $V_{DS,q} \approx 5$ V; the larger gate-drain voltage and pinch off condition lead to longer virtual gate formation, hence the increased current collapse. In contrast, for $V_{GS,q} \approx 2$ V and $V_{DS,q} \approx 0$ V, no current collapse is observed, instead a small increase in the current is seen. In this condition, the device is in the on state, and the traps are filled, which eliminated the current collapse,¹⁷ while the reduced self-heating in pulsed conditions likely leads to a slight increase in the current. $V_{GS,q} \approx -0.5$ V gave a higher dispersion compared to the $V_{GS,q} \approx 0$ quiescent condition, because more negative voltage causes more trapping and higher current collapse. The response of other quiescent conditions is an interplay of trapping and self-heating effects.²⁹

Temperature dependent pulsed IV measurements were also carried out up to 250°C. As seen in Fig. 3(b), a low current collapse of 13% is observed at 250°C for 200 ns pulse width similar to the case at room temperature. Drain lag, gate lag, and double pulsed measurements at higher temperatures show a similar trend as room temperature for the DC-RF dispersion (similar to Fig. 2). Figure 3(c) shows the double pulsed current collapse at 1 μs pulse width as a function of temperature. It shows a non-monotonic behavior with temperature with highest dispersion at 150°C. This trend is the result of complex interplay of several effects including trapping self-heating effects and the stage temperature. With an increase in temperature, traps can respond faster, while the self-heating effects could be reduced because of overall decrease in the current at higher temperatures [see Fig. 1(b)]. A more careful analysis, including thermal simulations, is needed to fully understand the temperature dependent pulsed IV data.

In order to eliminate the observed current collapse in the AlGaO/GaN HFETs, a Si_3N_4 passivation was investigated. It has been used to reduce or eliminate DC-RF dispersion/current collapse in AlGaO/GaN devices.^{30–33} Interestingly, after passivation, a significant change in the threshold voltage to -1 V is observed (see the [supplementary material](#)). It is attributed to possible intermixing of Au and Pt in the gate stack, resulting in a lower Schottky barrier, although introduction of traps under gate is not completely ruled out. Intermixing of Pt and Au at 200°C is reported in Ref. 34. The DC output characteristics of a HFET after passivation are shown in Fig. 4(a). The decreased DC drain current and transconductance can be attributed to increased sheet

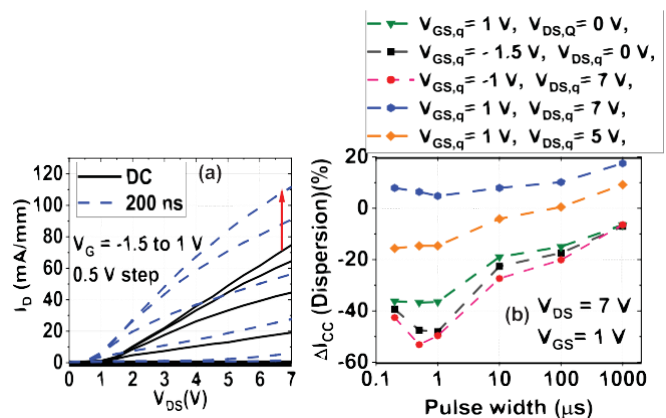


FIG. 4. (a) Output curve ($L_G \approx 200$ nm) after passivation ($V_{GS,q} \approx -1.5$ V, $V_{DS,q} \approx 0$ V) using the double pulse method and (b) comparison of current collapse at the double pulse method using different quiescent bias conditions after passivation.

resistance in the access regions due to plasma damage during Si₃N₄ deposition at 350 °C, which is higher than previous reports.^{25,35} In addition, as seen in the DC curves, the contact linearity has changed. All these changes in the DC characteristics need to be eliminated in an ideal passivation scheme. Further optimization of the Si₃N₄ process is required. In the subsequent analysis, the pulsed measurements are from V_{GS} -1.5 to 1 V (pinch off to the on state) to keep comparable gate overdrive ($V_{\text{overdrive}} = \frac{1}{4} V_{\text{GS}} - V_{\text{th}} \approx 2 \text{ V}$) as before passivation and comparable on-state DC drain currents.

Figure 4(a) shows the measured output curves for the passivated device by the DC and double pulse (200 ns pulse width) technique using V_{GS,q} $\frac{1}{4}$ -1.5 V and V_{DS,q} $\frac{1}{4}$ 0 V. We do not observe any current collapse due to DC-RF dispersion for all pulse widths (not shown here). At 200 ns pulse widths, the drain current is increased by 50% compared to DC at higher drain biases. This demonstrates that Si₃N₄ passivation can mitigate current collapse in AlGaO/GaO HFETs. Similar result was observed for gate lag measurements too. Even at 200 °C, no current collapse was observed (see the [supplementary material](#)). Surprisingly, pulsed measurements show higher currents than DC even at lower drain biases. This is observed for all pulse widths (see the [supplementary material](#)). This effect could be due to the effect of traps in the drain access region, which were likely introduced in the Si₃N₄ deposition process.

Figure 4(b) compares the DC-RF dispersion of the passivated HFET at different quiescent bias conditions as a function of the pulsed width. Current dispersion was compared at V_{GS} $\frac{1}{4}$ 1 V and V_{DS} $\frac{1}{4}$ 7 V bias points, which has the highest I_D. Most bias conditions, including the high V_{GD} pinch off condition (V_{GS,q} $\frac{1}{4}$ -1 V and V_{DS,q} $\frac{1}{4}$ 7 V), I_{D,pulse} are higher than the DC value, and the reduced pulse width increases the current, indicating effective passivation of the traps in the gate-drain access region that caused current collapse before passivation. The pulsed drain current increases continuously compared to DC at lower pulse widths due to the reduced self-heating effect in addition to the traps that cause current increase seen at lower drain biases. Only when both drain and gate quiescent bias conditions are set to high (V_{GS,q} $\frac{1}{4}$ 1 V and V_{DS,q} $\frac{1}{4}$ 7 V), a small current collapse is seen. This is attributed to the heating effect rather than any trapping effect as the traps are likely filled in the on-state. This is verified by using lower V_{DS,q} $\frac{1}{4}$ 5 V, which resulted in smaller dispersion than V_{DS,q} $\frac{1}{4}$ 7 V. Double pulsed I_{DS}-V_{GS} transfer curves (see the [supplementary material](#)) after passivation do not show any change in the threshold voltage ruling out traps under the gate,^{14,19,28} although further studies are necessary to completely rule this out.

Temperature dependent RF measurements were carried out on un-passivated and passivated HFETs using an ENA 5071C vector network analyzer (VNA) from 100 MHz to 19 GHz with CPW probes. The VNA was calibrated using an alumina standard substrate at each temperature. An on-wafer open structure was measured at each temperature and used to de-embed the parasitic capacitance from contact pads.³⁶ Figures 5(a) and 5(b) show f_T and f_{MAX} at two different temperatures before passivation. The lower gate length (L_G $\frac{1}{4}$ 160 nm) device has a higher f_T [Fig. 5(a)], while the longer gate length (L_G $\frac{1}{4}$ 200 nm) device gave higher f_{MAX} [Fig. 5(b)] due to lower gate resistance. The pre-passivation RF measurements were limited to V_{DS} $\frac{1}{4}$ 5 V to protect the devices. Figure 5(c) shows the temperature dependent f_T, and it does not degrade significantly with increasing temperatures. A peak f_T of 13 GHz is measured at 250 °C. Figure 5(d) shows

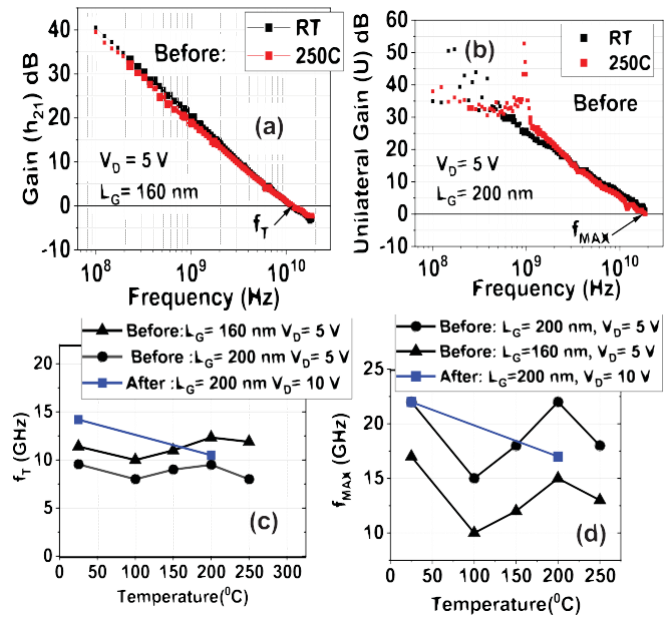


FIG. 5. (a) Measured small signal gain (h_{21}) at room temperature and 250 °C before passivation, (b) unilateral gain plot showing f_{MAX} at two different temperature before passivation, (c) comparison of f_T before and after passivation for two devices at different bias points, and (d) measured f_{MAX} for two devices before and after passivation.

the temperature dependent f_{MAX} , and a peak value of 22 GHz is measured at 200 °C. Figures 5(c) and 5(d) also show the f_T and f_{MAX} of a 200 nm gate length device (160 nm L_G device was destroyed in the passivation and RIE process) after passivation (see the [supplementary material](#) for detailed plots), and the values and trend are similar to before passivation, thus showing the suitability of the Si₃N₄ passivation.

In conclusion, a study of the temperature dependent pulsed IV characterization of b-(Al_xGa_{1-x})₂O₃/Ga₂O₃ HFETs was carried out. The DC-RF dispersion or current collapse in the gate lag measurements were lower than recessed channel MOSFETs due to the absence of any RIE damage to the channel. A moderate current collapse was observed before passivation. PECVD deposited Si₃N₄ passivation eliminated current collapse in the AlGaO/GaO HFETs. Pulsed measurements of the passivated devices show a 50% enhancement in the drain current at high drain biases due to reduced self-heating. Dispersion free operation was maintained even at higher temperatures. However, the 350 °C Si₃N₄ deposition changed the DC characteristics including the threshold voltage on currents and contact linearity. Additionally, different types of traps are introduced, which increase pulsed currents. Further optimization of the Si₃N₄ deposition process is needed for reliable passivation that does not impact the DC parameters. High frequency characterization up to 250 °C has been demonstrated for b-Ga₂O₃ HFETs. Negligible degradation of f_T and f_{MAX} at high temperatures is seen for both unpassivated and passivated devices. These results show viability of Ga₂O₃ devices for high temperature RF applications.

See the [supplementary material](#) for details on the I_D-V_G transfer curve before and after passivation, high temperature pulsed IV and RF

measurement after passivation plots, and peak g_m as a function of pulse width analysis.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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