Effect of annealing on interdigitated back contact silicon heterojunction solar cells(IBC)

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***Abstract*—Annealing effects have been studied on test structures and TLM pads to determine the optimum final annealing time for fabricated interdigitated back contact (IBC) solar cells. Initial results show that passivation will recover after 3 min annealing at 200 °C but will degrade by further annealing. Contact resistance measurement performed on TLM structures both for emitter and base stack show that by increasing the annealing time the contact resistance will increase. Using the initial annealing time of 5 min, we obtain a short circuit current density of 37 mA/cm^2 and open-circuit voltage of 691 mV, leading to a conversion efficiency of 19.3%.**

Keywords—annealing, passivation, resistance, interdigitated back contact solar cell.

I. INTRODUCTION

Amorphous silicon layers suffer from a very low lateral conductivity [1]. This, in the fabrication process of interdigitated back contact solar (IBC) cells as well as silicon heterojunction (SHJ) cells, an Indium Tin Oxide (ITO) layer is applied to the emitter and base contact area to increase the photogenerated current collection and to improve the charge transport to the metal contacts [1]. The ITO sputtering causes damage to the i-a-Si(H) layer by degrading the lifetime and open circuit voltage. This is due to dangling bonds created by ion bombardment and plasma luminescence [2]. A final temperature treatment is applied to reverse the sputtering damage at the a-Si:H/C-Si interface [3]. Elevated temperature during ITO deposition can recover some of the degradation resulting from sputtering. However, there is a temperature threshold above which degradation of the passivation is observed, which is attributed to hydrogen effusion [4]. Hydrogen saturates the dangling bonds at the a-Si:H/C-Si interface and hydrogen atoms can effuse at temperatures higher than 200°C, causing passivation to degrade [5]. Therefore, most of the conventional SHJ annealing is performed below 250°C [6].

The temperature treatment will also change the properties of ITO and the presence of underlying i-a-Si layer will increase the conductivity of the ITO layer [6]. The phenomenon of increasing n_e could be attributed to hydrogen effusion from underlying a-Si:H, which dopes the ITO and will increase the parasitic absorption [6].

It has been reported that annealing of SHJ solar cell will increase the carrier concentration in the ITO that mainly impacts the short circuit current and fill factor because of change in ITO front sheet resistance [7]. With annealing, the series resistance at the maximum power point first decreases due to a reduction in $R_{ITO\ sheet}$ but increases again with prolonged annealing [7]. Therefore, depending on the thermal budget required, the properties of the ITO must be changed. In this work, the impact of temperature treatments on interdigitated back contact solar cells (IBC) characterization results shall be examined experimentally.

II. EXPERIMENTAL DETAILS

Interdigitated Back Contact solar cell samples were fabricated on n-type CZ wafers, with a starting thickness of 185 μm and bulk resistivity of 1–10 Ω-cm. The front side of each sample was textured using alkaline wet etching (KOH and GP Solar additive), followed by an acidic cleaning process which is described in detail elsewhere [8]. The substrate surface was pretreated by HF prior to plasma-enhanced chemical vapor deposition. The front-side was then coated with a-Si:H(i) for passivation followed by an ARC of SiN. On the rear-side a-Si:H(i)/a-Si:H(n) layers were deposited consecutively. The intrinsic a-Si:H was treated with an in-situ hydrogen plasma to improve the chemical passivation. Rear-side a-Si:H(i)/a-Si:H(n) layers were partially etched by KOH etch using a conventional photolithographic technology. Then, after the cleaning and pretreatment, a-Si:H(i)/ a-Si:H(p) layers were deposited in the same way on all over the rear surface, and these a-Si:H(i)/a-Si:H(p) layers were partially removed by KOH, avoiding damage to a-Si:H(i)/ a-Si:H(n) layers. In this step, only the a-Si:H(i)/a-Si:H(p) layers should be removed, and the a-Si:H(i)/a-Si:H(n) layer protected by a SiN hard mask. Finally, electrodes were deposited on the rear side and patterned into an interdigitated layout using photolithography. The doped a-Si:H layers deposition parameters (susceptor temperature and gas flows) were kept constant across the entire study. Specifically, the susceptor temperature used for a-Si:H(n) and a-Si:H(p) layer was 250°C and 275°C respectively.

After initial deposition and repassivation of the emitter region, effective minority carrier lifetime and implied voltage were measured using a Sinton photoconductance-decay lifetime tester (WCT-120). Indium tin oxide (ITO) was deposited on the interdigitated pattern using a DC sputtering technique. A silver layer, also acting as a reflective mirror, was thermally evaporated on the rear side. Contacts were formed by another photolithography step followed by wet etching to form the final grid.

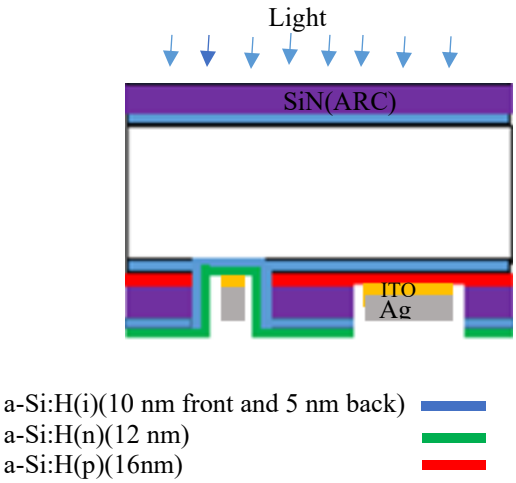


Fig. 1. Schematic of IBC-SHJ solar cell structure. Front side is random pyramid textured which is not shown in the figure. For better presentation the figure is not to scale.

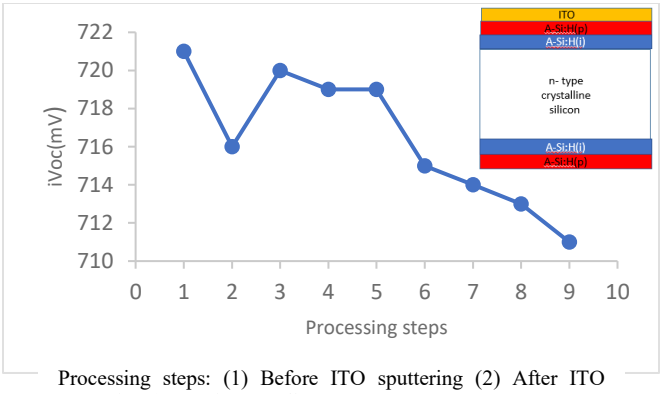
The IBC cell in this study was annealed for 5 min at 200°C in a vacuum environment with hydrogen purging to recover lifetime after metal grid deposition. The resulting cell architecture is represented in Fig. 1. A Sinton FCT-450 flash tester was used to measure the current-voltage and Suns-V_{oc} curves of each cell.

III. Results and Discussion

A. Annealing effect on passivation quality

We investigated the annealing effect on the passivation for the purpose of finding an ideal annealing time for the IBC structure. Test structures were created by depositing 5 nm of a-Si:H(i) followed by 16 nm of a-Si:H(p) on both sides of an n-type crystalline silicon and 150 nm of ITO sputtered on one side to form a stack like the IBC cell's emitter structure. Annealing was performed at 200°C in a vacuum environment with constant hydrogen purging. After deposition, the implied Voc degraded from 721 mV to 715mV and after 3 min of annealing it recovered to almost 90 % of original value. Fig 2. shows the measured implied Voc for further annealing steps up to 60 min of total annealing time.

By increasing the annealing time, the implied Voc will degrade to a lower value which is caused by hydrogen effusion from the amorphous layer.



Processing steps: (1) Before ITO sputtering (2) After ITO sputtering (3) 3 min annealing at 200 C (4) 5 min annealing (5) 7 min annealing (6) 10 min annealing (7) 15 min annealing (8) 20 min annealing (9) 30 min annealing

Fig. 2. Iimplied Voc change of the test structure shown in the inset figure at different annealing steps

B. Annealing effect on contact resitance

We fabricated TLM structures to measure contact resistivity and investigate the effect of annealing specifically on contact resistance. The TLM structures were made by depositing a-Si:H(i) and a-Si:H(p) on a p-type wafer for the emitter test structure and a full-area a-Si:H(i), followed by a-Si:H(n) layer on a n-type wafer for base test structure. ITO was sputtered through a shadow mask and silver was thermally evaporated using the same mask to create TLM pads with varying spacings of 0.3 to 4 mm.

Emitter TLM structures are shown as an example in Fig.4.

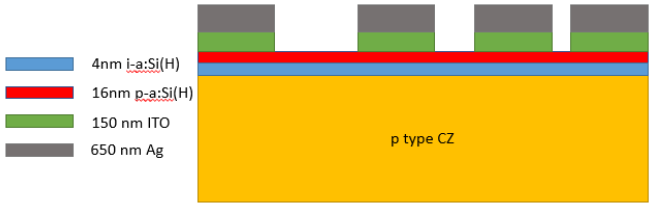


Fig. 3. TLM structure of the emitter stack.

The width of the pads was 2 mm and their length was 12 mm. Before annealing the TLM plots were not linear and showed diode characteristics. TLM structures were annealed at different intervals to make an ohmic contact between ITO and the amorphous layers. Each of the emitter and base structures were separately annealed starting from 5 min. Further annealing steps of 10, 30 and 60 min were performed on the similar test structures. For each annealing step, TLM measurements performed with a current-voltage sweep across each set of contacts using four probes.

Fig.4 shows the results of contact resistance measurement both for the emitter and base stack layers.

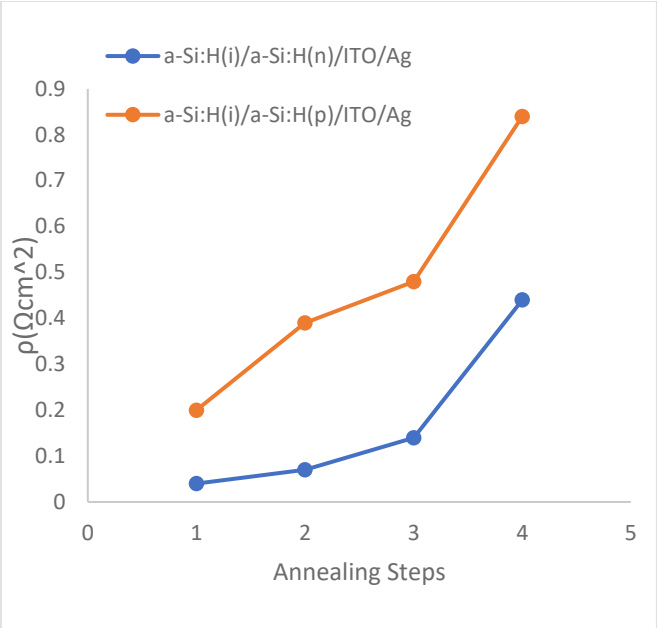


Fig.4. ITO Annealing effect on contact resistance. All annealing steps are at 200 C:
(1) 5 min annealing, (2)10 min annealing, (3)30 min annealing, (4)60 min annealing

As shown in Fig. 4, by increasing the annealing time, contact resistance both for emitter and base TLM structures will increase. The exact determination of what is causing the increase is challenging. A change in work function of the ITO could play a role [10], a reduction of the conductivity of the doped layer, possibly due to annealing [11], or a combination of both could be the cause, as both are linked [12].

C. Interdigitated Back-Contacted Silicon Heterojunction Solar Cell Results

The 1-sun I–V characteristic of our best 4-cm^2 IBC-SHJ solar cell is shown in Fig. 5 It shows a conversion efficiency of 19.3%, a Voc of 691 mV, and a Jsc of 37 mA/cm^2. FF reaches a moderate value of 71.7%. For this device, the series resistance is 1.3 Ω·cm2 and there is a high shunt resistance owning to an excellent device architecture.
The I-V characterization results shows the open circuit voltage as 691 mV which is lower compared to 736 mV that is reported using a similar fabrication process [9].

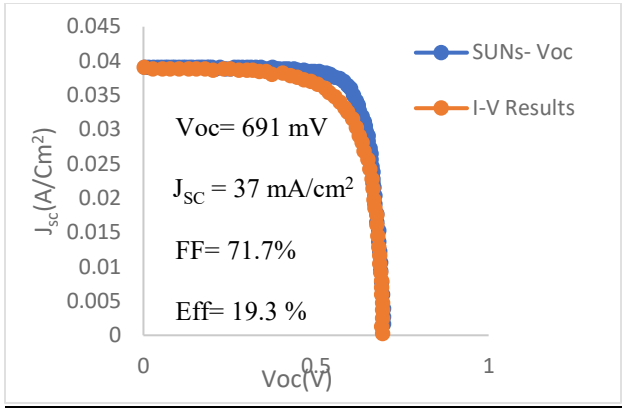
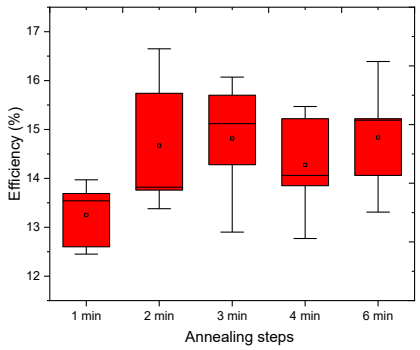
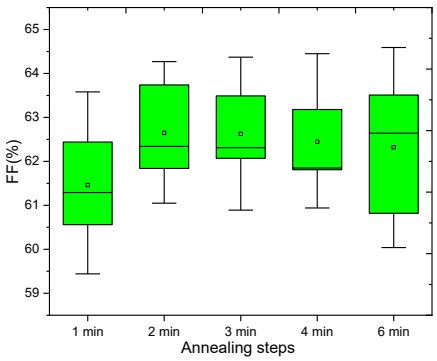


Fig. 5. I–V characteristic and Suns-Voc measurement of the best 4-cm^2 IBC-SHJ device

Another set of IBC cells including 5 cells was fabricated to test the effect of annealing on the degradation of the efficiency and other results. Fiq.6 shows the characterization results of the cells going through annealing at 200 C from 1 min to 6 min. The Box plots show that efficiency increased from %13 to above %16 by annealing around 3 min and after that the results is constant.
The future plan is to increase the annealing time to see what the results of extended annealing is.





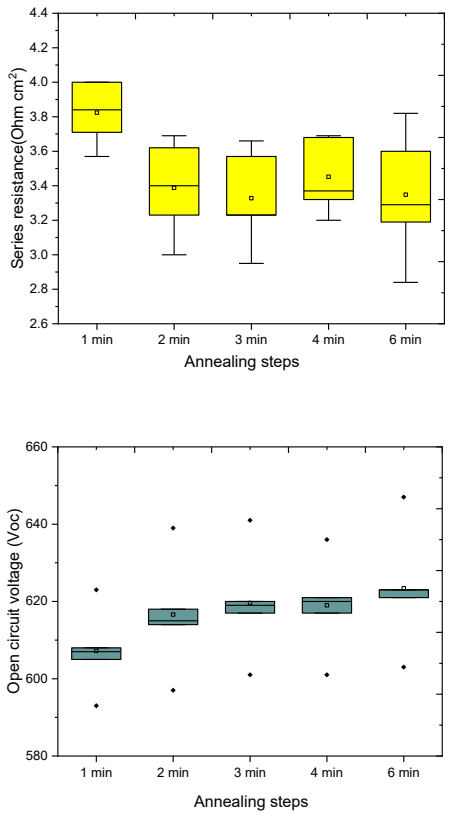


Fig. 6. I–V characteristic of the 4-cm^2 IBC-SHJ annealed at 200 C for different times started from 1 min and extended to 6 min.

CONCLUSION

This study aims to characterize the effect of annealing on the current-voltage characterization results of fabricated interdigitated back contact solar cells. Experiments performed on test structures show that by increasing the annealing time to more than 3 min, the passivation degrades and implied Voc decreases. Optimum annealing of the final structure is also important to achieve a low series resistance. Initial transfer length results show that the optimum annealing time to obtain the lowest contact resistance in emitter and base structures is 5 min. By using an initial annealing set to 5 min we obtain short a circuit current density of 37 mA/cm2 and open-circuit voltage of 691 mV, leading to a conversion efficiency of 19.3%. Final annealing step affects carrier transport through both hetero-contact layer stacks, as well as passivation. Also, optimum annealing is important to achieve a low series resistance and improve fill factor values and device performance. The effect of annealing on the current-voltage characteristic measurement is done on the IBC cells from 1 min to 6 min. The annealing effect on the IBC cells was not consistent with the test samples as there should be extended to above 6 min.

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