High-Frequency Tellurene MOSFETs with Biased Contacts

Kuanchen Xiong[#], Gang Qiu[$], Yixiu Wang[$], Lei Li[#], Alexander Göritz[*], Marco Lisker[*], Matthias Wietstruck[*], Mehmet Kaynak[*], Wenzhuo Wu[$], Peide D. Ye[$], Asher Madjar[^], and James C. M. Hwang[#1]

[#]Department of Electrical and Computer Engineering, Cornell University, USA
[$]Department of Electrical and Computer Engineering, Purdue University, USA
[*]IHP – Leibniz-Institut fur innovative Mikroelektronik, Germany
[^]Department of Electrical and Computer Engineering, Lehigh University, USA
[1]jch263@cornell.edu

***Abstract*—Microwave performance of MOSFETs with a tellurene channel is reported for the first time. The measured forward current-gain cutoff frequency and the maximum frequency of oscillation are 1.4 GHz and 3.6 GHz, respectively. Overcoming the challenge for contacting 2D materials, source contact bias is shown to increase the drain current three times and the peak transconductance four times. Additionally, tellurene being stable in air, the MOSFETs are stable for months even without surface passivation. This suggests that tellurene is a viable candidate channel material for thin-film transistors capable of operation at microwave frequencies.**

***Keywords*—cutoff frequency, microwave transistors, nanofabrication, nanotechnology, thin-film transistors**

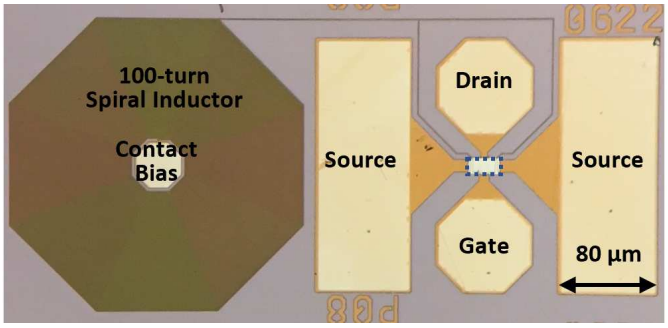
I. Introduction

Two-dimensional (2D) atomic layered materials such as graphene, MoS_2, and black phosphorus are promising channel materials for future-generation thin-film transistors [1]. Meanwhile, with increasing demands on low-cost wireless devices such as wearable monitors and internet of things, it is necessary to speed up thin-film transistors to the microwave range. However, to date most 2D MOSFET suffer from contact and stability issues. In this study, the contact has been improved by adding a contact bias [2] and the stability has been improved by using a new 2D material called tellurene, which is atomic layered tellurium. Tellurene has a sizable bandgap, high mobility, and air stability, and can be dispensed over a large area from a solution with a low thermal budget [3]. The resulted MOSFETs have a hole mobility of 700 $cm^2/V{\cdot}s$ and an on/off current ratio of 10^6. Large-scale fabrication and device-to-material correlation have also been demonstrated on tellurene [4]. This paper reports the microwave performance of tellurene MOSFETs for the first time.

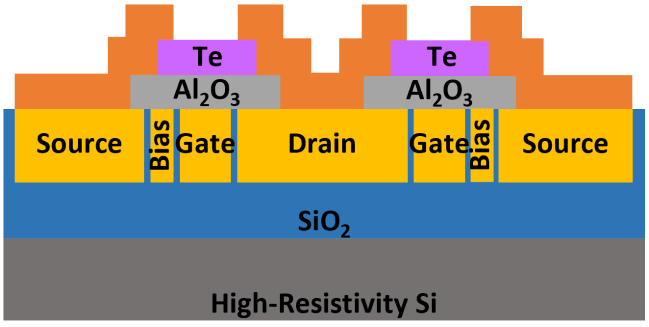
II. Fabrication

The CMOS-compatible large-scale fabrication process of tellurene MOSFETs involves four major steps: A) formation of Al buried gate and contact bias electrode, B) deposition of Al_2O_3 gate oxide, C) solution deposition of tellurene, and D) definition of active and contact regions. For design of experiments, although step A is performed on a 200-mm high-resistivity (10 kΩ·cm) Si wafer, it is subsequently diced into approximately 120 1 cm × 1 cm chips before step B. Following a gate-first sequence [5], in step B high-quality gate oxide is deposited at 300 °C without damaging tellurene.

Step A is performed at the IHP foundry using the back-end-of-line process of the SG13 technology. After wafer dicing, each 1 cm × 1 cm chip contains the footprints for approximately a thousand individually probable RF MOSFET [Fig. 1(a)]. Each MOSFET has two 10-μm-wide gate fingers for a total gate width W_G = 20 μm, which spans across a 10 μm × 20 μm active region. The gate length L_G = 0.8 μm unless otherwise noted. The gate thickness is approximately 0.5 μm. The source and drain are equally spaced from the gate so that $L_{SG} = L_{GD}$ = 0.4 μm. The last 5 μm of the source contact closest to the gate overlaps a contact bias electrode [6] [Fig. 1(b)]. The contact



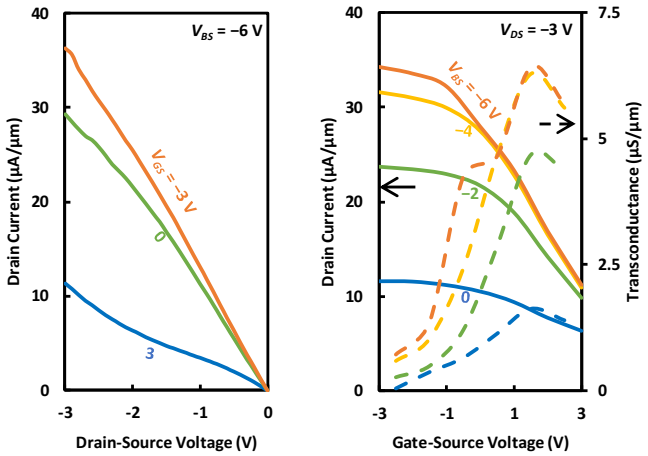
(a)



(b)

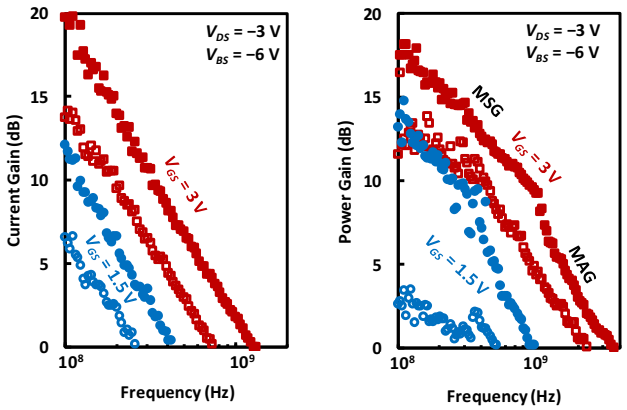
Fig. 1. (a) Top-view micrograph and (b) cross-section schematic of a tellurene MOSFET with two gate fingers. In (a), the active region of tellurene is highlighted in a dashed rectangle, and a thin metal line connects the contact bias to its probe pad through a spiral inductor.

2021 IEEE/MTT-S International Microwave Symposium - IMS 2021 | 978-1-6654-0307-8/21/$31.00 ©2021 IEEE | DOI: 10.1109/IMS19712.2021.9574853



(a) (b)

Fig. 2. Measured (a) output and (b) transfer characteristics of a tellurene MOSFET.



(a) (b)

Fig. 3. As-measured (empty symbols) and de-embedded (solid symbols) small-signal (a) current and (b) power gains of the tellurene MOSFET.

bias electrode is isolated from both the channel and source contact and is connected to its own probe pad through a spiral inductor to prevent RF leakage. Under normal MOSFET operation, the drain contact is forward biased by the drain bias, so no extra bias electrode is necessary there.

In step B, 30-nm-thick Al_2O_3 is deposited by ALD, then patterned by photolithography and 6:1 buffered oxide etch to expose the probe pads for not only the contact bias, but also the gate, source, and drain. Al_2O_3 is patterned before tellurene deposition to keep the tellurene surface pristine for top contacts. Wet etch is used because dry etch leaves a photoresist residue that is difficult to remove.

In step C, tellurene flakes are grown below 200 °C through the reduction of Na_2TeO_3 by N_2H_4 in an alkaline solution with the crystal surface protected by polyvinylpyrrolidone (PVP) ligand at a Na_2TeO_3/PVP mole ratio of 52.4 [3]. Following growth, tellurene is thinned down to approximately 10 nm in acetone for 4 h, then coated onto step-B chips by the Langmuir-Blodgett process.

In step D, tellurene active regions are patterned by photolithography and etched in an Oxford Instruments PlasmaLab 80+ plasma reactor for 30 s with 100-sccm CF_4 and 20-sccm O_2 under 200-W RF power. The 30-s etch time is divided into six 5-s periods interrupted by 10-s rest time to avoid photoresist charring. The active region has a high probability to be single crystalline, because its size is much smaller than the 100-μm grain size of tellurene [3].

After tellurene etch, the photoresist is stripped in acetone for 30 min. It can be seen in Fig. 1(a) that tellurene is free of photoresist residue. Ni and Au contact layers, 50-nm-thick and 100-nm-thick, respectively, are evaporated by an electron gun.

After the tellurene MOSFETs are fabricated, they are characterized in a Cascade Microtech Summit 1000 thermal probe station under ambient conditions. DC characterization is performed by using an Agilent Technologies 4156C precision semiconductor parameter analyzer. RF characterization is performed by using an Agilent N5230A PNA network analyzer.

III. Result and Discussion

A. DC Performance

Fig. 2 shows the output and transfer characteristics measured on a representative tellurene MOSFET. It can be seen that the MOSFET exhibits *p*-type conduction typical of solution-grown tellurene. The high work function of Ni reduces the contact resistance, which is further reduced by the contact bias V_{BS}. The leakage currents through the gate and the contact bias electrode, I_G and I_B, are negligible at 10^{-4} μA/μm and 10^{-8} μA/μm, respectively. The contact bias increases not only the drain current, but also the transconductance. For example, by decreasing V_{BS} from 0 to −6 V, the drain current increases three times while the peak transconductances increases four times. Overall, the device behaves like a long-channel MOSFET despite the sub-micrometer gate length.

B. RF Performance

With V_{DS} = −3 V and V_{BS} = −6 V, Fig. 3 shows the small-signal current and power gains measured on the tellurene MOSFET. It can be seen that although the DC transconductance peaks at a gate-source voltage V_{GS} = 1.5 V, the gains increase significantly by increasing V_{GS} further to 3 V. The gains increase further after de-embedding the parasitic capacitance of the probe pad, which is much larger than the active region as shown in Fig. 1(a). For example, with V_{GS} = 3 V, the as-measured forward-current cutoff frequency f_T = 0.76 GHz, but the de-embedded f'_T = 1.4 GHz. Similarly, the as-measured maximum frequency of oscillation f_{MAX} = 2.4 GHz, but the de-embedded f'_{MAX} = 3.6 GHz. These results are much better than solution-grown MoS_2 MOSFETs [7] and comparable to early-stage black phosphorus MOSFETs [8]. However, the tellurene MOSFETs are more stable and can be stored in dry air for at least three months even without surface passivation.

C. Small-Signal Model

Fig. 4 illustrates the small-signal model extracted from the measured small-signal data. The model includes parasitic capacitances associated with the probe pads C_{PG} = C_{PD} = 12 fF

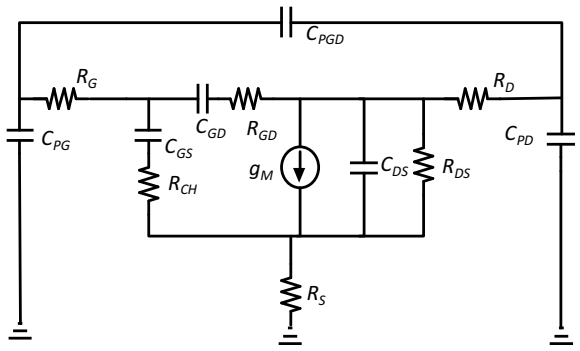


Fig. 4. Small-signal model of the tellurene MOSFET.

Table 1. Small-signal parameters of intrinsic tellurene MOSFET: L_G = 0.8μm, W_G = 20 μm, V_{DS} = −3 V, V_{GS} = 3 V, V_{BS} = −6 V

Symbol	Description	Unit	Value
R_S	Source Resistance	kΩ·μm	5.0
R_G	Gate Resistance	kΩ·μm	0.2
R_D	Drain Resistance	kΩ·μm	5.0
R_{GD}	Gate-Drain Resistance	kΩ·μm	20
R_{DS}	Drain-Source Resistance	kΩ·μm	290
R_{CH}	Channel Resistance	kΩ·μm	5.6
C_{GS}	Gate-Source Capacitance	fF/μm	0.94
C_{GD}	Gate-Drain Capacitance	fF/μm	0.37
C_{DS}	Drain-Source Capacitance	fF/μm	0.13
g_M	Transconductance	μS/μm	34

and C_{PGD} = 2 fF, which are extracted from an OPEN test structure with probe pads only. Similar to [9], Table 1 lists the intrinsic model parameters extracted with V_{DS} = −3 V, V_{GS} = 3 V, and V_{BS} = −6 V. Notice that, despite contact bias, the source resistance is still an order of magnitude higher than that of a 2D $PtSe_2$ MOSFETs [10]. This is mainly due to the series resistance of the 0.4-μm-long access region between the gate and the source, which is not biased. Shortening the access region or extending the contact bias below it will decrease the source resistance but increase the source-gate capacitance. Therefore, more careful tradeoff is needed to further optimize the microwave performance of the tellurene MOSFETs.

D. Gate Length Dependence

To investigate the effect of gate length, other tellurene MOSFETs are similarly fabricated with L_G = 0.4, 1.6, or 4 μm with small-signal characteristics measured and extracted as illustrated in Fig. 5. As C_{GS} and C_{GD} decreases with decreasing L_G, f'_T and f'_{MAX} increase generally [11]:

$$C_{OX} = \epsilon_S / t_{OX}, \tag{1}$$

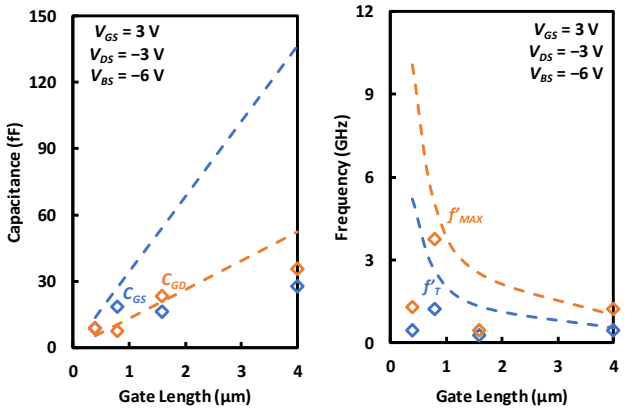
$$\alpha = 1 - V_{CH}/V_{DS,SAT}, \tag{2}$$

$$C_{GS} = 2W_G L_G C_{ox}(1 + 4\alpha + \alpha^2)/3(1+\alpha)^2, \tag{3}$$

$$C_{GD} = 2W_G L_G C_{ox}(2\alpha + \alpha^2)/3(1+\alpha)^2, \tag{4}$$

$$f''_T = g_M/2\pi(C_{GS} + C_{GD}), \tag{5}$$

$$f'_T = g_M/2\pi\{C_{GS} + C_{GD}[1 + g_M(R_S + R_D)]\}, \tag{6}$$



(a) (b)

Fig. 5. Measured (symbols) vs. modeled (curves) gate-length dependence of (a) gate-drain and gate-source capacitances C_{GS} and C_{GD} and (b) intrinsic cutoff frequencies f'_T and f'_{MAX} of the tellurene MOSFET.

$$f'_{MAX} = f'_T/2\sqrt{(2\pi f''_T C_{GD} + 1/R_{DS})(R_G + R_S)}. \tag{7}$$

where ϵ_s is the permittivity and t_{OX} is the thickness of the gate oxide, and $V_{CH} = V_{DS}/3 = -1$ V, V_T = 5 V, and $V_{DS,SAT} = V_{GS} - V_T = -2$ V. The calculated values of C_{GS}, C_{GD}, f'_T, and f'_{MAX} are included in Fig. 5 as dashed curves. It can be seen that they agree with the measured data qualitatively, but tend to overestimate quantitatively. This is probably because other parameters such as R_G and g_M also depend on L_G. Additionally, the relatively long access region helps reduce C_{GS} as mentioned earlier. This shows that, to improve f'_T, and f'_{MAX}, many parameters other than L_G need to be optimally scaled.

The cutoff frequencies decrease unexpectedly at L_G = 0.4 μm, mainly because L_{SG} and L_{GD} fail to scale with L_G and remains at 0.4 μm. With $L_G < L_{SG} + L_{GD}$, $R_{CH} < R_S + R_D$ and most of V_{DS} drops across the access region rather than being applied to the channel under L_G to increase I_D and g_M. This is similar to quasi-saturation in a bipolar transistor [11] and prevents the drain current from actual saturation as shown in Fig. 2(a).

IV. Conclusion

This study is the first report on the RF performance of tellurene MOSFETs. Gigahertz operation is achieved with a low-cost solution-based and CMOS-compatible process. Contact bias helps reduce the contact resistance and the gate-source capacitance, enabling microwave operation. However, it needs to be better scaled for sub-micrometer gate length MOSFETs.

Acknowledgment

This work was supported in part by NSF/AFOSR under Grant No. 1433459-EFMA. The synthesis of tellurene was sponsored by the National Science Foundation under Grant No. CMMI-1762698. The device processing was performed at the Cornell NanoScale Facility, an NNCI member supported by NSF Grant NNCI-2025233.

REFERENCES

[1] Z. Lin *et al.,* "2D materials advances: from large scale synthesis and controlled heterostructures to improved characterization techniques, defects and applications," *2D Mater.*, vol. 3, no. 4, p. 042001, Dec. 2016.

[2] K. Xiong *et al.*, "Large-scale fabrication of submicron-gate-length MOSFETs with a trilayer $PtSe_2$ channel grown by molecular beam epitaxy," *IEEE Trans. Electron Devices*, vol. 67, no. 3, pp. 796–801, Mar. 2020.

[3] Y. Wang *et al.,* "Field-effect transistors made from solution-grown two-dimensional tellurene," *Nat. Electron.*, vol. 1, pp. 228–236, 2018.

[4] K. Xiong *et al.*, "Wafer-scale material-device correlation of tellurene MOSFETs," in *IEEE MTT-S Int. Microw. Workshop Ser. Adv. Mater. Processes (IMWS-AMP) Dig.*, Ann Arbor, MI, USA, Jul. 2018, pp. 1–3.

[5] W. Wei *et al.,* "Graphene FETs with aluminum bottom-gate electrodes and its natural oxide as dielectrics," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2769–2773, Sep. 2015.

[6] C. Li *et al.,* "Black phosphorus high-frequency transistors with local contact bias," *ACS Nano*, vol. 14, no. 2, pp. 2118−2125, Jan. 2020.

[7] K. Xiong *et al.,* "Large-scale fabrication of RF MOSFETs on liquid-exfoliated MoS_2," in *Eur. Microw. Conf. (EuMC)*, Madrid, Spain, Sep. 2018, pp. 1−4.

[8] X. Luo, Y. Rahbarihagh, J. C. M. Hwang, H. Liu, Y. Du, and P. D. Ye, "Temporal and thermal stability of Al_2O_3-passivated phosphorene MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1314–1316, Dec. 2014.

[9] F. Pasadas *et al.,* "Small-signal model for 2D-material based FETs targeting radio-frequency applications: The importance of considering nonreciprocal capacitances," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4715−4723, Nov. 2017.

[10] L. Li *et al.,* "Wafer-scale fabrication of recessed-channel PtSe2 MOSFETs with low contact resistance and improve gate control," *IEEE Trans. Electron Devices,* vol. 65, no. 10, pp. 4102−4108, Oct. 2018.

[11] W. Liu, *Fundamentals of III-V Devices HBTs, MESFETs, and HFETs/HEMTs.* New York, NY, USA: Wiley, 1999.