

Ga₂O₃-on-SiC Composite Wafer for Thermal Management of Ultra-Wide Bandgap Electronics

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ABSTRACT: β -phase gallium oxide (Ga₂O₃) is an emerging ultra-wide bandgap (UWBG) semiconductor ($E_G \sim 4.8$ eV) which promises generational improvements in the performance and manufacturing cost over today's commercial wide bandgap power electronics based on GaN and SiC. However, overheating has been identified as a major bottleneck to the performance and commercialization of Ga₂O₃ device technologies. In this work, a novel Ga₂O₃/4H-SiC composite wafer with high heat transfer performance and an epi-ready surface finish has been developed using a fusion bonding method. By taking advantage of low-temperature metalorganic vapor phase epitaxy (MOVPE), a Ga₂O₃ epitaxial layer was successfully grown on the composite wafer while maintaining the structural integrity of the composite wafer without causing interface damage. An atomically smooth homoepitaxial film with a room-temperature Hall mobility of ~ 94 cm²/Vs and volume charge of $\sim 3 \times 10^{17}$ cm⁻³ was achieved at a growth temperature of 600°C. Phonon transport across the Ga₂O₃/4H-SiC interface has been studied using frequency-domain thermoreflectance (FDTR) and a differential steady-state thermoreflectance (SSTR) approach. Scanning transmission electron microscopy (STEM) analysis suggests that phonon transport across the Ga₂O₃/4H-SiC interface is dominated by the thickness of the SiN_x bonding layer and an unintentionally formed SiO_x interlayer. Extrinsic effects that impact the thermal conductivity of the 6.5 μ m thick Ga₂O₃ layer was studied via time-domain thermoreflectance (TDTR). Thermal simulation was performed to estimate the improvement of the thermal performance of a hypothetical single-finger Ga₂O₃ metal-semiconductor field-effect transistor (MESFET) fabricated on the composite substrate. This novel power transistor topology resulted in a $\sim 4.3 \times$ reduction in the junction-to-package device thermal resistance. Furthermore, an even more pronounced cooling effect is demonstrated when the composite wafer is implemented into the device design of practical multi-finger devices. These innovations in device-level thermal management give promise to the full exploitation of the promising benefits of the UWBG material, which will lead to significant improvements in the power density and efficiency of power electronics over current state-of-the-art commercial devices.

KEYWORDS: Composite substrate, fusion bonding, gallium oxide (Ga_2O_3), low temperature metal organic vapor phase epitaxy (MOVPE), thermal boundary resistance (TBR), thermal management, ultra-wide bandgap (UWBG) semiconductor devices.

INTRODUCTION

Ultra-wide bandgap (UWBG) β -phase gallium oxide (Ga_2O_3), $E_G \sim 4.8$ eV, is emerging as a replacement for today's commercially available wide bandgap (WBG) power electronics such as gallium nitride (GaN) and silicon carbide (SiC) due to its generational improvements in performance and manufacturing cost.¹ The lateral figure of merit (LFOM)² is a metric that compares the theoretically achievable power switching performance of laterally configured transistor devices. It is defined as $LFOM = V_{BR}^2/R_{ON-SP}$, where V_{BR} is the breakdown voltage and R_{ON-SP} is the specific ON-resistance. The LFOM can also be expressed as $q\mu n_s E_c^2$, where q is the electron charge, μ is the channel mobility, n_s is the sheet charge density, and E_c is the critical electric field². Since E_c scales as the 2-2.5 power of the bandgap energy (E_G), the LFOM offered by Ga_2O_3 is the highest among the technologically relevant semiconductors shown in **Table 1**. While diamond ($E_G \sim 5.5$ eV) could potentially offer a higher LFOM, key challenges associated with large area substrate availability and substitutional doping have remained unsolved over the last few decades. In contrast, high crystalline quality and potentially low cost Ga_2O_3 substrates can be manufactured using diverse melt-growth techniques (similar to the case of Si)¹, and shallow n-type doping schemes are readily available. The high LFOM offered by Ga_2O_3 gives promise to the development of lateral power switches with kV-class breakdown voltages and minimized device footprints. The enhanced power switching performance at the device-level will eventually translate into commensurate improvement in the system-level size, weight, and power (SWaP) and efficiency.

Table 1. Material properties and the LFOM for conventional, WBG, and UWBG semiconductors.³⁻⁶

Material	Conventional		WBG		UWBG
Property	Si	GaAs	SiC	GaN	$\beta\text{-Ga}_2\text{O}_3$
Bandgap, E_G (eV)	1.12	1.43	3.26	3.42	4.8
Relative dielectric constant, ϵ	11.9	13.1	10.1	9.7	10
Breakdown field, E_c (MV/cm)	0.3	0.4	3	3.3	8
Electron (channel) mobility, μ (cm ² /V·s)	1400	8500	1020	1350(2000)	180(420)
Saturated electron velocity, v_s (cm/s)	1×10^7	2×10^7	2×10^7	2.7×10^7	1.5×10^7
Thermal conductivity, k (W/m·K)	150	46	490	130	11-27
Normalized LFOM ($q\mu n_s E_c^2$)	1	10.8	72.9	172.9	213.3

The targeted higher power handling capability (e.g., 10 W/mm) and reduced device footprint of Ga_2O_3 electronics (both enabled by the superior LFOM), translate into extremely high operational heat fluxes (>1 MW/cm²). Moreover, the thermal conductivity of Ga_2O_3 (10.9-27 W/m·K)⁵ is the lowest among the semiconductors listed in **Table 1**. Therefore, overheating has become a major bottleneck to the commercialization of Ga_2O_3 electronics. In fact, no reported Ga_2O_3 device has achieved the performance projected by the superior LFOM, and a thermally limited technological plateau has been reached.

Chatterjee et al.⁷ demonstrated that the channel temperature of a homoepitaxial Ga_2O_3 metal-oxide-semiconductor field-effect transistor (MOSFET) would exceed 1500°C at a targeted power density of 10 W/mm. This work highlights that a composite wafer^{8,9} which consists of a Ga_2O_3 layer (thinner than 10 μm) integrated with a high thermal conductivity substrate (e.g., SiC, AlN, diamond) using an integration process that results in a reasonable interfacial thermal boundary resistance (<60 m²·K/GW) would reduce the device junction-to-package thermal resistance to a manageable level, which is comparable to that for commercial GaN-on-Si high electron mobility transistors (HEMTs)¹⁰. The importance of these thermal design parameters has also been suggested in a study aiming for Ga_2O_3 /polycrystalline-SiC vertical device development.⁸ In addition, an ideal and practical composite substrate should allow subsequent growth/fabrication of Ga_2O_3 lateral devices. Such composite wafers require an epi-ready surface morphology, low wafer bow, and a process that is scalable to large-diameter wafers. Another critical challenge is managing the strain induced by the difference in thermal expansion coefficients between the two materials attached with each other. The interface between the Ga_2O_3 and the heat-sinking substrate needs to be stress-engineered so that the materials stay attached from room temperature up to subsequent high temperature device processing steps. A previous study has demonstrated direct growth of Ga_2O_3 on SiC via molecular beam epitaxy (MBE).¹¹ In this work, a composite wafer has been constructed using a wafer bonding approach to better fulfill the aforementioned requirements.

In this work, a novel Ga_2O_3 /4H-SiC composite wafer with high heat transfer performance has been developed using a fusion bonding approach.¹² The thermal conductivity of the Ga_2O_3 layer and the effective thermal boundary resistance (TBR)

at the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ interface were characterized through the combined use of time-domain thermoreflectance (TDTR), frequency-domain thermoreflectance (FDTR), and a differential steady-state thermoreflectance (SSTR) technique. The measured thin film thermal conductivity was compared with a Debye-Callaway model incorporating phononic parameters derived from first-principles calculations. Individual resistive components that comprise the effective TBR at the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ interface were analyzed using an acoustic mismatch model (AMM) and diffusive mismatch model (DMM). Furthermore, scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDX) were used to investigate the interface quality and chemistry, respectively. A Si-doped Ga_2O_3 epitaxial layer was successfully grown on the composite substrate by taking advantage of a low-temperature metalorganic vapor phase epitaxy (MOVPE) process. Finally, thermal modeling of single- and multi-finger Ga_2O_3 lateral transistors was performed to evaluate the improvement of the device thermal resistance by replacing the Ga_2O_3 substrate with the composite substrate developed in this study. The outcomes of this work suggest that the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ composite substrate technology is an effective solution for the device-level thermal management of Ga_2O_3 electronics, which gives promise to exploit the full potential of the UWBG material.

FABRICATION OF A $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ COMPOSITE SUBSTRATE

A novel composite substrate to serve as a platform for subsequent epitaxial growth and device fabrication was created using a wafer integration scheme illustrated in **Figure 1 (a)**. The starting material was a (010)-oriented Fe-doped Ga_2O_3 wafer using the Czochralski method in an inductively heated iridium crucible. The wafers were produced by slicing 750- μm -thick disks from an ingot and polishing them to achieve an epi-ready finish.¹³ This orientation was selected because it is favorable over the (201) and (001) orientations due to the higher cross-plane thermal conductivity⁵ and lower coefficient of thermal expansion (CTE) mismatch with 4H-SiC.¹⁴ The surface of the 25 mm-diameter Ga_2O_3 wafer was processed to result in an average surface roughness of $\sim 1 \text{ nm}$ (RMS roughness of 2.8 nm). This surface preparation was necessary to make the wafers suitable for the subsequent low-temperature bonding process.¹⁵ The Ga_2O_3 wafer and a 50 mm-diameter 4H-SiC wafer were each coated with 15 nm of SiN_x to prepare them for fusion bonding using a standard process^{16,17} with well-characterized TBR in previous reports¹⁸.

Wet activation was performed in a diluted SC1 cleaner (ammonium hydroxide, hydrogen peroxide and deionized water) to remove organic contaminants and particles. The Ga_2O_3 and 4H-SiC wafer surfaces were then activated in oxygen plasma, joined at room temperature to initiate fusion bonding^{16,17}, and the bonded wafers were cured at 215°C in a N_2 convection oven. The interface is covalently bonded, which avoids the poor interface quality associated with previously reported $\text{Ga}_2\text{O}_3/\text{diamond}$ van der Waals interfaces.⁹ The low-temperature bonding process enables bow and warp requirements to be met for potential large-diameter wafer integration (**Figure 1 (b)**). Finally, the Ga_2O_3 was thinned down using a series of lapping plates and a diamond abrasive (9 μm , 3 μm , and 0.25 μm diamond grit size), followed by a silica-based chemical-mechanical polishing (CMP) process to remove subsurface damage and enable subsequent epitaxial growth for device processing. A Ga_2O_3 film thickness of less than 10 μm was pursued as shown in **Figure 1 (c)**, to minimize the overall thermal resistance of the composite substrate, and the final thickness of the Ga_2O_3 layer was determined to be $\sim 6.5 \mu\text{m}$. The aforementioned integration process does not involve the introduction of implantation-induced point defects into the Ga_2O_3 layer which is accompanied by a previously reported surface-activated bonding method.¹⁹ Therefore, the $\text{Ga}_2\text{O}_3/\text{SiC}$ substrate developed in this work can serve as an ideal platform for subsequent device fabrication as it allows the growth of homoepitaxial layers with the highest crystalline quality, potentially without threading dislocations.

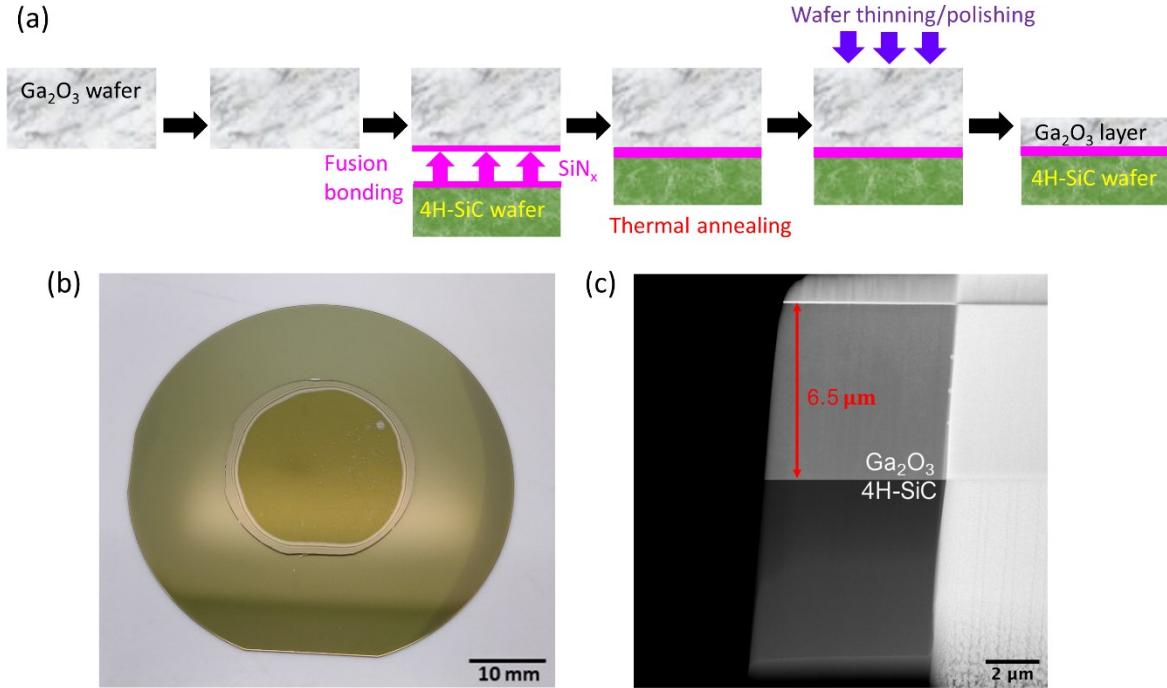


Figure 1. (a) The wafer bonding and thinning approach used to create the Ga_2O_3 composite substrate. (b) An image of Ga_2O_3 bonded onto 4H-SiC. The yield is nominally 100% except in the edge exclusion region. (c) Cross-sectional transmission electron microscopy (TEM) image of the Ga_2O_3 -on-SiC composite wafer.

It should be noted that the stress/strain induced by the CTE mismatch of the two attached materials must be managed such that the heterointerface stays intact from room temperature up to high-temperature conditions associated with the subsequent device processing steps. Although diamond possesses a higher thermal conductivity ($> 1500 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$)²⁰ than 4H-SiC, 4H-SiC was selected due to the availability of larger diameter semi-insulating substrates, high thermal conductivity (347 $\text{W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$)²¹, and lower CTE mismatch^{14,22}, that would prevent de-bonding of the Ga_2O_3 , caused by unacceptable levels of thermal strain²³ under high growth temperatures, i.e., 600-1000°C for molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD), and low-pressure chemical vapor deposition (LPCVD) growth processes.²⁴

DIFFERENTIAL STEADY-STATE THERMOREFLECTANCE

The time-domain thermoreflectance (TDTR) method²⁵ has been used to study the thermal transport across interfaces of exfoliated Ga_2O_3 membranes transferred onto single-crystal diamond⁹ and thin films integrated with SiC via surface-activated bonding.¹⁹ However, it should be noted that the Ga_2O_3 thickness of these structures was limited to 140-430 nm. TDTR offers acceptable measurement sensitivity to the heterointerface only under such thickness ranges due to the shallow probing volume. This limitation associated with the thermal penetration depth originates from the high modulation frequency of the pump laser (e.g., 2.2 MHz) and the low thermal conductivity of Ga_2O_3 .²⁶ On the other hand, frequency-domain thermoreflectance (FDTR)²⁷ can achieve a deeper thermal penetration depth at the lower modulation frequency range²⁶; however, the measurement sensitivity to the heterointerface quickly drops as the Ga_2O_3 film thickness increases. Accordingly, the TDTR and FDTR techniques are incapable of probing the “thermally-buried” Ga_2O_3 /4H-SiC heterointerface of the Ga_2O_3 composite substrate developed in this work, with a Ga_2O_3 thickness of $\sim 6.5 \mu\text{m}$.

A steady-state thermoreflectance (SSTR) method was recently developed by Braun et. al.²⁸ This technique uses a much lower pump laser modulation frequency (e.g., 150 Hz) as compared to TDTR, which establishes quasi-steady-state thermal condition during measurements. This lower modulation frequency allows the study of thermal transport processes at longer diffusion times and length scales, which enables accurate measurement of the thermal conductivity of bulk materials.²⁶ By taking advantage of the deeper thermal penetration depth of SSTR, we developed a differential SSTR process, which allows simultaneous determination of the thermal conductivity of the $\sim 6.5 \mu\text{m}$ -thick Ga_2O_3 film and the effective thermal boundary resistance (TBR) at the Ga_2O_3 /4H-SiC interface of the composite substrate. First, the thermal conductivity of the 4H-SiC

substrate is determined prior to wafer bonding (**Figure 2 (a)**). Next, the probing depth of the SSTR setup is controlled by adjusting the pump laser radius²⁶ to measure the thermal conductivity of the Ga_2O_3 thin film after the bonding/thinning process is complete (**Figure 2 (b)**). Finally, the overall thermal resistance of a probing volume that extends below the Ga_2O_3 /4H-SiC interface of the composite wafer is measured using a larger pump laser radius (**Figure 2 (c)**). By subtracting the measured thermal resistance of the 4H-SiC substrate and the Ga_2O_3 film from the total thermal resistance, the effective TBR at the Ga_2O_3 /4H-SiC interface is extracted.

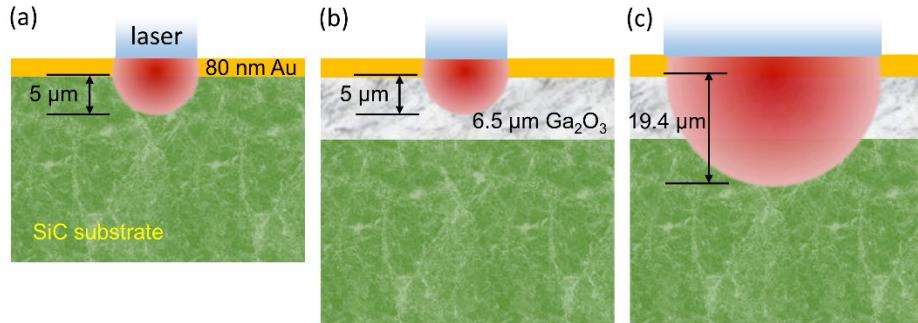


Figure 2. The differential SSTR process to measure (a) the thermal conductivity of the 4H-SiC substrate, (b) the thermal conductivity of the Ga_2O_3 layer, and (c) the effective TBR at the Ga_2O_3 /4H-SiC interface.

LOW-TEMPERATURE MOVPE GROWTH OF Ga_2O_3 EPITAXIAL LAYER

MOVPE has emerged as a very promising technique that allows the growth of high-quality β - Ga_2O_3 homoepitaxial films with room-temperature electron mobility values close to the theoretical limit ($\sim 200 \text{ cm}^2/\text{Vs}$) over a wide range of growth temperatures^{24,29-33}. Recently, we have shown that device-grade homoepitaxial films with high carrier mobility values can be grown at a lowered growth temperature of 600°C using MOVPE³⁴. To avoid potential de-bonding of the Ga_2O_3 layer of the composite substrate due to the thermal expansion mismatch that would be pronounced under high growth temperatures, we took advantage of the recently developed low-temperature MOVPE technique. A lightly Si-doped Ga_2O_3 epitaxial film was grown in an Agnitron Agilis reactor using Tri-ethylgallium, oxygen gas, and diluted silane as the precursor gases, and argon as the carrier gas. Prior to loading into the growth reactor, the sample was cleaned using Acetone, isopropyl alcohol (IPA), and DI water in a sonication bath for 2 minutes each. This was followed by a diluted HF dip for 15 minutes. The growth was performed at a temperature of 600°C, chamber pressure of 60 Torr, and a $\sim 400 \text{ nm}$ thick Ga_2O_3 epilayer was grown at a growth rate of 6.2 nm/min³³. After growth, the electronic transport properties, and the surface morphology of the MOVPE grown film were characterized using Hall-effect measurements and atomic force microscopy (AFM), respectively. Prior to growth, the composite substrate was analyzed using AFM (Bruker Dimension Icon) as shown in **Figure 3(a)**. The surface of the composite substrate was extremely smooth with an RMS roughness of $\sim 0.17 \text{ nm}$, which is similar to those for commercially available (010)-oriented Ga_2O_3 substrates, thus, showing the efficacy of the polishing technique. Extremely smooth films with atomically flat surfaces with sub-nanometer RMS roughness ($\sim 0.4 \text{ nm}$) were achieved. **Figure 3 (b) and (c)** show large area ($5 \times 5 \mu\text{m}^2$) and a corresponding small area ($0.5 \times 0.5 \mu\text{m}^2$) AFM scans of the MOVPE grown film. Smooth surface morphology could be achieved at this growth temperature due to large Ga adatom diffusion as discussed elsewhere³³. The sample did not show any signs of wear during the entire growth/processing steps including the solvent cleaning, acid cleaning, and epilayer growth.

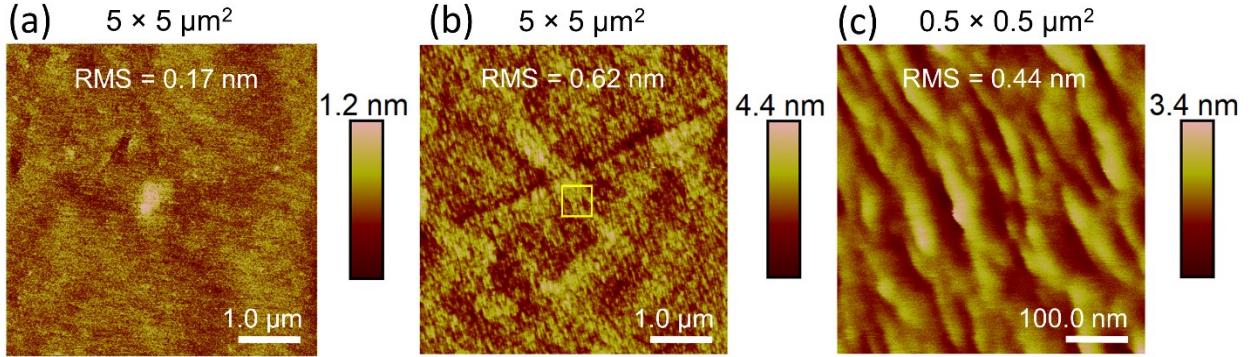


Figure 3. (a) AFM image of the polished Ga_2O_3 /4H-SiC composite substrate after solvent cleaning. (b) Surface morphology of the MOVPE grown Si-doped film for a $5 \times 5 \mu\text{m}^2$ area. (c) A $0.5 \times 0.5 \mu\text{m}^2$ AFM scan corresponding to the yellow-boxed area shown in (b).

The electronic transport properties were analyzed using room-temperature Hall measurements (Ecopia HMS 3000). Ti/Au (50 nm/100 nm) ohmic contacts were deposited using DC sputtering on the four corners using a shadow-mask to form the Van der Pauw structure. The contacts exhibited perfectly Ohmic behavior without the need for contact annealing. A room temperature Hall mobility of $94 \text{ cm}^2/\text{Vs}$ and a sheet charge of $1.2 \times 10^{13} \text{ cm}^{-2}$ were extracted corresponding to a volume charge of $\sim 3 \times 10^{17} \text{ cm}^{-3}$. This first demonstration of epilayer growth on the novel composite substrate shows the feasibility of growing smooth homoepitaxial n-type doped high-quality single crystalline epilayers using MOVPE. In other words, this demonstration highlights the compatibility of this novel composite substrate with standard solvent cleaning and acid cleaning while also proving its sturdiness at low pressures and high temperatures, that are required for epilayer growth. These initial results are extremely promising for the development of high-power Ga_2O_3 -based lateral devices with potentially superior thermal performance to that of devices on Ga_2O_3 bulk substrates.

RESULTS AND DISCUSSION

Figure 4 illustrates phonon scattering mechanisms that would govern the overall junction-to-package thermal resistance of devices grown on the Ga_2O_3 /4H-SiC composite wafer. First, when the thickness of the thinned single crystal Ga_2O_3 film becomes comparable to the mean free path of acoustic phonons, incoherent phonon-boundary scattering will reduce the thermal conductivity. Also, the wafer thinning/polishing processes may result in subsurface crystallographic imperfections causing phonon-defect scattering effects. Second, the transmission of phonons across the Ga_2O_3 /4H-SiC interface will not only be governed by the acoustic/diffusive mismatch between dissimilar materials but also the low thermal conductivity of the SiN_x bonding layer.

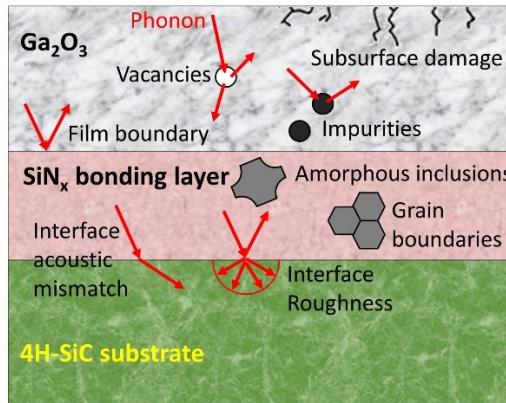


Figure 4. Phonon scattering within the Ga_2O_3 /4H-SiC composite wafer.

THERMAL CONDUCTIVITY OF THE THINNED/POLISHED Ga_2O_3

Previous studies⁷⁻⁹ suggest that a thinner Ga_2O_3 layer remaining on a composite substrate will result in a higher heat transfer performance. Therefore, in addition to measuring the thermal conductivity of the 6.5 μm -thick Ga_2O_3 layer of the composite wafer, this layer was thinned into a wedge shape and characterized. The film thickness was measured along several locations using cross-sectional scanning electron microscopy (SEM) on specimens prepared via focused ion beam (FIB) milling, as shown in **Figure 5 (a)**. The cross-plane thermal conductivity of the pre-integrated (010) substrate and the post-integrated Ga_2O_3 film were measured via time-domain thermoreflectance (TDTR)²⁵ and resulting values are shown in **Figure 5 (b)**. The cross-plane thermal conductivity of the (010)-oriented substrate (i.e., in the [010] direction) agrees with values reported in literature (22.5-27.0 $\text{W/m}\cdot\text{K}$)^{5,35}. The TDTR measurements were performed next to each FIB region as well as in between the FIB regions where the thickness was estimated via linear interpolation. It should be noted that results for the $\sim 1.828 \mu\text{m}$ region is not reported due to de-bonding near-edge interface which has resulted from the additional polishing process. Possible root causes for the discrepancy between the thermal conductivities of the bulk and thinned Ga_2O_3 include (i) the thickness dependence of the thermal conductivity of the Ga_2O_3 films (i.e., incoherent phonon-boundary scattering)^{36,37} and (ii) potential subsurface crystallographic imperfections (i.e., phonon-defect scattering) resulting from the wafer thinning/polishing processes.

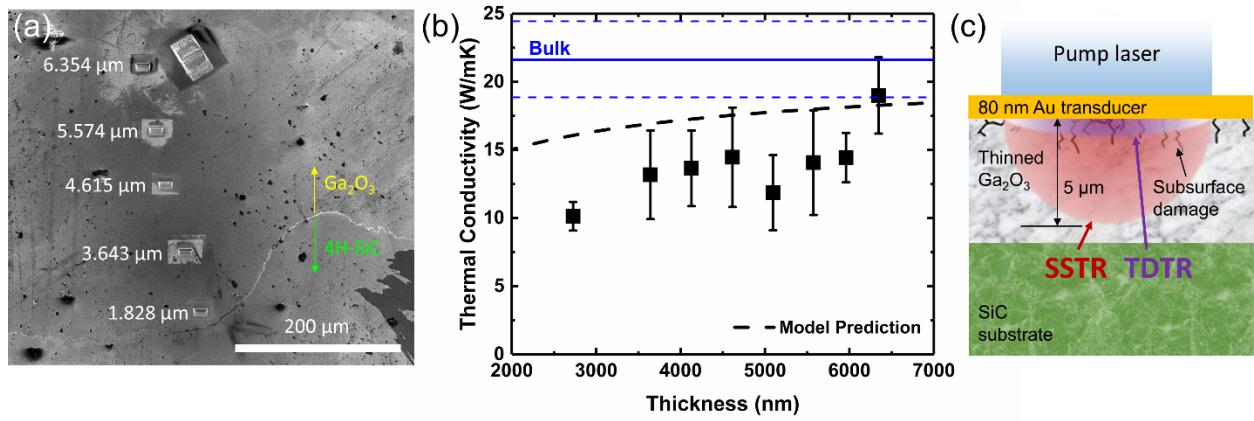


Figure 5. (a) Plan view 325 \times SEM image showing the locations of FIB milling and their corresponding thicknesses measured via cross-sectional SEM. (b) The measured thermal conductivity of the wedged Ga_2O_3 thin film and the bulk substrate. The blue dashed lines indicate the upper and lower bounds of the bulk thermal conductivity, i.e., error bars. Also shown are predictive modeling results used to estimate the thickness dependence of the Ga_2O_3 thermal conductivity in the [010] direction. (c) Probing volumes of TDTR and SSTR within the Ga_2O_3 composite wafer.

TDTR and SSTR²⁸ measurements were leveraged to determine whether subsurface defects are indeed present and impacting the thermal conductivity of the Ga_2O_3 layer. As shown in **Figure 5 (c)**, SSTR probes the through-thickness average thermal conductivity of the thinned Ga_2O_3 layer (the probing depth is 5 μm) whereas TDTR only probes the cross-plane thermal conductivity near the top surface of the films (the probing depth is 1.35 μm).²⁶ The directionally-averaged thermal conductivity of the pre-integrated (010) substrate and the post-integrated 6.5 μm Ga_2O_3 film were determined by SSTR to be $19.4 \pm 3.03 \text{ W/m}\cdot\text{K}$ and $18.4 \pm 3.39 \text{ W/m}\cdot\text{K}$, respectively. The difference between these results (5% reduction in the thermal conductivity) confirms the presence of phonon-boundary scattering effects, because the SSTR probes a volume that extends much deeper than the potential region with subsurface damages; otherwise, the thermal conductivities of the Ga_2O_3 bulk substrate and the film measured by SSTR should have been similar values. However, TDTR results in **Figure 5 (b)** show overall lower thermal conductivity values as compared to the model predictions. This suggests the presence of subsurface damages that reduce the near-surface cross-plane thermal conductivity of the thinned Ga_2O_3 layers.

The thermal conductivity accumulation function^{38,39} of bulk Ga_2O_3 in the [010] direction has been derived using first-principles calculations⁴⁰. This calculated phonon mean free path spectrum indicates that acoustic phonons with intrinsic mean free paths ranging from several nm to $\sim 1 \mu\text{m}$ carry a significant fraction of the heat in this crystalline system. Therefore, Ga_2O_3 films with a thickness on the order of 1-10 μm would exhibit a noticeable film thickness dependence for their thermal conductivities.⁴¹ It should be noted that a strong film thickness dependence of the thermal conductivity of single crystalline β -phase Ga_2O_3 in the [100] direction has been reported.⁴² **Figure 5 (b)** plots the measured thermal conductivities of the Ga_2O_3 layer with variable thickness along with the Debye-Callaway model³⁵ predictions (black dashed line). According to the Debye-Callaway model, the phonon-boundary scattering rate is dominant over impurity and Umklapp scattering rates, leading to the decreasing trend of the thermal conductivity as the film thickness reduces. The model predictions and

measurement data show reasonable agreement, which suggests that the thermal design of Ga_2O_3 composite substrates must account for the film thickness dependence of the Ga_2O_3 thermal conductivity.

TBR AT THE Ga_2O_3 /4H-SiC INTERFACE

The directionally averaged thermal conductivities of the 6.5 μm thick Ga_2O_3 layer and the 350 μm thick 4H-SiC substrate were measured by SSTR and were determined to be 18.4 $\text{W}/\text{m}\cdot\text{K}$ and 306.4 $\text{W}/\text{m}\cdot\text{K}$, respectively. With the knowledge of these parameters, the differential SSTR process illustrated in **Figure 2** was used to determine the effective thermal boundary resistance (TBR) at the Ga_2O_3 /4H-SiC interface. The mean value of the measured effective thermal boundary conductance (TBC) was 21.2 $\text{MW}/\text{m}^2\text{K}$, which corresponds to an effective TBR of 47.1 $\text{m}^2\text{K}/\text{GW}$. This TBR value is comparable to effective TBRs for GaN-on-diamond composite wafers formed via similar fusion bonding techniques using SiN_x adhesive layers with a similar thickness.^{12,43} However, this TBR is more than 3 \times higher than the reported value for a Ga_2O_3 /SiC interface with a 30 nm Al_2O_3 interlayer¹⁹, and a much lower TBR ($\sim 7 \text{ m}^2\text{K}/\text{GW}$) has been achieved via direct heteroepitaxial growth of Ga_2O_3 on SiC¹¹. The reason for the higher TBR in this study and strategies for potential improvement are discussed in the following text.

Due to the total thermal resistance in the SSTR probed volume being dominated by the 6.5 μm Ga_2O_3 film, the TBC has a relatively low measurement sensitivity (discussed later in **EXPERIMENTAL METHOD** section). The low sensitivity implies that a change in the TBC will have little impact on the measurement results. Even though the mean value for the TBC was fitted with the SSTR, the error range cannot be accurately determined. Therefore, FDTR was also performed on a thinner region of the wedged Ga_2O_3 on SiC (**Figure 5 (a)**) to determine the error bars of the TBC. The thickness (2.2 μm) of the Ga_2O_3 layer below the FDTR probing spot ($\sim 26.4 \mu\text{m}$ in diameter) was estimated based on two adjacent FIB regions. The FDTR measured effective thermal boundary conductance (TBC) was $23.4 \pm 7.6 \text{ MW}/\text{m}^2\text{K}$, which corresponds to an effective TBR of $42.8_{-10.5}^{+20.6} \text{ m}^2\text{K}/\text{GW}$ (the error bars for TBR are derived from the upper and lower bounds of the measured TBC; therefore, the error bars are asymmetric).

It should be noted that the effective TBR at the Ga_2O_3 /4H-SiC interface of the composite substrate is an aggregate of thermal resistance components arising from (i) the interfacial acoustic/diffusive mismatch between the Ga_2O_3 and the bonding layer, (ii) the low thermal conductivity bonding layer itself, and (iii) the interfacial acoustic/diffusive mismatch between the bonding layer and the 4H-SiC substrate. The theoretical TBR at the $\text{Ga}_2\text{O}_3/\text{SiN}_x$ and $\text{SiN}_x/4\text{H-SiC}$ interfaces were calculated using the acoustic mismatch model (AMM) and diffusive mismatch model (DMM) following the implementation presented by Bellis et al.⁴⁴ **Figure 6** shows the fractional contributions of the calculated interfacial transmission of phonons, and the equivalent thermal resistance from the 30 nm thick SiN_x adhesive layer to the effective Ga_2O_3 /4H-SiC TBR. The largest contribution arises from the SiN_x intermediate bonding layer due to its low thermal conductivity ($\sim 1.9 \text{ W}/\text{m}\cdot\text{K}$)⁴⁵ and its comparatively large estimated thickness (30 nm).^{20,46} Discussions on the SiO_x related data shown in **Figure 6** follows next.

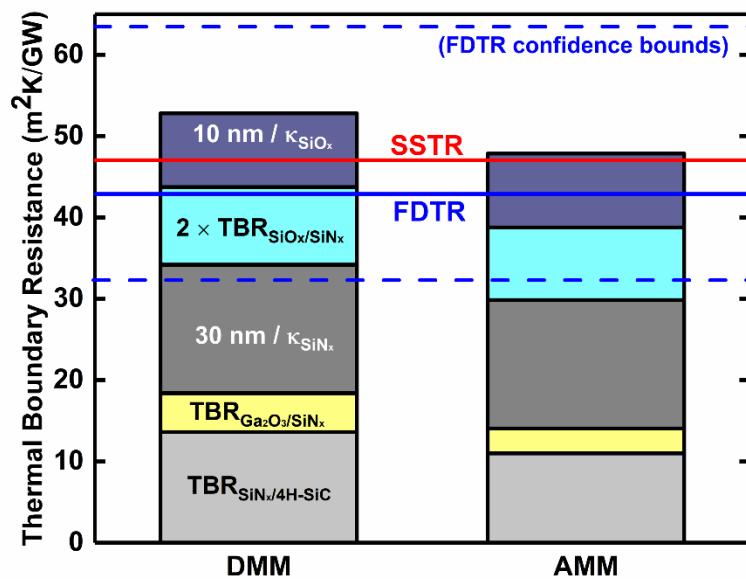


Figure 6. The effective TBR at the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ interface measured by the differential SSTR process and FDTR, and the calculated sum of individual resistive components that contribute to the overall effective TBR. Also shown are the thermal resistance components arising from the unintentionally formed 10 nm SiO_x interlayer within the SiN_x bonding layer. The blue dashed lines indicate the 95% confidence bounds for the FDTR measurement result.

To determine the accurate bonding layer thickness and to evaluate the interface quality and chemistry, scanning transmission electron microscopy (STEM) imaging and energy dispersive X-ray spectroscopy (EDX) mapping were performed. **Figure 7** shows a 10 nm SiO_x interlayer formed between the 15 nm thick SiN_x bonding layers that were joined together via fusion bonding. This SiO_x interlayer is typical of hydrophilic fusion bonding processes and is understood to result from the reaction of interfacial water and oxygen with silicon⁴⁷. The inset in **Figure 7 (a)** shows the nanodiffraction patterns from individual layers across the interface, and they confirm that the structure of the SiN_x layer remains amorphous. By considering the thermal resistance of this interlayer and the TBR at the two $\text{SiO}_x/\text{SiN}_x$ interfaces (from AMM and DMM calculations), the experimentally determined effective TBR shows good agreement with the theoretical calculation results. The low thermal conductivity of the SiO_x layer (1.1 W/mK⁴⁸) contributes 21% towards the total TBR determined by FDTR. Additionally, the acoustic and diffusive mismatch between the SiO_x and the SiN further increases the thermal resistance across the interface. These experimental and theoretical findings suggest that a minimum effective TBR of 20 m²K/GW (based on the prediction by DMM) can be achieved by eliminating the formation of the SiO_x interlayer (by, optimizing the activation process) and reducing the thickness of the SiN_x bonding layer to, for example, 3 nm. Other possible avenues for improving the TBR of the bond interface are reducing the roughness of each of the two bonding surfaces, optimizing the deposition parameters of the intermediate layer, and utilizing intermediate material with a higher thermal conductivity.⁴⁹

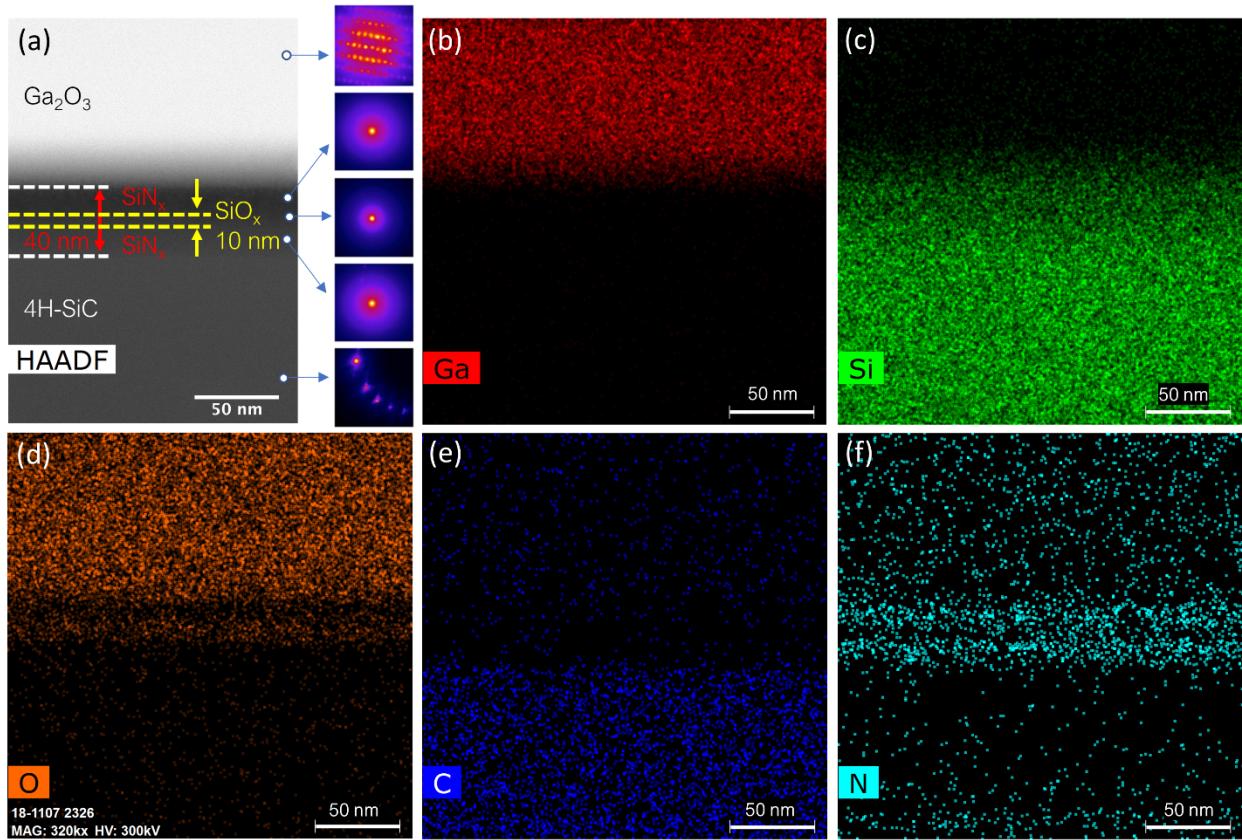


Figure 7. STEM-EDX for the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ interface. (a) A high angle annular dark field (HAADF) image. The inset in (a) shows the nanodiffraction patterns from individual layers shown in the cross section. (b) Ga (c) Si (d) O (e) C and (f) N EDX profiles. The elemental mapping represents the existence of both SiN_x bonding layer and SiO_x interlayer between the Ga_2O_3 film and 4H-SiC substrate.

IMPLICATIONS ON DEVICE THERMAL PERFORMANCE

Thermal simulation was performed using COMSOL Multiphysics to estimate the improvement in the device thermal performance by incorporating the Ga_2O_3 /4H-SiC composite substrate into the device design. An 85°C constant temperature boundary condition was applied on the bottom of surface of the devices, while a natural convection boundary condition (with a heat transfer coefficient, $h = 5 \text{ W/mK}$) was applied to the remaining surfaces. To calculate temperature, a $1 \mu\text{m}$ diameter domain probe adjacent to the drain side of the gate edge (**Figure 8 (b), (c)**) was used to mimic the results of Raman measurements in literature^{50,51}. It should also be noted that while the single channel model represented the full device geometry, in order to save computational resources, a quarter model of the 6-finger device was constructed taking into account of the four-fold symmetry. A hypothetical single channel homoepitaxial Ga_2O_3 metal-semiconductor field-effect transistor (MESFET) fabricated on a (010)-oriented Fe-doped semi-insulating Ga_2O_3 substrate is shown in **Figure 8 (a)**. The gate-to-source distance (L_{GS}), gate length (L_G), and gate-to-drain spacing (L_{GD}) were $1 \mu\text{m}$, $1.5 \mu\text{m}$, and $1.5 \mu\text{m}$, respectively. The gate width for this device was $185 \mu\text{m}$. More details of the thermal modeling procedure can be found in references^{50,52}. To simplify the thermal analysis, the device was assumed to operate under a fully-opened channel condition, where the gate-source voltage (V_{GS}) was kept at 0 V . Therefore, the heat generation profile across the channel was assumed as a uniform heat flux distribution.⁵³ Temperature-dependent thermal conductivity of the Ga_2O_3 substrate was adopted from reference⁵. For comparison, a hypothetical single channel MESFET fabricated on the Ga_2O_3 ($6.5 \mu\text{m}$)/4H-SiC ($350 \mu\text{m}$) composite wafer developed in this study (**Figure 8 (b)**) was simulated. The anisotropic temperature-dependent thermal conductivities of the Ga_2O_3 layer and 4H-SiC substrate were adopted from references³⁵ and^{21,54}, respectively. The directionally averaged thermal conductivities at room temperature measured in these references reasonably agree with the SSTR results for the composite substrate. **Figure 8 (d)** shows a comparison of the simulation results for the single channel homoepitaxial device and the device integrated with the composite substrate. The temperature rise was calculated for power densities ranging from 1 W/mm to 5 W/mm . The temperatures shown in **Figure 8 (d)** correspond to the average value within a $1 \mu\text{m} \times 1 \mu\text{m}$ area in the mid-point of the channel surface next to the drain side corner of the gate. The temperature rise (ΔT) and thus the junction-to-package device thermal resistance of the homoepitaxial device case was found to be ~ 4.5 times higher than that of the device fabricated on the composite substrate.

Figure 8 (e) compares the channel temperature rise of hypothetical 6-finger Ga_2O_3 MESFETs fabricated on a $500 \mu\text{m}$ thick (010)-oriented semi-insulating Ga_2O_3 substrate versus the Ga_2O_3 /4H-SiC composite substrate. A diagram of the 6-finger MESFET's device layout can be found in **Figure 8 (c)**. The homoepitaxial 6-finger device exhibits an extremely high device thermal resistance, which is ~ 2.3 times higher than that of a single finger device due to thermal crosstalk among adjacent channel regions dissipating heat.⁵⁵ However, if the composite substrate is utilized, heat dissipation is remarkably improved, and the resulting device thermal resistance is reduced from $\sim 370 \text{ mm}\cdot\text{K/W}$ for the homoepitaxy case to $\sim 42 \text{ mm}\cdot\text{K/W}$, which is far lower than other Ga_2O_3 FETs reported in literature⁵¹ and comparable to GaN-on-Si multi-finger devices⁵⁶. These results indicate that implementing a high heat transfer performance composite substrate will be essential for cooling practical multi-finger lateral FETs or reducing the device thermal resistance to a manageable level once the device technology matures.

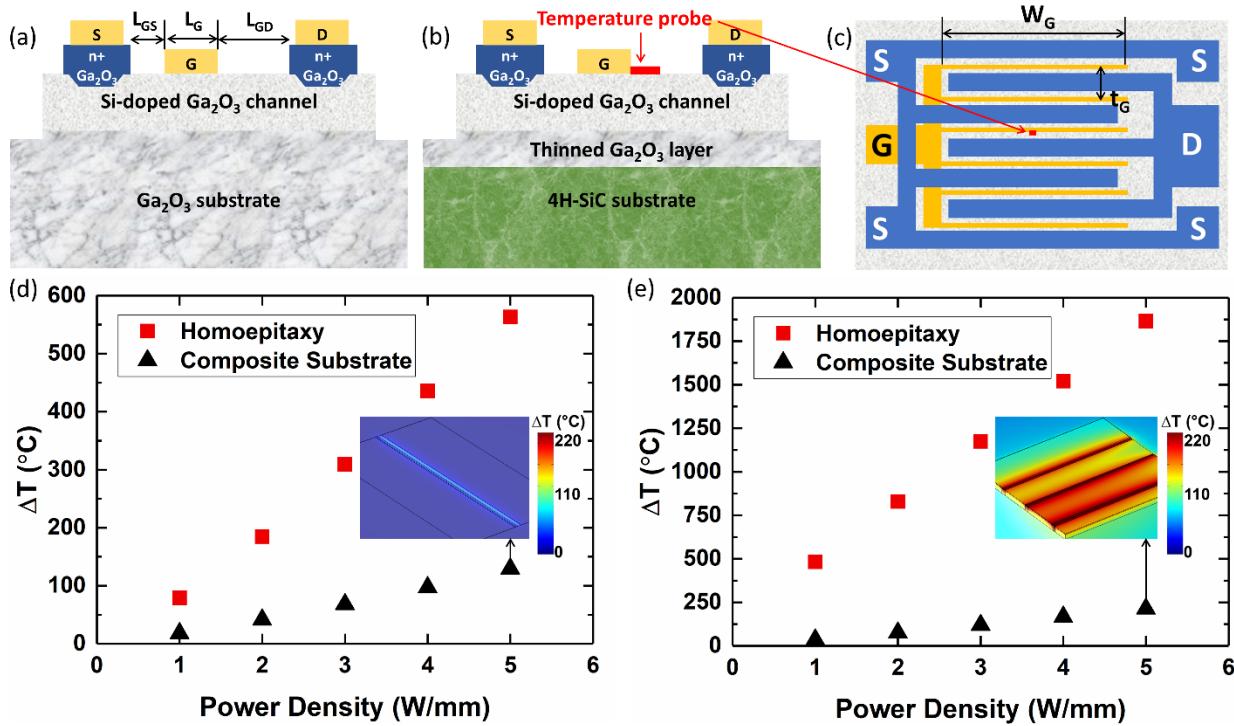


Figure 8. (a) Schematic of a simulated single-channel Ga_2O_3 MESFET. (b) Hypothetical MESFET fabricated over the Ga_2O_3 composite substrate. (c) The planar device layout of the hypothetical multi-finger Ga_2O_3 MESFET. (d) The simulated channel temperature rise of the single-finger homoepitaxial MESFET vs. the MESFET integrated with the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ composite substrate. The surface temperature profile of the “Composite Substrate” case for 5 W/mm power dissipation is shown in the inset. (e) The simulated channel temperature rise of 6-finger Ga_2O_3 MESFETs employing a 500 μm thick Ga_2O_3 substrate vs. the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ composite substrate. The surface temperature profile of the “Composite Substrate” case for 5 W/mm power dissipation is shown in the inset.

CONCLUSIONS

In this study, a novel $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ composite wafer with high heat transfer performance and an epi-ready surface finish was developed. The composite wafer meets the design requirement that will enable reliable thermal management for high power Ga_2O_3 lateral FETs as suggested by Chatterjee et al.⁷ Thermal characterization was performed with a combined approach of TDTR, FDTR, and SSTR. Notably, a differential-SSTR method was demonstrated to directly characterize the effective TBR at the $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ interface, which is inaccessible by TDTR and FDTR methods due to the relatively thick Ga_2O_3 layer (6.5 μm). The TBC measured by differential-SSTR (21.2 MW/m²K) is in good agreement with the FDTR measurement (23.4 ± 7.6 MW/m²K) performed after thinning the Ga_2O_3 layer. The TBC is mainly limited by the low thermal conductivity SiN_x bonding layer and an unintentionally formed SiO_x layer; therefore, the TBC can be further improved with optimization of the bonding process and interface. The thermal conductivity of the post-integrated/thinned (010) Ga_2O_3 layers (measured by TDTR) showed a strong film thickness dependence within a thickness ranging of 2.7 – 6.5 μm . The measured thickness-dependent thermal conductivities were overall lower than the Debye-Callaway model predictions. The discrepancy could be caused by the defects or the subsurface damages resulting from the thinning and polishing procedures. The collected thermal data highlights important thermal design considerations for developing similar composite wafers.

The $\text{Ga}_2\text{O}_3/4\text{H-SiC}$ composite wafer enables subsequent growth of homoepitaxial Ga_2O_3 layers and device fabrication. In this study, Si-doped Ga_2O_3 was homoepitaxially grown on the composite substrate by low-temperature MOVPE and has demonstrated promising electronic transport characteristics. The low-temperature MOVPE process demonstrated the feasibility to fabricate devices on the composite wafer without damaging the $\text{Ga}_2\text{O}_3/\text{SiC}$ interface.

The thermal performance of the composite wafer was studied via device thermal simulation. The composite substrate effectively cools a single finger MESFET to a ~4.5 times lower temperature rise as compared to a homoepitaxial device fabricated on a Ga_2O_3 substrate. Effective heat dissipation was demonstrated for a hypothetical multi-finger device where the device thermal resistance is reduced from ~370 mm·K/W to ~42 mm·K /W. The thermal simulation demonstrated the

composite wafer as a reliable thermal management solution that has the potential to facilitate mass production of commercial devices. Outcomes of this work will facilitate the electro-thermal co-design¹⁰ of next generation Ga_2O_3 power electronics with unparalleled performance, minimized form factor, and higher power density over current WBG device technologies. The new class of Ga_2O_3 electronics will reduce system-level cooling complexity and cost while increasing component lifetime. The performance gains in power switching for individual devices can lower wafer processing demands and manufacturing costs.

EXPERIMENTAL METHODS

STEADY-STATE THERMOREFLECTANCE (SSTR)

Steady-state thermoreflectance (SSTR) is a laser-based pump-probe technique, which is ideal to measure the thermal conductivity of bulk materials.²⁸ A metal transducer with a thickness of ~ 80 nm is deposited on the specimen. The reflectivity of this transducer changes linearly with temperature. The pump laser is modulated with a low-frequency square wave to introduce a periodic heat flux that results in a steady-state temperature rise. The change in the reflectivity in response to the reflected probe laser intensity is captured by a photodetector. Briefly, based on the linear relationship between temperature and heat flux under steady-state heating, the thermal conductivity of the specimen can be extracted. The detailed setup of the SSTR system used in this study has been described in our previous work.⁵⁷ The pump and probe lasers were focused on the sample with the following objectives: (1) a $2.5\times$ objective (NA = 0.08), which has pump and probe radius of $19.4\text{ }\mu\text{m}$ and $12.4\text{ }\mu\text{m}$, respectively, (2) a $10\times$ objective (NA = 0.25), which has pump and probe radius of $5\text{ }\mu\text{m}$ and $4.3\text{ }\mu\text{m}$, respectively. The pump and probe radii were measured using a scanning-slit optical beam profiler to evaluate the probe-averaged temperature rise in the thermal model.^{28,58} As shown in **Figure 9 (a)**, when the pump radius is at $5\text{ }\mu\text{m}$, the measurement has exclusive sensitivity to the Ga_2O_3 thermal conductivity. When the pump size increases, the thermal penetration depth increases, and therefore the measurement gains sensitivity to the TBC at the heterointerface. The thermal conductivity of the 4H-SiC is measured using a pre-integrated bare substrate, and the TBC at the metal transducer/sample interface is measured with by using calibration samples and assumed to be the same for the tested materials since the metal transducers are deposited on all of these samples simultaneously. In this work, single crystal sapphire was used as a calibration sample due to its well-known thermal conductivity of 33 W/mK .⁵⁹ A representative fitting result for SSTR measurements is shown in **Figure 10 (a)**.

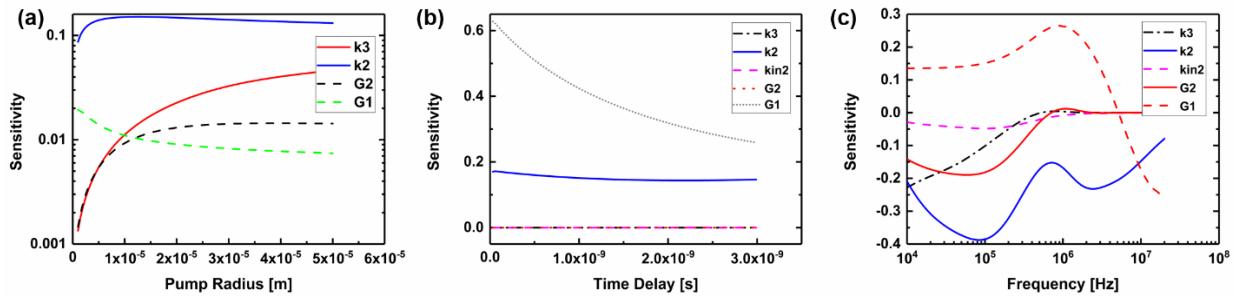


Figure 9. The sensitivity plot for the composite wafer for (a) SSTR on $6.5\text{ }\mu\text{m}$ -thick Ga_2O_3 on SiC, (b) TDTR on $3.6\text{ }\mu\text{m}$ -thick Ga_2O_3 on SiC, and (c) FDTR on $2.2\text{ }\mu\text{m}$ -thick Ga_2O_3 on SiC. In the legend, k_2 and kin_2 stand for the cross-plane and in-plane thermal conductivity of the Ga_2O_3 film, respectively. k_3 stands for the thermal conductivity of the 4H-SiC substrate. G_1 and G_2 stand for the thermal boundary conductance at the transducer/ Ga_2O_3 and Ga_2O_3 /4H-SiC interfaces, respectively.

TIME-DOMAIN THERMOREFLECTANCE (TDTR)

TDTR is an optical pump-probe technique that allows the extraction of thermal properties based on heat diffusion from ultrafast femtosecond laser pulses.^{25,60} Details of the TDTR setup used in this study has been described in our previous work⁶¹. The radius of the focused pump and probe beams were characterized using a scanning-slit optical beam profiler and were $8.4\text{ }\mu\text{m}$ and $6\text{ }\mu\text{m}$, respectively. Literature values were used for the thermal conductivity of Au as well as volumetric heat capacities (c_v) of Au⁶², β -phase Ga_2O_3 ⁶³ and 4H-SiC⁶⁴. The TBC between the metal transducer and the Ga_2O_3 films was fitted simultaneously with the Ga_2O_3 thermal conductivity. The TBC between the Ga_2O_3 films and the 4H-SiC substrate, the in-plane thermal conductivity, and the 4H-SiC substrate thermal conductivity have little impact on the fitting process due to their low measurement sensitivity, as shown in **Figure 9 (b)**. Measurements were performed on three locations near each FIB location to account for errors in laser focusing, pump and probe alignment, and local variation of the material. The uncertainty was calculated based on 95% confidence bounds from the multiple measurements and $\pm 2\text{ nm}$ uncertainty associated with the transducer thickness. The same measurement approach was used for FDTR. A representative fitting result for TDTR measurements is shown in **Figure 10 (b)**.

FREQUENCY-DOMAIN THERMOREFLECTANCE (FDTR)

FDTR is an optical pump/probe technique that measures material thermal properties based on fitting the phase of the thermal wave over a range of modulation frequencies^{27,65}. Details of the FDTR setup used in this study can be found in our previous work⁶¹. The radius of the focused pump and probe beams were characterized using a scanning-slit optical beam profiler and were 13.4 μm and 13.1 μm , respectively. Material properties used to post-process the FDTR raw data were identical to those used in the analytical model for TDTR experiments. As shown in **Figure 9 (c)**, the in-plane thermal conductivity of the Ga_2O_3 has low sensitivity. The TBC between the metal transducer and the 4H-SiC substrate and the 4H-SiC thermal conductivity were simultaneously determined (fitted) by characterizing a bare 4H-SiC substrate. A metal transducer/ Ga_2O_3 TBC identical to the metal transducer/4H-SiC TBC was assumed for the wedge-shape thinned Ga_2O_3 composite substrate because an identical transducer deposition procedure was used for these samples. The 4H-SiC thermal conductivity was used as a known parameter for subsequent measurement, where the TBC between the Ga_2O_3 layer and 4H-SiC and the Ga_2O_3 thermal conductivity were simultaneously determined during the characterization of the composite wafer. A representative fitting result for FDTR measurements is shown in **Figure 10 (c)**.

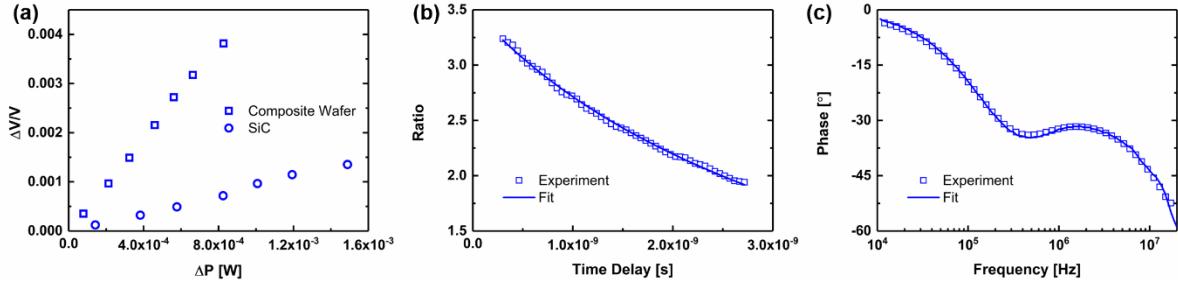


Figure 10. (a) SSTR measurement results for the composite wafer and 4H-SiC substrate using a 19.4 μm pump radius. The difference between the slopes for the 4H-SiC and the composite wafer data corresponds to the total thermal resistance of the 6.5 μm -thick Ga_2O_3 layer and the effective TBR. The TBR was extracted by conducting SSTR measurements on the 6.5 μm -thick Ga_2O_3 layer using a 5 μm pump radius (not shown), which allowed to perform the differential SSRT process. Representative data fitting results for (b) TDTR on a 3.6 μm -thick Ga_2O_3 layer on 4H-SiC, and (c) FDTR on a 2.2 μm -thick Ga_2O_3 layer on 4H-SiC, where the Ga_2O_3 /SiC TBC and the Ga_2O_3 thermal conductivity were simultaneously fitted.

SCANNING TRANSMISSION ELECTRON MICROSCOPY (STEM)

Scanning Transmission Electron Microscopy (STEM) samples were prepared using focused ion beam (Thermofisher Helios Dual-beam FIB). To retain a clean and thin specimen, the surface of the STEM foils was cleaned using low energy ion milling (Fischione Nanomill) operated at 500 eV. The high angle annular dark field (HAADF) STEM imaging was performed using Thermofisher aberration-corrected Titan STEM with probe convergence half angles of 10.03 mrad at an accelerating voltage of 300 kV. The microscope is also equipped with ChemiSTEM Energy dispersive X-ray spectroscopy (EDX) system, which allows for the characterization of the composition of the cross-section STEM sample. Five chemical species (Ga, Si, O, C, and N) at the interface were analyzed by the EDX elemental mapping. The 40 nm SiN_x adhesive layer was determined at the interface region. Due to the inhomogeneity of the lattice mismatch between the Ga_2O_3 thin films and 4H-SiC substrate, the SiN_x bonding interface was marginally delaminated, resulting in the oxidation layer of 10 nm SiO_x within the SiN_x interfacial region. The elemental profile further demonstrated the distribution of O based on the cross-section STEM-EDX measurements.

THEORETICAL CALCULATIONS

THERMAL CONDUCTIVITY MODELING

The Debye-Callaway model was applied to obtain the thickness-dependent thermal conductivity of β -phase Ga_2O_3 single crystals along the [010] direction.³⁵ The phonon-phonon Umklapp scattering, phonon-impurity scattering, and phonon-boundary scattering are included in the resistive phonon scattering processes of the model. The scattering rates of the three scattering mechanisms are expressed as:

$$[\tau_U^j(x)]^{-1} = \frac{k_B^2 \gamma_j^2}{M \hbar v_j^2 \theta_j} x^2 T^3 e^{-\frac{\theta_j}{3T}} \quad (1)$$

$$[\tau_I^j(x)]^{-1} = \frac{V k_B^4 \Gamma}{4 \pi \hbar^4 v_j^3} x^4 T^4 \quad (2)$$

$$[\tau_B^j]^{-1} = \frac{2 v_j}{d} \quad (3)$$

where k_B is the Boltzmann constant, T is the temperature, \hbar is the reduced Planck's constant, q is the Debye temperature, v is the sound velocity, subscript “ β ” denotes the branch in the phonon dispersion spectrum, and $x = \hbar\omega/k_B T$ with ω being the angular frequency. For β -phase Ga_2O_3 , $V = 1.0587 \times 10^{-29} \text{ m}^3/\text{atom}$ and $M = 6.2231 \times 10^{-26} \text{ kg/atom}$. The Grüneisen parameters, γ_L and γ_T , are treated as two fitting parameters and are obtained by fitting the temperature-dependent thermal conductivity from 80 to 400 K to the first-principles calculations along the [010] direction of bulk β -phase Ga_2O_3 . The parameters that were used in the model calculation are listed in **Table 2**. These parameters were derived from the aforementioned first-principles calculations.⁵

Table 2. Zone-boundary frequencies $f_{L,T}$ and phonon (sound) velocities $v_{L,T}$ of longitudinal and transverse phonons for β -phase Ga_2O_3 along the [010] direction from the first-principles calculations. $\theta_{L,T}$ are the Debye temperatures calculated from these cutoff frequencies following $\theta = \frac{2\pi\hbar f}{k_B}$. $\gamma_{L,T}$ are the Grüneisen parameters.

Parameter	f_L	f_{T1}	f_{T2}	v_L	v_{T1}	v_{T2}	θ_L	θ_{T1}	θ_{T2}	γ_L	γ_T
Unit	(THz)	(THz)	(THz)	(m s ⁻¹)	(m s ⁻¹)	(m s ⁻¹)	(K)	(K)	(K)		
Value	4.6	3.0	2.4	7270	3590	1960	220	144	115	1.1	0.85

ACOUSTIC MISMATCH (AMM) AND DIFFUSIVE MISMATCH (DMM) MODELING

The acoustic mismatch (AMM) and diffusive mismatch (DMM) models were implemented to calculate the interfacial thermal conductance (TBC) for the β -phase $\text{Ga}_2\text{O}_3/\text{SiN}_x$, $\text{SiN}_x/4\text{H-SiC}$, and $\text{SiO}_x/\text{SiN}_x$ interfaces. The AMM and DMM models are based on the Landauer formalism following the general Landauer formula for the TBC expressed as:

$$G = \sum_p \frac{1}{2} \int_0^{\omega_d} \int_0^{\pi/2} D_1(\omega) \frac{df_{BE}}{dT} \hbar\omega v_1(\omega) \tau_{1,2}(\theta, \omega) \cos(\theta) \sin(\theta) d\theta d\omega \quad (4)$$

The index p indicates the phonon branch, ω_d represents the cutoff frequency, D represents the phonon density of states (DOS), ω represents the angular frequency, f_{BE} is the Bose-Einstein distribution function of phonons, T is the temperature, \hbar is the reduced Planck constant, v is the phonon group (or sound) velocity, $\tau_{1,2}$ is the transmission coefficient from the medium 1 to 2, and θ is the angle of incidence. The major difference in the mathematical expressions for the AMM and DMM models relies on the definition of the transmission coefficients. The transmission coefficient is defined in terms of ω for the DMM and, for the AMM, θ and ω are involved in the definition of $\tau_{1,2}$. Thus, for the AMM, the transmission coefficient can be expressed as

$$\tau_{1,2,\text{AMM}}(\theta, \omega) = \frac{4 \frac{Z_2}{Z_1} \cdot \frac{\cos(\theta_2)}{\cos(\theta_1)}}{\left(\frac{Z_2}{Z_1} + \frac{\cos(\theta_2)}{\cos(\theta_1)} \right)^2} \quad (5)$$

where Z represents the acoustic impedance. On the other hand, the transmission function for the DMM model as a function of the frequency can be written as follows:

$$\tau_{1,2,\text{DMM}}(\omega) = \frac{\sum_p M_2(\omega)}{\sum_p M_1(\omega) + \sum_p M_2(\omega)} \quad (6)$$

where M is the phonon number of modes of mediums 1 and 2. Since the transmission coefficient for the DMM model is not dependent on the incidence angle, the integration θ is not required, and the mathematical expression for the TBC can be simplified. The calculations of the TBC using the AMM and DMM models are based on the formulation presented by Bellis et al.⁴⁴, and **Table 3** lists the main parameters required for these calculations.

Table 3. Implemented parameters for the calculations of the thermal boundary conductance (G) using the AMM and DMM formulations.

Medium A	Medium B	Speed of sound [m/s] v_L, v_T		Mass density [kg/m ³]		G_{AMM}	G_{DMM}
		Medium A	Medium B	Medium A	Medium B	[MWm ⁻² K ⁻¹]	[MWm ⁻² K ⁻¹]
4H-SiC [0001]	SiN_x [111]	13200, 6900 ⁶⁶	23189, 9276 ⁶⁷	3210	3100	91.0991	73.6241

β -Ga ₂ O ₃ [010]	SiN _x [111]	7800, 3550 ⁵	23189, 9276 ⁶⁷	5880	3100	327.8500	208.8000
SiO ₂ [Amorph.]	SiN _x [111]	5800, 3700 ⁶⁸	23189, 9276 ⁶⁷	2650	3100	224.3095	209.5125

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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